24.5 A 20Gb/s Broadband Transmitter with Auto-Configuration Technique

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The ever-growing volume of communication over backplane channels necessitates transceivers with equalization techniques. Among the existing solutions, transmit pre-emphasis manifests itself in its simplicity and accuracy. However, making it adaptive is not a trivial work due to the lack of eye-opening information from the receive side, unless a back channel or a bidirectional topology is included [1, 2]. In this paper, an adaptive scheme that automatically configures the transmitter at power up without using any additional trace is presened. A 20Gb/s feedforward transmitter and a collaborating receiver verify this approach, where adaptive pre-emphasis is achieved without extra power consumption.

To estimate the channel loss from the transmit side, one must acquire a certain index both appreciable and monotonically (either directly or inversely) proportional to the length of the channel. For a certain medium once the length is determined, the transmitter can adjust the boosting accordingly to optimally compensate the channel loss. Some ranging techniques such as roundtrip time-of-flight measurement [3] are impractical here, simply due to the heavy loss of the media and inadequate sampling bandwidth. One solution is to form an artificial loop through the differential traces and make it oscillate as shown in Fig. 24.5.1. During calibration, both transmitter and receiver are disconnected from the channels and odd-number inverters (5 in this design) are inserted between the 2 transmission lines. Such a ring oscillator must satisfy Barkhausen criteria to ensure stable oscillation along the loop. The resonance frequency, determined by gate and propagation delays, can be precisely calculated by the 20GHz input clock. To be more specific, T_D denoes the average gate delay of the inverters and the steady-state oscillation frequency is obtained as

$$f_0 = \frac{1}{10T_D + \frac{4l}{v}}, \quad (1)$$

where l represents the trace length and v the group velocity. With this resonance frequency known, the transmitter can estimate the length and therefore the loss of the channel. The optimal coefficients for the FIR filter are obtained by looking up a built-in table that contains predefined data. In real applications, adaptive equalizers in the receive side could be used as well to overcome the PVT variations.

It is worth noting that two 50Ω terminators (R_{ring}) must be placed temporarily when the transmitter is under configuration, otherwise the reflection would severely degrade the signal integrity and prohibit the loop from oscillation. It goes back to normal data delivery mode when the calibration procedure is done. With the inverters disabled and R_{ring} removed, the transmitter and receiver reconnect to the channel lines with balanced 50Ω terminations on both ends to conduct high-speed data transmission.

The architecture of the full transceiver is shown in Fig. 24.5.2, where a single-tap half-bit-spaced pre-emphasis driver is used to perform the equalization. R_1-R_2 and S_1-S_2 combination serves as the terminator R_{ring} in Fig. 24.5.1, providing bias voltage of around $V_{DD}/2$ under configuration. The loading resistor R_L is actually realized as on-resistance of MOS switches, that facilitates impedance control as follows: at data transmission, R_L is regulated to 50Ω and R_3, R_4, together with the on-resistance of S_5 form a total termination resistance of 100Ω to providing on-chip termination on both sides; under calibration, R_L, S_5, and some other switches inside the output driver are turned off completely to isolate the traces and allow ring oscillation. Calculating the frequency and selecting an appropriate coefficient (from ROM), the configuration unit sends the result to the output driver in a 6b digital format. In this prototype, the configuration unit is realized externally for simplicity. Note that this technique can be easily extended to multiple-tap transversal filters as long as more sophisticated tables are established.

Figure 24.5.3 depicts the proposed output driver along with the 50Ω regulator. Two inputs D_{in} and D'_{in} are summed up with different weightings, and the tuning is accomplished by changing the tail currents I_{SS1} and I_{SS2}. Note that the total amount of I_{SS1} and I_{SS2} remains as a constant (= I_{tot}). This arrangement creates a fixed common-mode level of 0.9V, allowing precise termination control. Under self-configuration, transistors M_5-M_8 and switches S_1-S_2 are off to seclude the channels from supply and ground. During data transmission, the NMOS (M_5 and M_7) and PMOS (M_6 and M_8) devices are regulated by V_{CN} and V_{CP}, respectively, to maintain 50Ω resistance on each arm. To generate V_{CN} and V_{CP}, the output common-mode is applied to an opamp and are compared with a reference voltage, which is nominally equal to 0.9V and is produced by a scaled-down replica consisting of I_{SS3} (= I_{tot}/8), switch S_3, transistor M_9, and resistor R_3 (=200Ω). Here, M_5 and M_7 inevitably require control voltage >1.2V, suggesting a second supply of 1.8V for the opamp and subsequent circuits. The negative feedback develops stable outputs of V_{CN} ≈ 1.6V and V_{CP} ≈ 0.2V. It is worth noting that I_{SS1}, I_{SS2}, and I_{SS3} are mirrored from the same source, making the loadings composed of transistors M_5-M_8 closely follow one-fourth of R_3. Inductive peaking technique is used to extend the bandwidth.

The transmitter and receiver are fabricated in 90nm 1P9M CMOS technology. The chips are mounted on a PCB with input/output pads wirebonded to the traces. The transceiver consumes 125mW from dual 1.2V and 1.8V supplies, of which 105mW is dissipated in the transmitter and 20mW in the receiver.

Figure 24.5.4 plots the measured oscillation frequency of the calibration ring and the optimal coefficient α (the current tuning factor in Fig. 24.5.3) for different channel lengths. Good matching can be observed between the simulated and measured oscillation frequencies, and interpolation could be used to determine the coefficient α for any arbitrary length < 20cm. The oscillation waveform of the 15cm channel under calibration is captured by probing the channel directly with high-impedance sampling head. As depicted in Fig. 24.5.5, it suggests an amplitude of 167mV and a frequency of 221.7 MHz. Figure 24.5.6 shows the outputs of the receiver in response to a 15Gb/s and a 20Gb/s 2^{31}-1 PRBS after 0.5cm and 20cm channels with and without the adaptive pre-emphasis. The rms data jitter measures 1.55 and 2.69ps, respectively, in the presence of an intrinsic jitter of 0.95ps from the pattern generator. The transceiver with 5cm channel achieves error-free operation (BER < 10^{-12}) up to 20Gb/s. Figure 24.5.7 shows a micrograph of the die. The transmitter occupies 1.0×0.7mm^2, and the receiver 0.7×0.3mm^2 including pads.

Acknowledgments:
The authors thank MediaTek and National Science Council (NSC) for support and TSMC for chip fabrication.

References:

[1] K. Yamaguchi, K. Sunaga, S. Kaeriyama, et al., "12Gb/s Duobinary Signaling With ×2 Oversampled Edge Equalization," *ISSCC Dig. Tech. Papers,* pp. 70-71, Feb., 2005.
[2] Y Tomita, H. Tamura, M. Kibune, et al., "A 20Gb/s Bidirectional Transceiver Using a Resistor-Transconductor Hybrid," *ISSCC Dig. Tech. Papers,* pp. 518-519, Feb., 2006.
[3] "15-04-0581-07-004a-ranging-subcommittee-final-report.doc," *IEEE P802.15*, Nov., 2004.

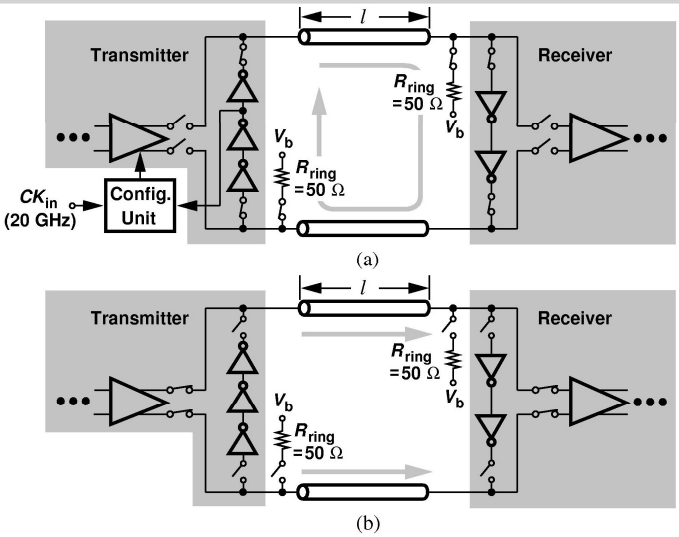


Figure 24.5.1: Operation of the transceiver under (a) calibration (b) normal data delivery.

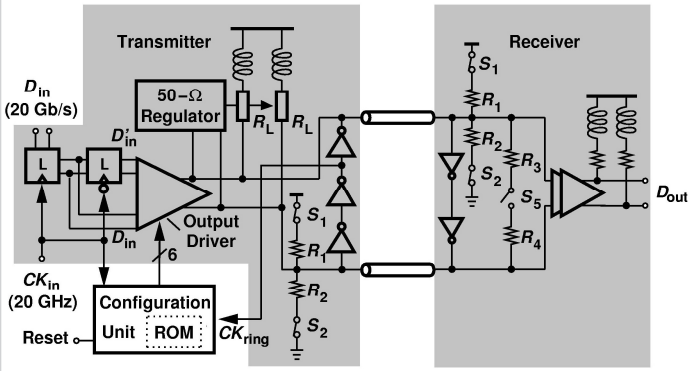


Figure 24.5.2: Transceiver architecture.

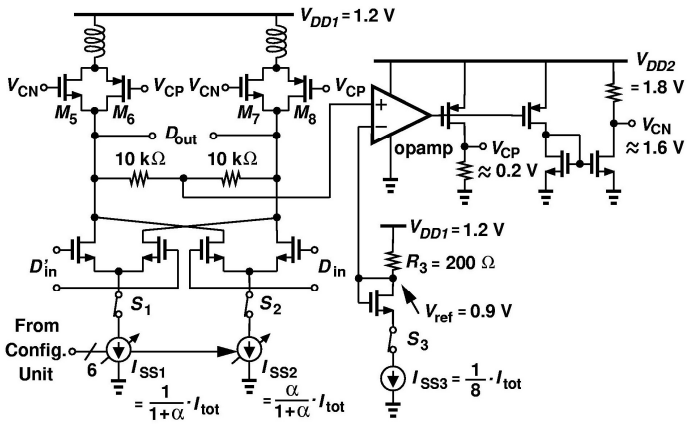


Figure 24.5.3: Output driver.

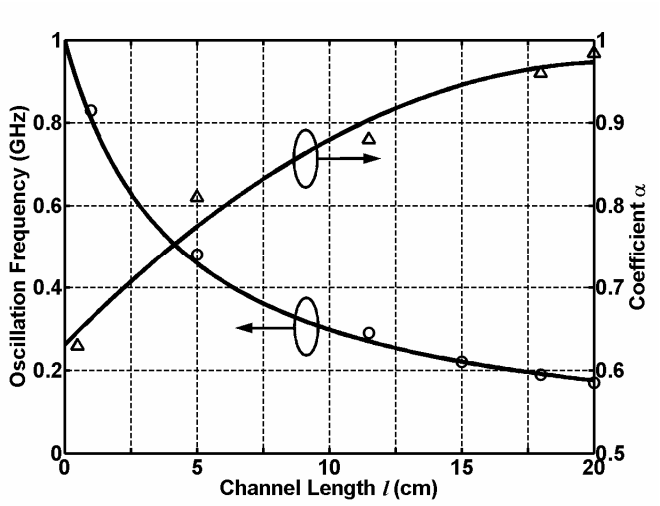


Figure 24.5.4: Measured oscillation frequency and optimal coefficient α.

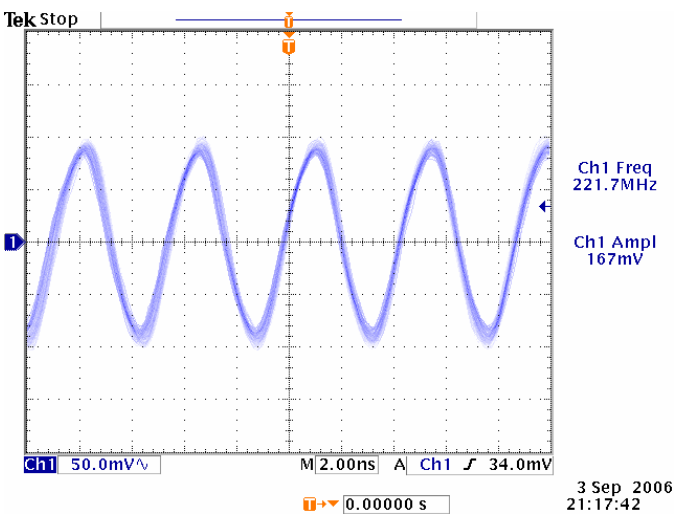
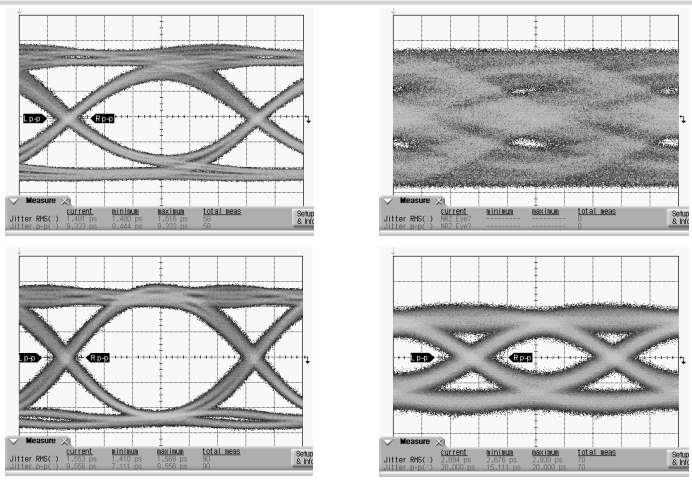


Figure 24.5.5: Measured oscillation waveform for 15-cm channel under configuration.



(a) (b)

Figure 24.5.6: Measured waveforms without (upper) and with (lower) adaptive pre-emphasis for data rate and channel length of (a) 15Gb/s, 0.5cm (b) 20Gb/s, 20cm (horizontal scale: 10ps/div).

Continued on Page 614

24

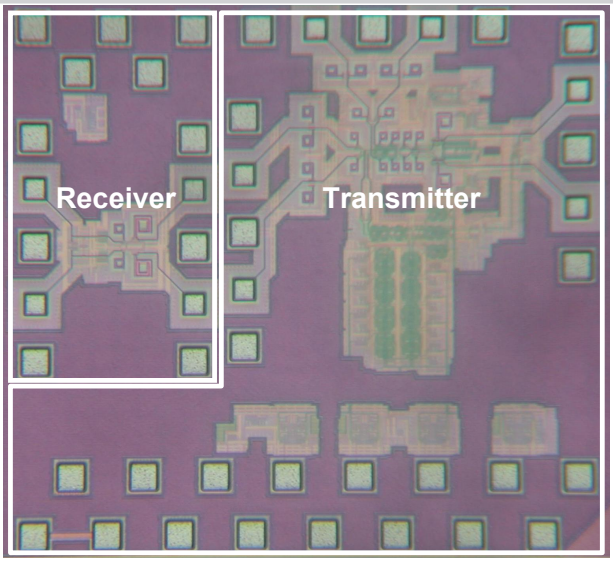


Figure 24.5.7: Chip micrograph.

