A 40-Gb/s Transmitter with 4:1 MUX and Subharmonically Injection-Locked CMU in 90-nm CMOS Technology

Huaide Wang and Jri Lee

National Taiwan University, Taipei, Taiwan

Abstract

A low-power low-jitter 40-Gb/s transmitter incorporating triple-resonance technique and subharmonically injection -locked CMU is presented. Designed and fabricated in 90-nm CMOS technology, this chip provides 4:1 multiplexing and achieves 454 fs,rms output data jitter while consuming only 325 mW from a 1.5-V supply.

I. Introduction

Recently 40-Gb/s serial links have been demonstrated in advanced CMOS technologies [1][2]. While the bandwidth and jitter performance of these CMOS chips are fairly acceptable, their power consumption is as large as that of their bipolar counterparts. One primary reason is that CMOS circuits need to adopt many broadband techniques, which consume significant power. On the other hand, the phase noise performance of the clock multiplication unit (CMU) is of great importance, since it is imposed on the output data directly.

This paper presents a 40-Gb/s transmitter in 90-nm CMOS that incorporates triple-resonance technique to extend the bandwidth. A subharmonically injection-locked CMU providing ultra-low noise clock is also employed to suppress the jitter. Costing negligible power, this novel technique can bring down the high-frequency clock jitter to the level of crystal oscillators [3]. The circuit achieves fully-open output data eye with 454 fs,rms and 2.89 ps,pp data jitter, while consuming 325 mW from a 1.5-V supply.

II. Architecture

The transmitter design is shown in Fig. 1, where a two-stage tree structure constitutes the 4:1 multiplexing. To facilitate the testing, a built-in 2^7–1 PRBS generator is included to provide four 10-Gb/s pseudo-random inputs for the 4:2 MUX stage. An on-chip CMU provides 20-GHz and 10-GHz clocks for the two stages. As proven in [3], the subharmonic injection locking technique can considerably reduce the clock jitter. We here apply it to the CMU, resulting in a very clean data output. A current-mode 2:1 selector with class-AB biasing employs 3 peaking techniques to exploit the largest bandwidth. Note that fixed delays ΔT_1, ΔT_2, and ΔT_3 are placed between the selectors and retiming latches to accommodate the required phase difference. Owing to the precise clocking and sufficient bandwidth, we avoid the use of phase interpolator or delay-locked loop (DLL) and save significant power.

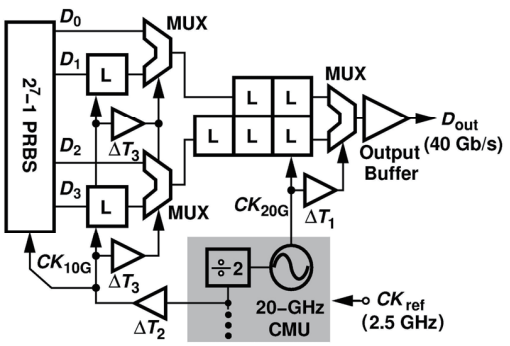

Fig. 1. Transmitter architecture.

III. Building Blocks

A. 40-Gb/s 2:1 Selector

The 40-Gb/s 2:1 selector is depicted in Fig. 2(a). Here, shunt and series peaking inductors (L_1 and L_2) are introduced in the output port to increase the bandwidth by resonating out the parasitic capacitance of the switching pairs M_1-M_4 and the output buffer. Theoretical analysis indicates a 3.5 × bandwidth improvement in small-signal operation. In large-signal mode with clock switching, the parasitic capacitance associated with common-source nodes P and Q affects the current transition time. The internal peaking technique [4] is therefore applied here to sharpen the steering currents of M_5 and M_6. As a result, a triple-resonance network ensures the largest bandwidth and maximum eye opening. Figure 2(b) illustrates the simulated large-signal performance (i.e., the eye opening) for different peaking techniques. With the same power consumption, the triple-resonance selector can maintain 90% eye opening up to 50 Gb/s. Note that we employ stacking inductors to minimize the area and ease the routing.

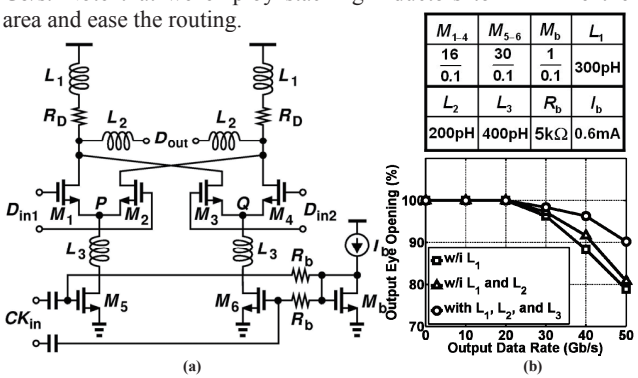

Fig. 2. (a) 40-Gb/s selector designs, (b) eye opening comparison.

B. 20-GHz CMU

The CMU design is depicted in Fig. 3. Based on the subharmonic injection technique, it utilizes the clean reference (CK_{ref}) to correct the accumulated VCO phase error periodically. A fixed delay (approximately 25 ps) together with an XOR gate creates pulses (V_{inj}) on occurrence of CK_{ref} transitions, leading to a double-edge injection periodically appearing every 4 cycles. The rule of thumb is that the output phase noise ($\mathcal{L}_{out}$) within the lock range would be reshaped to $\mathcal{L}_{ref}+20\log_{10}N$, where $\mathcal{L}_{ref}$ denotes the phase noise profile of the reference and N the frequency ratio. As the offset frequency increases, $\mathcal{L}_{out}$ would gradually deviate from the governance of $\mathcal{L}_{ref}$ beyond the lock range and approach the original phase noise of the PLL without injection locking. Here, a proper delay ΔT_1 is required so as to ensure the injection locking does not damage the original phase locking of the loop. It can be demonstrated (both theoretically and experimentally) that a wide

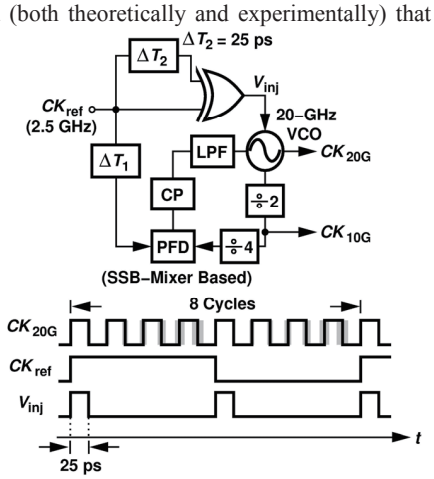

Fig. 3. CMU design with subharmonic injection locking.

tolerable range (>200°) for ΔT_1 is expectable in regular design, and a fixed ΔT_1 is sufficient for the loop to stay in stable over supply and temperate variations of ±10% V_{DD} and 85°C. Note that large frequency ratio can also be accommodated by using cascading. The technique can achieve ultimately-low jitter as long as the subrate reference (CK_{ref}) is clean enough.

C. PRBS Generator

The built-in PRBS generator is depicted in Fig. 4. Following the design in [5], we take 4 dependent bit sequences from the data chain of depth 7. Such an arrangement provides sufficient randomness while saving significant silicon area. Note that each 10-Gb/s input is a standard 2^7–1 PRBS, allowing the 40-Gb/s output to do BER testing through the Anritsu DMUX module (MP1804A) and BERT (MP1776A).

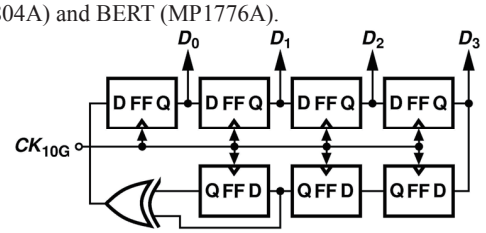

Fig. 4. 2^7-1 PRBS generator.

IV. Experimental Results

The transmitter has been designed and fabricated in 90-nm CMOS technology and tested on a high-speed probe station. Figure 5 shows the photograph of the die, which occupies 0.9 mm × 0.85 mm including pads. It consumes a total power of 325 mW, of which 105 mW dissipated in the PLL and 220 mW in the MUX core. The injection-locked PLL presents an operation range of 600 MHz (19.5~20.1 GHz). Figure 6 depicted the output phase noise with and without the subharmonic injection locking as well as the phase noise of the reference. The measured clock noise follows the reference profile tightly by 18 dB [= $20\log_{10}(20/2.5)$], resulting an integrated rms jitter (from 100-Hz to 1-GHz offset) of 182.9 fs. The time-domain measurement (363 fs) would yield similar result after deembeeding the instrument noise. Here the subrate clock output from MP1803A is applied as the reference. Note that the subharmonic injection technique is proven to be immune from PVT variations. Without any manual tuning, the PLL presents only 33 fs jitter deviation over 70°C temperature and 200-mV supply variations.

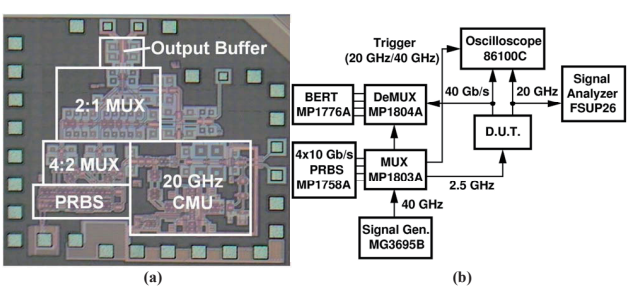

Fig. 5. (a) Die photo, (b) testing setup.

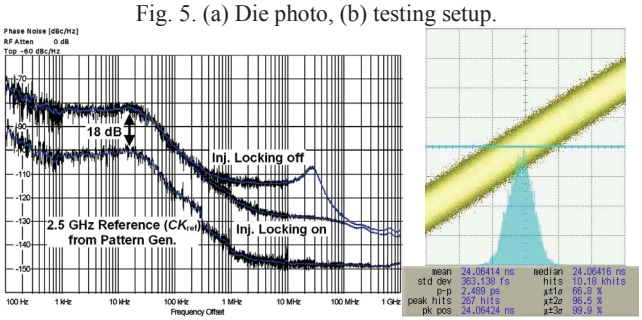

Fig. 6. (a) Phase noise, (b) time-domain jitter (vertical scale: 10 mV/div, horizontal scale: 1 ps/div) of the CMU output (CK_{20G}).

The output data is illustrated in Fig. 7, where very clean eye with large opening (280 mV, single-endedly) is demonstrated. Attributed to the excellent phase-noise of the clock, the output data reveals very low rms and peak-to-peak jitter of 454 fs and 2.89 ps, respectively. The signal integrity testing suggests a BER of less than 10^{-12}. Table I summaries the performance of this work and some other previously published 40-Gb/s transmitters. A comparison between recently published 40-Gb/s transmitters in terms of data jitter and power consumption is depicted in Fig. 8.

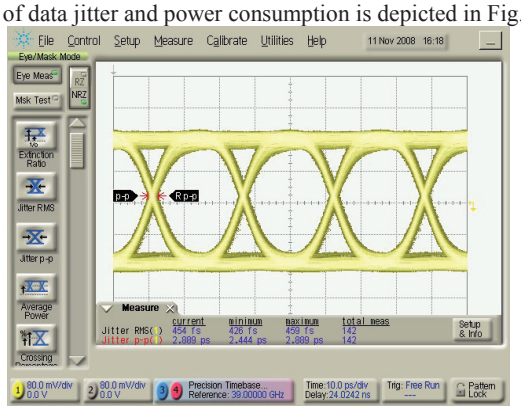

Fig. 7. Transmitter output at 39 Gb/s.

TABLE I
PERFORMANCE SUMMARY

	[1]	[2]	[6]	This Work
Data Rate (Gb/s)	39.8~44.6	35.2~38.6	36~43	39~39.6
Function	16:1 MUX CMU	16:1 MUX CMU	4:1 MUX CMU	4:1 MUX CMU
Output Data RMS Jitter	570 fs	1.53 ps	880 fs	454 fs
Clock RMS Jitter	265 fs	652 fs	254 fs	183 fs
Output Swing (Single-Ended)	500 mV_{p-p}	260mV_{p-p}	500 mV_{p-p}	280 mV_{p-p}
BER	<10^{-12} (2^{31}-1 PRBS)	N/A	<10^{-15} (2^{31}-1 PRBS)	<10^{-12} (2^7-1 PRBS)
Power Diss.	2.79 W	2.8 W	4.98 W	325 mW
Supply Voltage	1.8/1.1 V	1.5/1.3 V	1.8/-5.2 V	1.5 V
Area (mm^2)	25.5	9	8.25	0.77
Technology	65-nm CMOS	0.13-µm CMOS	0.18-µm BiCMOS	90-nm CMOS

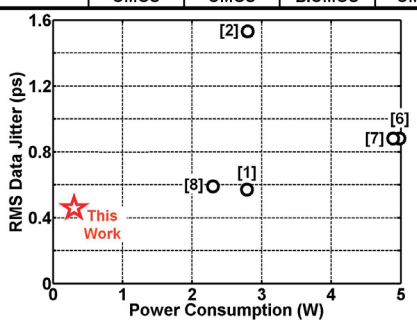

Fig. 8. Jitter and power consumption comparison.

Acknowledgement

The authors thank MediaTek, TSMC, and NSC for support.

References

[1] Y. Amamiya et al., "A 40Gb/s Multi-Data-Rate CMOS Transceiver Chipset with SFI-5 Interface for Optical Transmission Systems'' *ISSCC*, 2009.

[2] J. Kim et al., ''Circuit Techniques for a 40Gb/s Transmitter in 0.13µm CMOS'', *ISSCC*, 2005.

[3] Jri Lee and H. Wang, "Subharmonically Injection-Locked PLLs for Ultra-Low-Noise Clock Generation," *ISSCC*, 2009.

[4] Jri Lee et al., "A 20-Gb/s 2-to-1 MUX and a 40-GHz VCO in 0.18-µm CMOS Technology," *VLSI Symp.*, 2005.

[5] J. J. O'Reilly, "Series-parallel generation of m-sequences," *Radio Electron. Eng.*, 1975.

[6] H. Tao et al., "40–43-Gb/s OC-768 16:1 MUX/CMU Chipset with SFI-5 Compliance'', *JSSC*, 2003.

[7] D. K. Shaeffer et al., "A 40/43Gb/s SONET OC-768 SiGe 4:1 MUX/CMU'', *ISSCC*, 2003.

[8] M. Meghelli et al., "A 0.18-µm SiGe BiCMOS Receiver and Transmitter Chipset for SONET OC-768 Transmission Systems '', *JSSC*, 2003.