A 20-Gb/s 2-to-1 MUX and a 40-GHz VCO in 0.18-μm CMOS Technology

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Abstract

A 20-Gb/s MUX incorporates multiple resonance techniques and a 40-GHz VCO employs a differentially-stacked inductors. Fabricated in 0.18-μm CMOS technology, the MUX achieves a data jitter of 1.57 ps,rms and the VCO a phase noise of -90 dBc/Hz at 1-MHz offset.

I. Introduction

The ever increasing volume of data transmission over the internet necessitates the multiplexer (MUX) and voltage-controlled oscillator (VCO) to operate tens of gigahertz. Recent researches have demonstrated high-speed MUX circuits realized in SiGe technology [1][2], but they require 3 to 5-V supply and a few Watts of power. High-speed CMOS VCOs usually employ high-resistivity substrate, increasing the fabrication cost.

This paper presents the design and experimental verification of a 20-Gb/s 2-to-1 MUX and a 40-GHz VCO fabricated in standard 0.18-μm CMOS technology. The MUX achieves an output data jitter of 1.57 ps,rms with a power consumption of 22 mW, whereas the VCO arrives at a phase noise of -90 dBc/Hz at 1-MHz offset while consuming 1 mW from a 1-V supply.

The next section describes the design of the MUX circuit. Section III presents the VCO details, and section IV summarizes their experimental results.

II. MUX

A. Internal Peaking Technique

Although inductive peaking technique has been widely used to improve the bandwidth, a conventional current-steering selector with inductive peaking in the output still suffers from speed limitation due to the finite rise and fall times of internal nodes. As illustrated in Fig. 1(a), when the clock turns on, the parasitic capacitance C at node A must be discharged so as to lower V_A until either M_1 or M_2 is on. The -3-dB bandwidth ω_1 is therefore given by $(r_{O3}C)^{-1}$, where r_{O3} denotes the output resistance of M_3. The relatively large capacitance C considerably degrades the performance at high speed.

To raise the bandwidth associated with the internal nodes, a series inductor L is inserted between the clock and data stages [Fig. 1(b)], splitting C into two components [3]. Assuming M_1-M_2 pair and M_3 contribute approximately equal capacitance ($C/2$), we choose L to resonate with $C/2$ at $2\omega_1$ to minimize peaking: at $\omega = 2\omega_1$, the L-$C/2$ network acts as a short, absorbing all of I_{in} and causing $|V_A/I_{in}| = [2\omega_1(C/2)]^{-1} = r_{O3}$; at $\omega = 2\sqrt{2}\omega_1$, the π network of $C/2$-L-$C/2$ resonates, forcing all of I_{in} to flow through r_{O3} and making $|V_A/I_{in}| = r_{O3}$. (The two capacitors in the π network carry equal and opposite currents.) Quantitative analysis reveals that

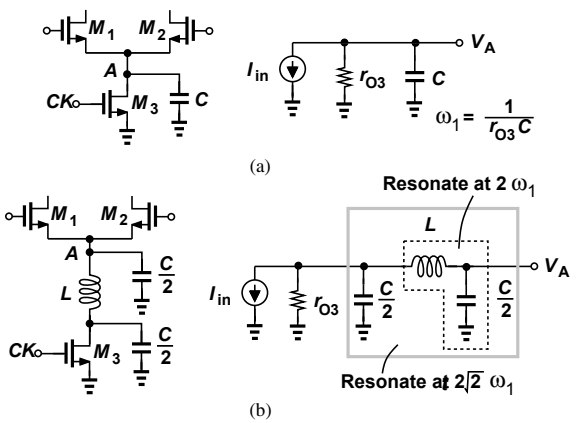


Fig. 1. Internal node behavior (a) without (b) with series inductor.

$$|\frac{V_A}{I_{in}}|(j\omega) = \frac{4r_{O3}}{\sqrt{[4-(\frac{\omega}{\omega_1})^2]^2 + [4(\frac{\omega}{\omega_1}) - \frac{1}{2}(\frac{\omega}{\omega_1})^3]^2}}, \qquad (1)$$

and the transfer function is plotted in Fig. 2. The peak (2.1 dB) and valley (-1.4 dB) occur at $2.5\,\omega_1$ and $1.3\,\omega_1$, respectively. The -3-dB bandwidth is approximately equal to $3.05\,\omega_1$. In other words, this technique extends the bandwidth by a factor of 3. In practice, the inductor L introduces parasitic capacitance and loss, limiting the bandwidth improvement to a lesser extent. The capacitance C is not splitted evenly either, necessitating careful design and simulations.

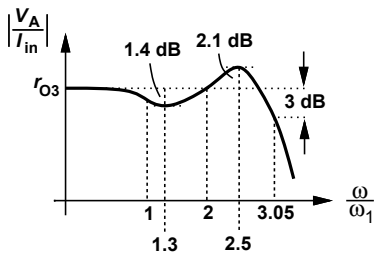


Fig. 2. Transfer function of the circuit in Fig. 1(b).

B. 2-to-1 MUX Design

Figure 3 depicts the proposed MUX, where the tail current source is eliminated to relax the voltage headroom requirement. Current switching in M_5-M_6 is accomplished by gate control, a "Class-AB" operation. Since the tail current source is removed, M_5-M_6 can be much narrower, presenting a smaller capacitance to the clock buffer. A large peak current

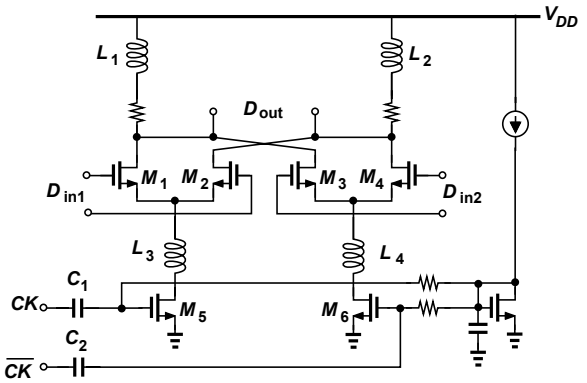


Fig. 3. 40-Gb/s selector.

is also created to provide greater voltage swings at the output. The coupling capacitors C_1 and C_2 are realized as fringe structure [4] using metal-2 through metal-5 layers. Simulation indicates a bottom-plate capacitance of only 5% on each side. The output is buffered by an inductively-peaked stage so as to relax the tradeoff between voltage swing and impedance matching. Simulation reveals that this circuit can operate at a speed beyond 30 Gb/s, although the limited testing environment only verify it up to 20 Gb/s.

III. VCO

The highest operation frequency that an LC oscillator can achieve depends on the quality factor (Q) and the self-resonance frequency (f_{SR}) of the inductor. It can be shown that, for a conventional LC oscillator with a cross-coupled pair, the resonance frequency ω_{osc} is given by

$$\omega_{osc} = Q\,\omega_T, \tag{2}$$

where ω_T denotes the transit frequency of the devices and the inductor's parasitic capacitance is neglected. In other words, an LC oscillator can operate at a very high frequency if the inductor provides a sufficiently high Q. In practice, neither the inductor's parastic capacitance is negligible nor can an on-chip inductor achieve very high Q, leading to an operation frequency typically less than ω_T. Thus, raising the f_{SR} and Q of the inductors becomes essential in high-speed VCO design.

A. Differentially-Stacked Inductors

Among the various inductor topologies, a stacked inductor provides a high f_{SR} by reducing the equivalent parasitic capacitance [5], but the asymmetric structure restricts its application in differential circuits. On the other hand, a differential (balanced) inductor achieves a higher Q by reducing the effect of substrate loss [6] and is well-suited for a differential stimulus. However, the interwinding capacitance somewhat lowers the f_{SR}.

A topology combining both structures is proposed to resolve the foregoing dilemma. As shown in Fig. 4(a), two layers of spirals are stacked differentially to preserve symmetry, allowing differential excitation. The strong mutual coupling

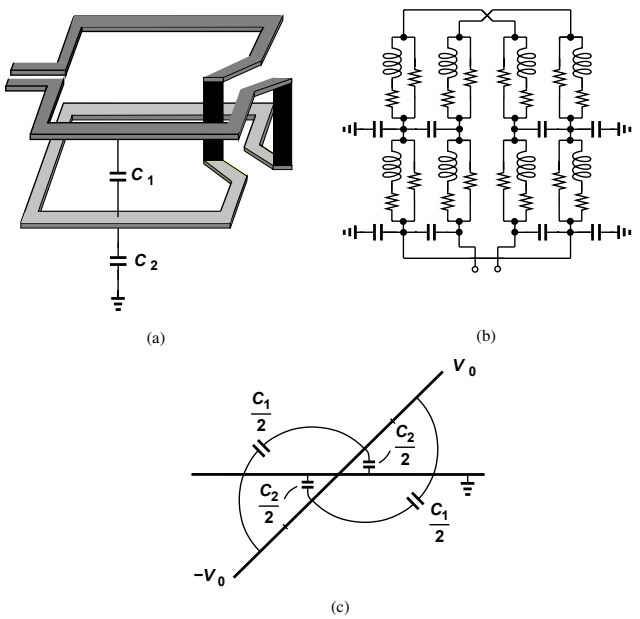


Fig. 4. (a)Proposed differentially-stacked inductor (b) its model (c) the voltage profile.

between the top and bottom layers forms a total inductance of nearly 4 times that of a single-layer inductor. Such a structure can be modeled as illustrated in Fig. 4(b). The inductance, layer-to-layer capacitance C_1, and layer-to-substrate capacitance C_2 are decomposed evenly into 8 segments, and loss is represented by the series and parallel resistances. Assuming perfect coupling between the two layers, we obtain the differentially-stimulated voltage profile [Fig. 4(c)], where C_1 experiences a constant voltage V_0 across it and C_2 a linear voltage variation from $-V_0/2$ to $V_0/2$. To calculate the equivalent capacitance, we equate the total electric energy stored in the structure for a peak differential voltage of $2V_0$ to $C_{eq}(2V_0)^2/2$, and obtain [5]

$$E_{elec} = \frac{1}{2}\,C_1\,\mathrm{V}_0^2 + 2\int_0^{C_2/2} \frac{1}{2}\left(\frac{x}{C_2/2}\frac{V_0}{2}\right)^2 dx = \frac{1}{2}\,C_{eq}(2V_0)^2, \tag{3}$$

yielding the equivalent capacitance as

$$C_{eq} = \frac{C_1}{4} + \frac{C_2}{48}. \tag{4}$$

Equation (4) reveals that C_1 impacts the self-resonance frequency 12 times as much as C_2. It is thus desirable to place the two layers of spirals far from each other, in agreement with the conclusion of simple stacked inductors in [5].

Figure 5 plots the simulated f_{SR} for three different inductor structures (stacked, differential, and the proposed) designed and optimized in a 0.18-μm CMOS technology with 6 metal layers. The proposed topology achieves at least 18% higher

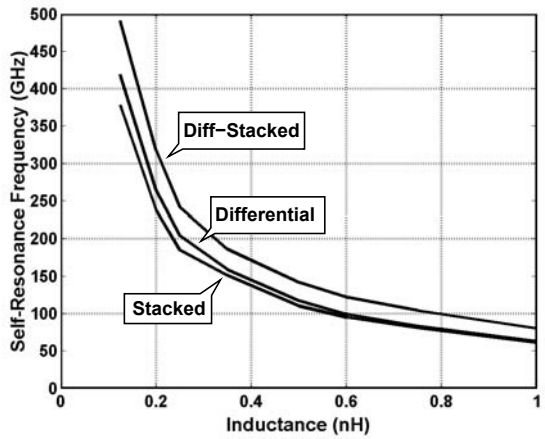


Fig. 5. Simulated f_{SR}.

f_{SR} than others. The differentially-stacked topology can be further extended to multiple-layer stacks as well. For a single-turn differential inductor with n stacked spirals, the equivalent capacitance is given by

$$C_{eq,multi} = \sum_{k=1}^{n-1} (\frac{n-k}{n})^2 C_k + \frac{C_n}{12n^2}. \quad (5)$$

It is also possible to implement a differentially-stacked inductor with multiple turns. Due to the complexity, these structures require electromagnetic simulations to develop accurate models.

B. VCO Design

As illustrated in Fig. 6, the VCO incorporates a cross-coupled pair with the proposed inductor and MOS varactors.

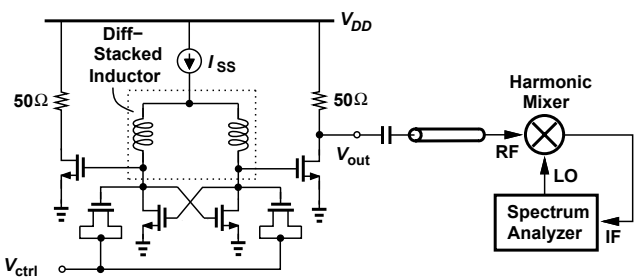
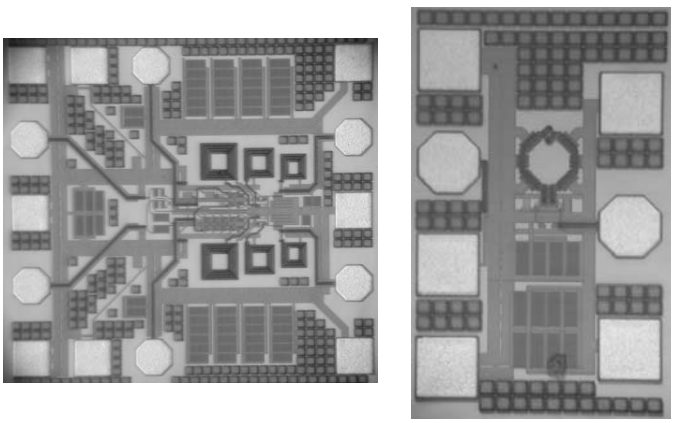


Fig. 6. VCO and its testing environment.

To further increase the Q, the inductor is implemented as an octagonal shape, and the bottomlayer of the inductor is realized as parallel shunt spirals connected through vias. To reduce the capacitive coupling to the substrate, a ground shield made of polysilicon sticks with minimum gap width is placed underneath the spirals in the direction perpendicular to the current flow [7]. The inductor model is obtained from electromagnetic simulations [8].

IV. Experimental Result

The MUX and VCO circuits have been designed and fabricated in 0.18-μm CMOS technology. Figure 7 shows the die photos, which measure 0.7×0.7 mm^2 and 0.3×0.45 mm^2, respectively, including pads. The on-chip high-speed lines are designed as 50-Ω microstrip lines to absorb the routing capacitance. Both circuits are tested on a high-speed probe station.



(a) (b)

Fig. 7. Chip photograph: (a) MUX (b) VCO.

To simplify the testing hardware, a built-in shift register is included in the MUX circuit to propagate the input data, providing two retimed input data sequences with only one pseudo-random binary sequence (PRBS) source.

The MUX circuit was tested the day before the paper submission deadline. Figure 8 depicts the preliminary results of the input and output waveforms in response to a 10-Gb/s pseudo-random input data of length $2^{31} - 1$, suggesting an rms and peak-to-peak jitter of 1.57 and 8.5 ps, respectively. The MUX consumes 22 mW from a 1.8-V supply excluding the buffer.

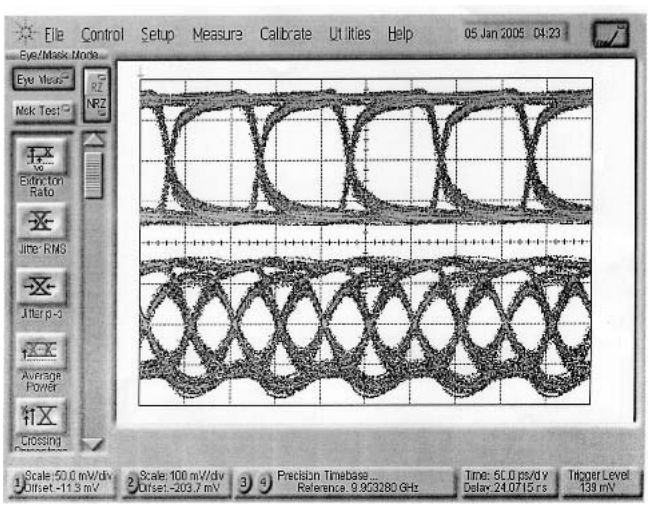


Fig. 8. Input and output waveforms of the MUX (horizontal scale: 50 ps/div, vertical scale: 100 mV/div).

The VCO achieves a phase noise of -90 dBc/Hz at 1-MHz offset while consuming 1 mW from a 1.3-V supply. Figure

9 plots the spectrum. The tuning characteristic is depicted in Fig. 10, where a tuning range of 1.4 GHz is obtained when the supply voltage is equal to 1.8 V. The "in-situ" measurement suggests an inductor Q of 12 at 40 GHz. The VCO begins to work at a tail current of 450 μA with a 1-V supply. This design presents a figure of merit [FOM, $L(\Delta f/f)^2P$] of -182 dBc/Hz. Table 1 summaries the performance of these two circuits and some other previously published works realized in standard CMOS technologies.

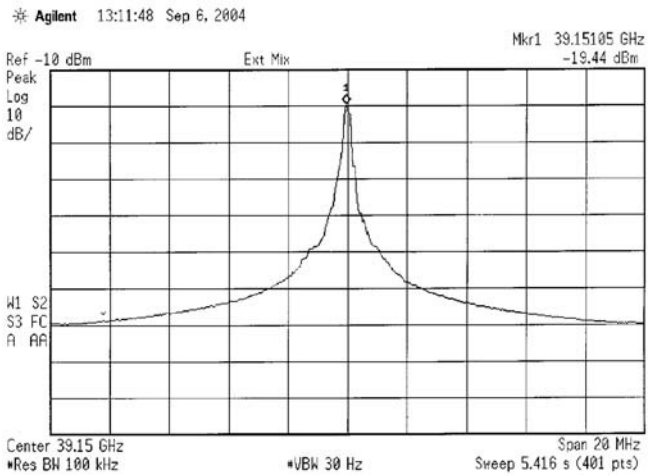


Fig. 9. VCO ouptut spectrum.

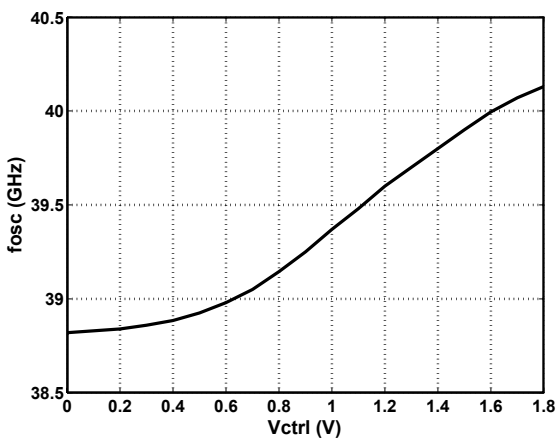


Fig. 10. VCO tuning range.

Parameter	[9]	[10]	[11]	This Work
Max. Output Data Rate	25 Gb/s	40 Gb/s	43 Gb/s	20 Gb/s
Function	2 : 1	2 : 1	2 : 1	2 : 1
Supply Voltage	1.5 V	1.5 V	1.8 V	1.8 V
Power Diss.	44 mW	100 mW	285 mW	22 mW
Technology	0.12−um CMOS	0.12−um CMOS	90−nm CMOS	0.18−um CMOS

(a)

Parameter	[12]	[13]	This Work
Frequency	43 Gb/s	51 Gb/s	40 Gb/s
Tunning Range	4.2 %	1.2 %	3.5 %
Phase Noise (@ 1−MHz offset)	−90 dBc/Hz	−85 dBc/Hz	−90 dBc/Hz
Supply Voltage	≥ 1 V	≥ 1 V	≥ 1 V
Power Diss.	7 mW	1 mW	1 mW
Chip Area	N/A	0.5 mm x 0.9 mm	0.3 mm x 0.45 mm
FOM	−174 dBc/Hz	−179 dBc/Hz	−182 dBc/Hz
Technology	0.13−um Standard CMOS	0.12−um Standard CMOS	0.18−um Standard CMOS

(b)

Table 1. Performance summary for (a) MUX (b) VCO .

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