13.7 A 40Gb/s Clock and Data Recovery Circuit in 0.18μm CMOS Technology

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Clock and data recovery (CDR) circuits operating at tens of gigabits per second pose difficult challenges with respect to speed, jitter, signal distribution, and power consumption. Recent integration of 10Gb/s receivers in CMOS technology encourages further research on CMOS solutions for higher speeds, especially if it leads to low-voltage, low-power realizations.

The design and experimental verification of a 40Gb/s CMOS phase-locked CDR is described. Shown in Fig. 13.7.1, the architecture incorporates a multiphase voltage-controlled oscillator (VCO), a quarter-rate phase detector (PD), a voltage-to-current (V/I) converter, and a simple loop filter. The PD uses the half-quadrature phases provided by the VCO to sample the input data every 12.5 ps, thereby detecting data edges and determining whether the clock is early or late. Four of these samples fall in the center of the data eye, retiming and demultiplexing the 40Gb/s input into four 10Gb/s outputs. In the absence of data transitions, the V/I converter generates no output current, leaving the oscillator control line undisturbed. With quarter-rate sampling, the flipflops' hold time can be four times as long as that required in full-rate operation, but their acquisition speed must still guarantee correct sampling of the input bits in less than 25ps.

The speed, jitter, and driving capability required of the oscillator point to the use of an LC realization. Coupled oscillators [1] operate away from the resonance frequency of the tanks to create the required phase shift, bearing a trade-off between reliability of oscillation and the phase noise. The multiphase oscillator in [2] drives transmission lines by a gain stage loaded by resistors, incurring energy loss in each cycle.

The multiphase oscillator introduced here is based on the concept of differential stimulus of a closed-loop transmission line at equally-spaced points. Illustrated in Fig. 13.7.2a, the circuit sustains a phase separation of 180° at diagonally-opposite nodes, providing 45° phase steps in between. Unlike coupled oscillators, this circuit does not operate away from the resonance frequency. Also, in contrast to the design in [2], the transmission line requires no termination resistors, displaying lower phase noise and larger voltage swings for a given power dissipation and inductor Q.

The topology of Fig.13.7.2a nonetheless necessitates long interconnects between the nodes and their corresponding $-G_m$ cells. However, since diagonally-opposite inductors carry currents that are 180° out of phase, the circuit can be modified as shown in Fig. 13.7.2b, where inductor elements are grouped into differential structures and the $-G_m$ cells are placed in close proximity of the oscillator nodes. SpectreRF simulations indicate that, for a given power dissipation, inductor Q, and frequency of oscillation, the proposed oscillator achieves twice the voltage swings and 12 dB lower phase noise than that in [2].

Each differential port of the VCO is buffered by an inductively-loaded differential pair. These buffers (1) isolate the VCO from the long interconnects going to the PDs that would otherwise introduce greater uncertainty in the oscillation frequency; (2) generate voltage swings above the supply voltage, driving the flipflops efficiently; and (3) isolate the VCO from the data edges coupled through the phase detectors.

The PD employs eight flipflops to strobe the data at 12.5ps intervals (Fig. 13.7.3). In a manner similar to an Alexander topology [3], the PD compares every two consecutive samples by means of an XOR gate, generating a net output current if the two are unequal, i.e., if an edge has occurred. With no data transitions, the FFs produce equal outputs, and the V/I converters a zero current.

Figure 13.7.4 depicts the master-slave flipflop used in the phase detector. Here, NMOS switches M_1 and M_2 sample D_{in} on the parasitic capacitances at nodes X and Y when CK is high. Since the minimum input common-mode (CM) level is dictated by the gate-source voltage of M_3-M_4 and the headroom required by I_{SS}, the sampling switches experience only an overdrive voltage of 0.5V even if CK reaches V_{DD}, failing to provide fast sampling. This issue is remedied by setting the CM level of CK and $\overline{CK}$ equal to V_{DD}, a choice afforded by the inductively-loaded VCO buffer. The peak value of CK thus exceeds V_{DD} by 0.8V, more than doubling the sampling speed of M_1 and M_2.

With large clock swings available, the current switching in pairs M_5-M_6, M_7-M_8 and M_9-M_{10} is accomplished by gate control rather than conventional source-coupled steering. The proposed topology offers two advantages: (1) since the tail current source is removed, M_{11}-M_{13} can be quite narrower, presenting a smaller capacitance to the VCO buffer; (2) since the drain currents of M_{11}-M_{13} are not limited by a tail current source, these transistors experience "class AB" switching, drawing a large current at the peak of the clock swing and providing greater voltage swings and a higher gain in the data path.

The CDR circuit has been fabricated in a 0.18μm CMOS technology. Figure 13.7.5 shows a photograph of the die, which measures 1.4mm². Figure 13.7.6 depicts the CDR input and output waveforms under locked condition in response to a pseudo-random sequence of length 2^{31}-1. The demultiplexed data experiences some ISI, but if further demultiplexing is included on the same chip, the ISI can be tolerated. The recovered clock, suggesting an rms jitter of 1.756ps and a peak-to-peak jitter of 9.67ps is displayed in Fig. 13.7.7. However, as shown in the inset, the oscilloscope itself suffers from rms and peak-to-peak jitters of 1.508ps and 8.89ps, respectively. Thus, the CDR output contains a jitter of 0.9ps,rms and at most 9.67ps,pp. Preliminary measurements indicate a bit error rate of 10^{-6}, demonstrating correct data recovery and demultiplexing. The overall power consumption excluding the output buffers is 144mW from a 2V supply.

Acknowledgments

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References

[1] J. Kim and B. Kim, "A Low Phase-Noise CMOS LC Oscillator with a Ring Structure," *ISSCC Dig. of Tech. Papers*, pp. 430-431, Feb. 2000.

[2] J. E. Rogers and J. R. Long, "A 10Gb/s CDR/DEMUX with LC Delay Line VCO in 0.18μm CMOS," *ISSCC Dig. of Tech. Papers*, pp. 254-255, Feb. 2002.

[3] J. D. H. Alexander, "Clock Recovery from Random Binary Data," *Electronics Letters*, vol. 11, pp. 541-542, Oct. 1975.

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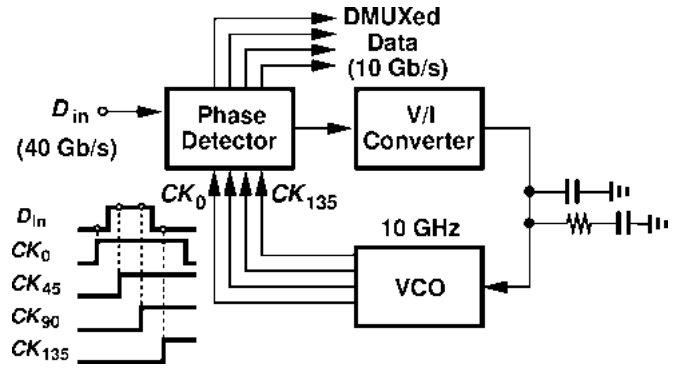

Figure 13.7.1: CDR architecture.

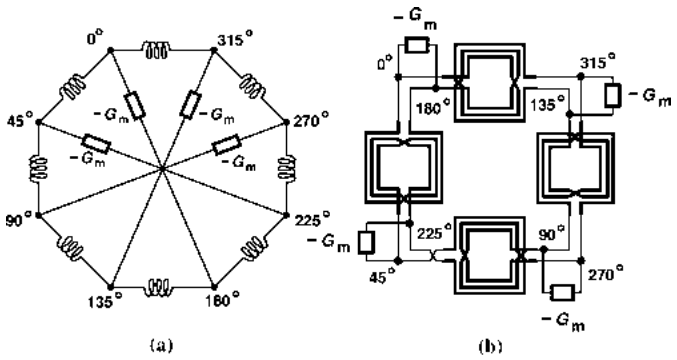

Figure 13.7.2: (a) Multiphase oscillator, (b) modification of (a).

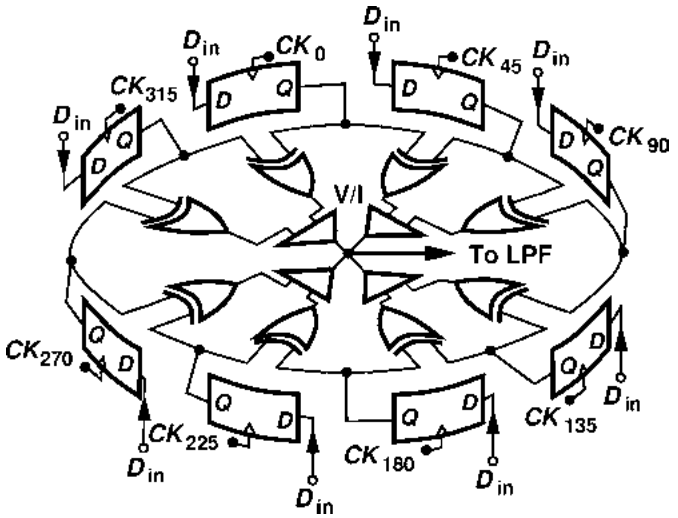

Figure 13.7.3: Quarter-rate phase detector.

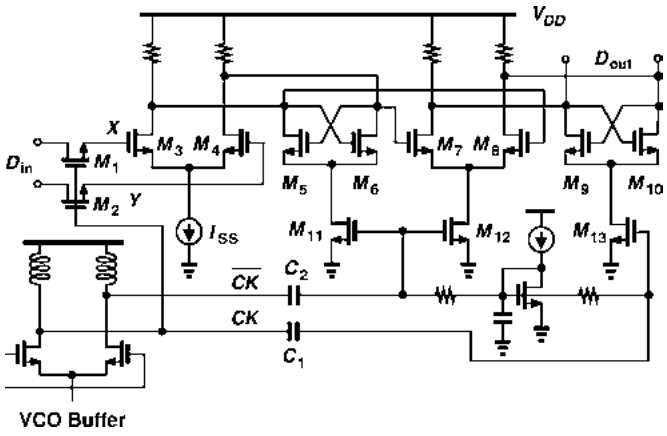

Figure 13.7.4: Proposed flipflop.

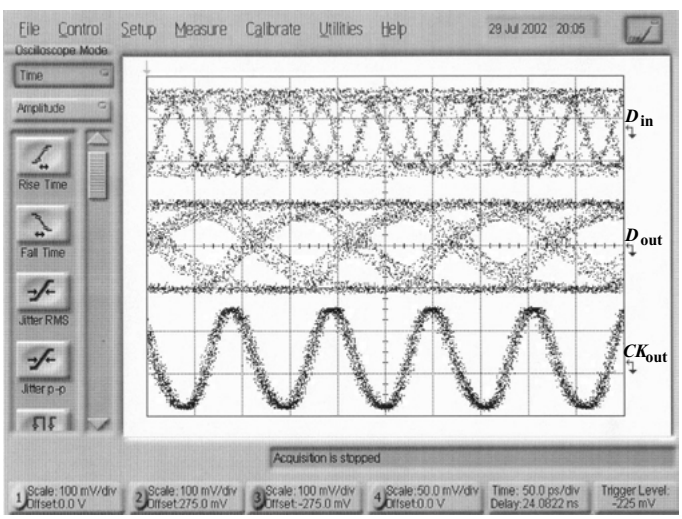

Figure 13.7.6: Input and outputs of CDR circuit (horizontal scale: 50 ps/div., vertical scale 100mV/div.).

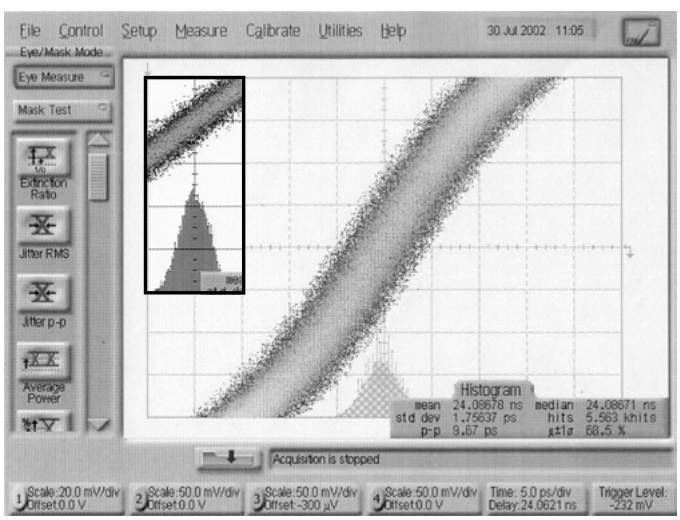

Figure 13.7.7: Measured clock and oscilloscope jitter (horizontal scale: 5ps/div).

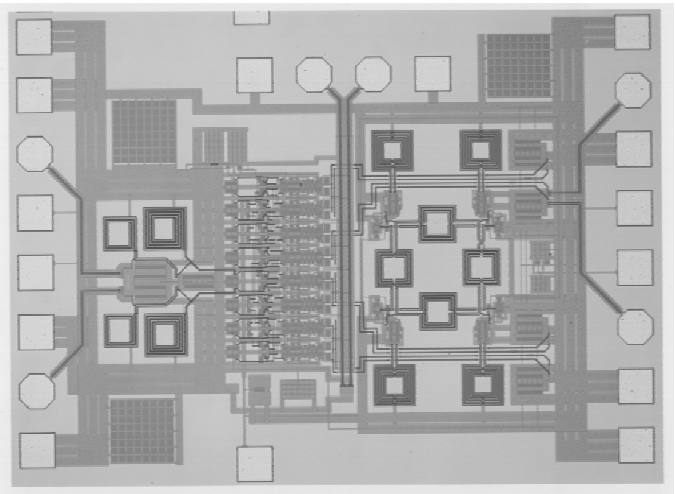

Figure 13.7.5: Chip micrograph.

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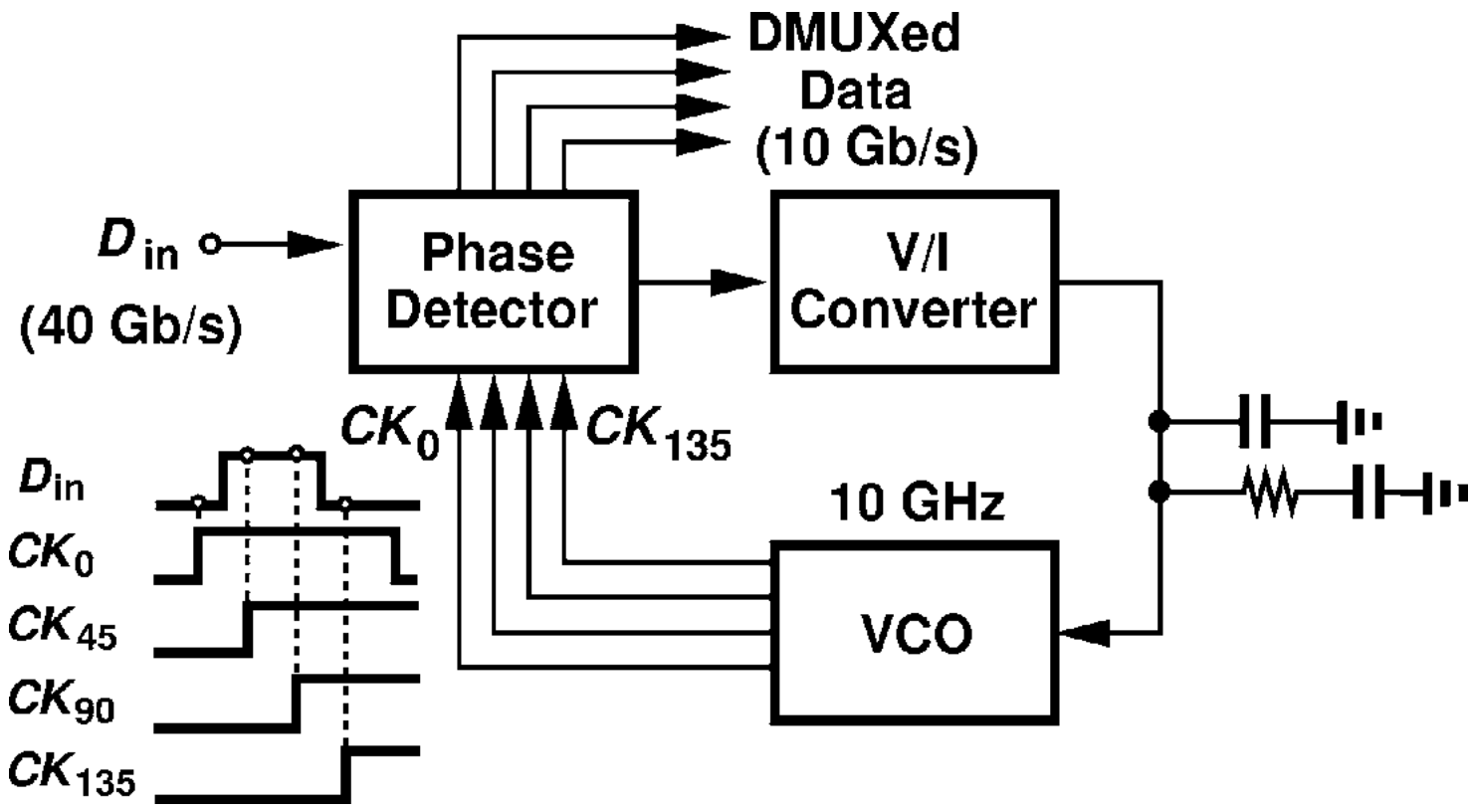

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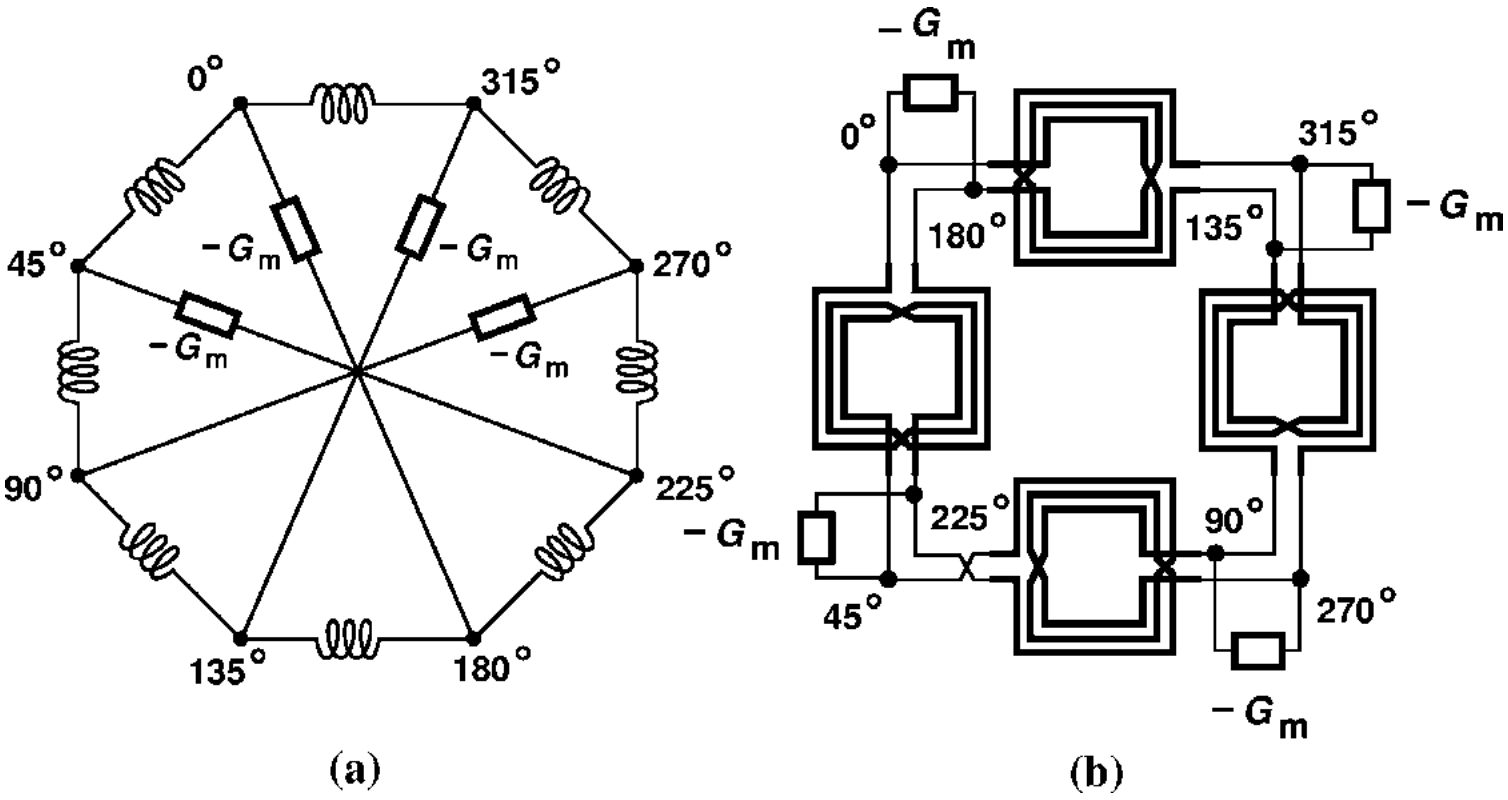

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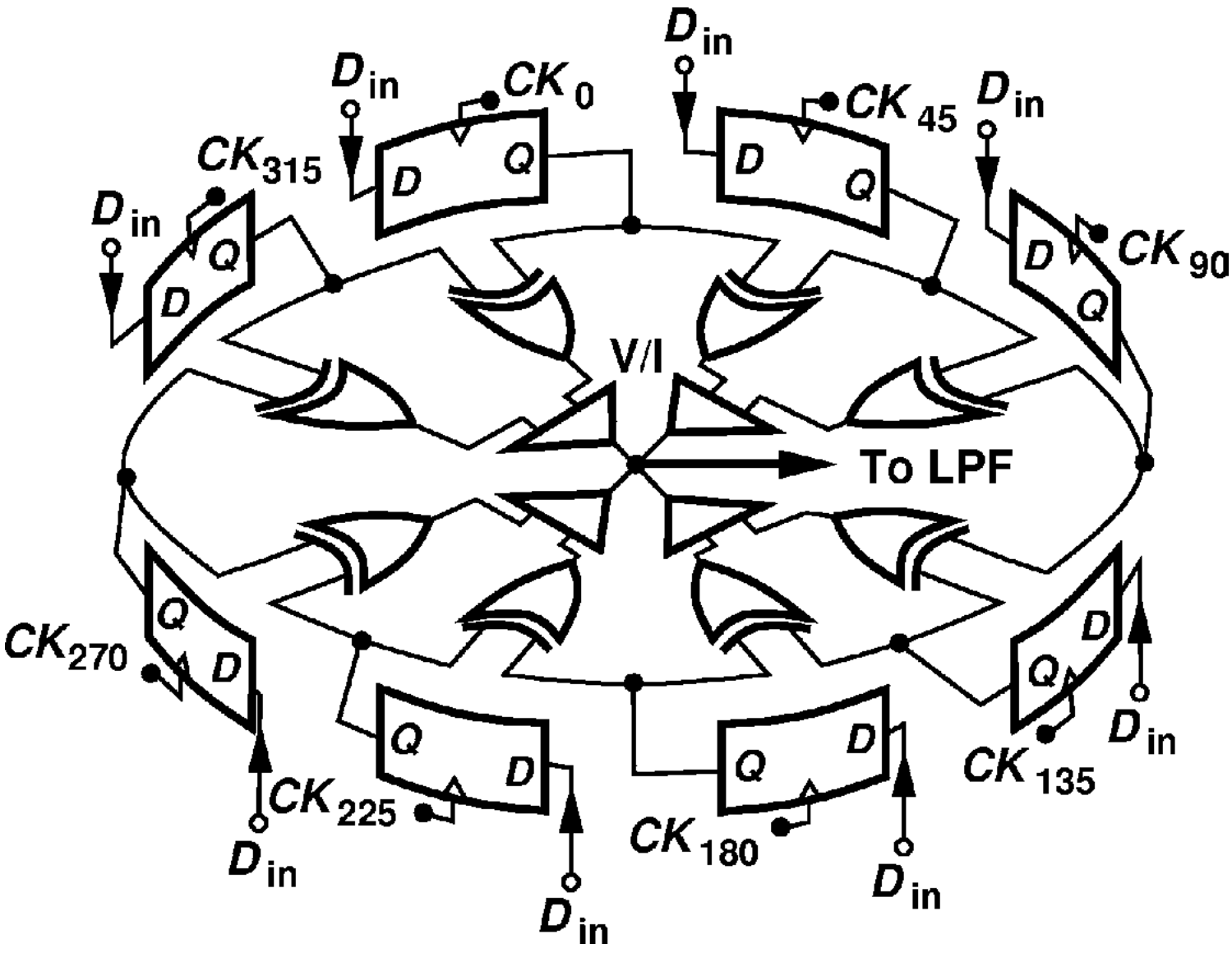

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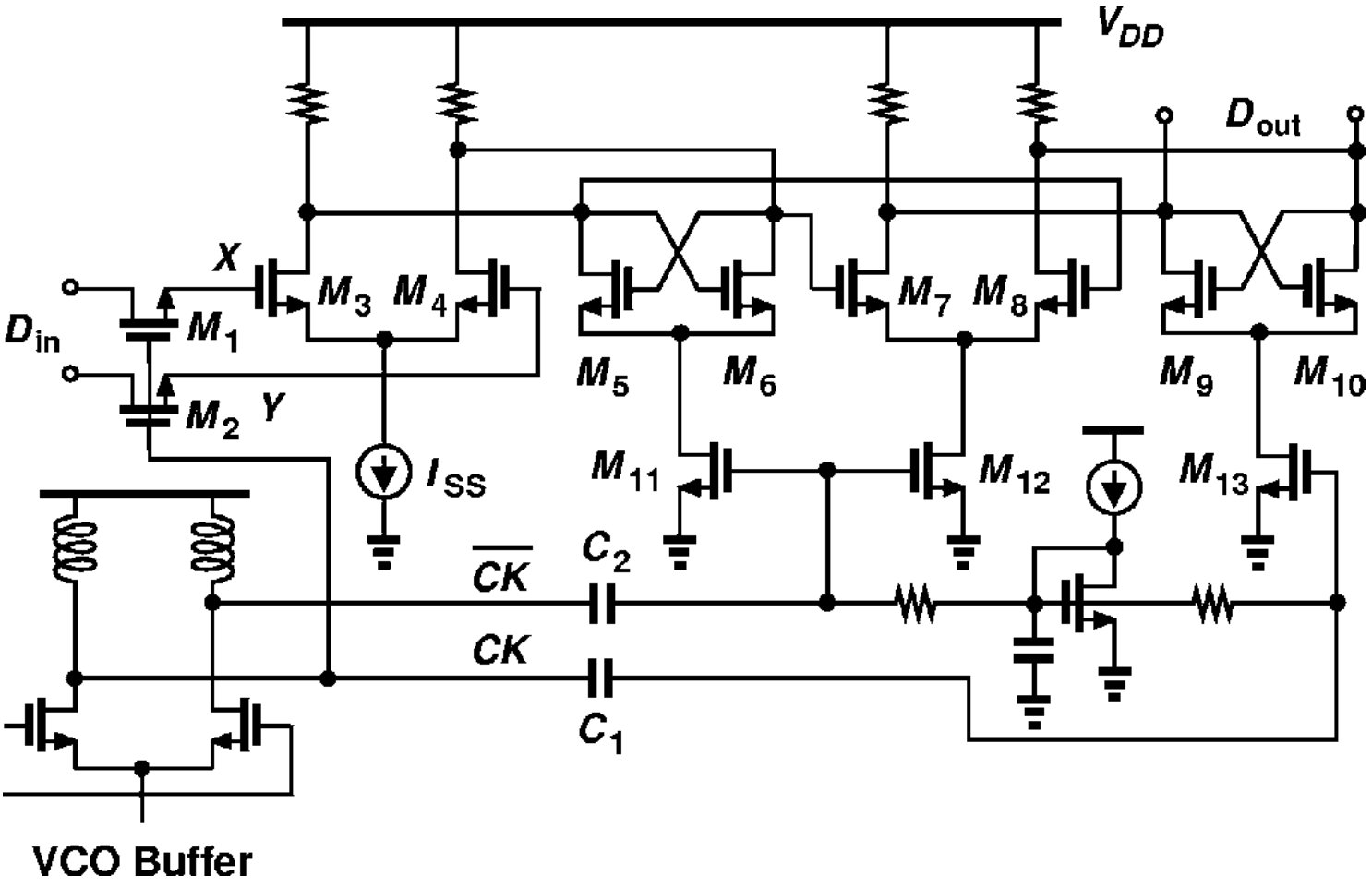

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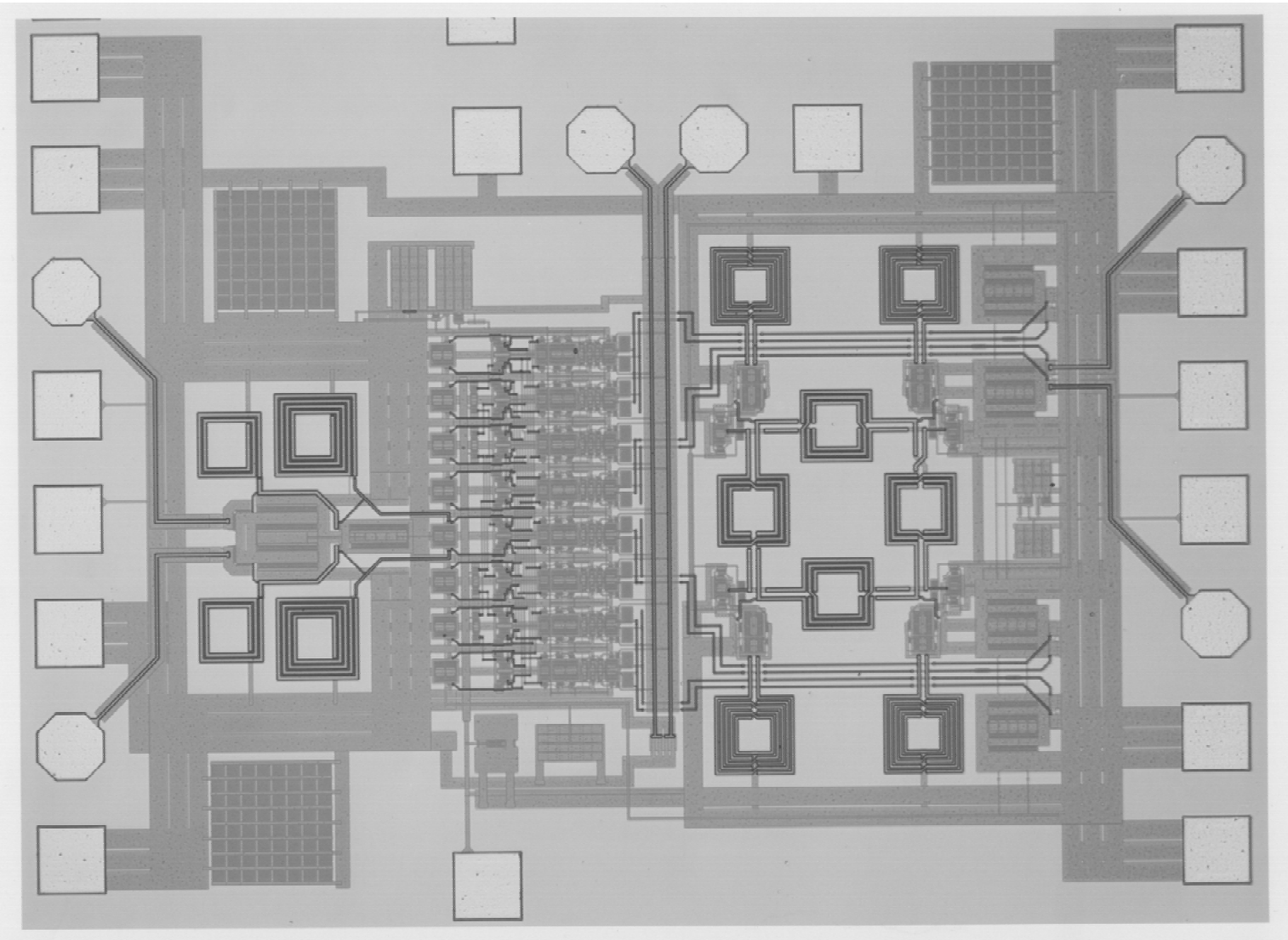

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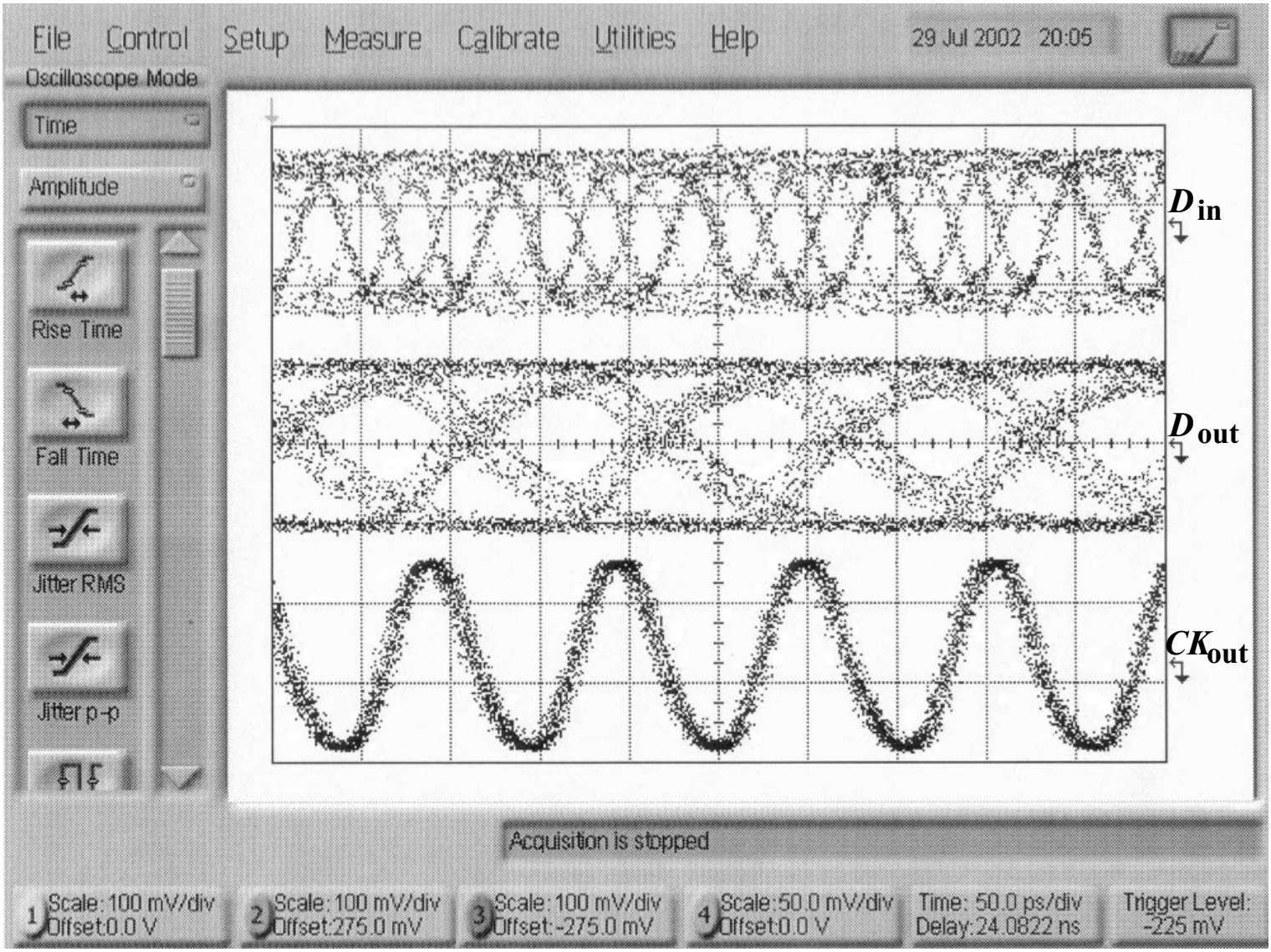

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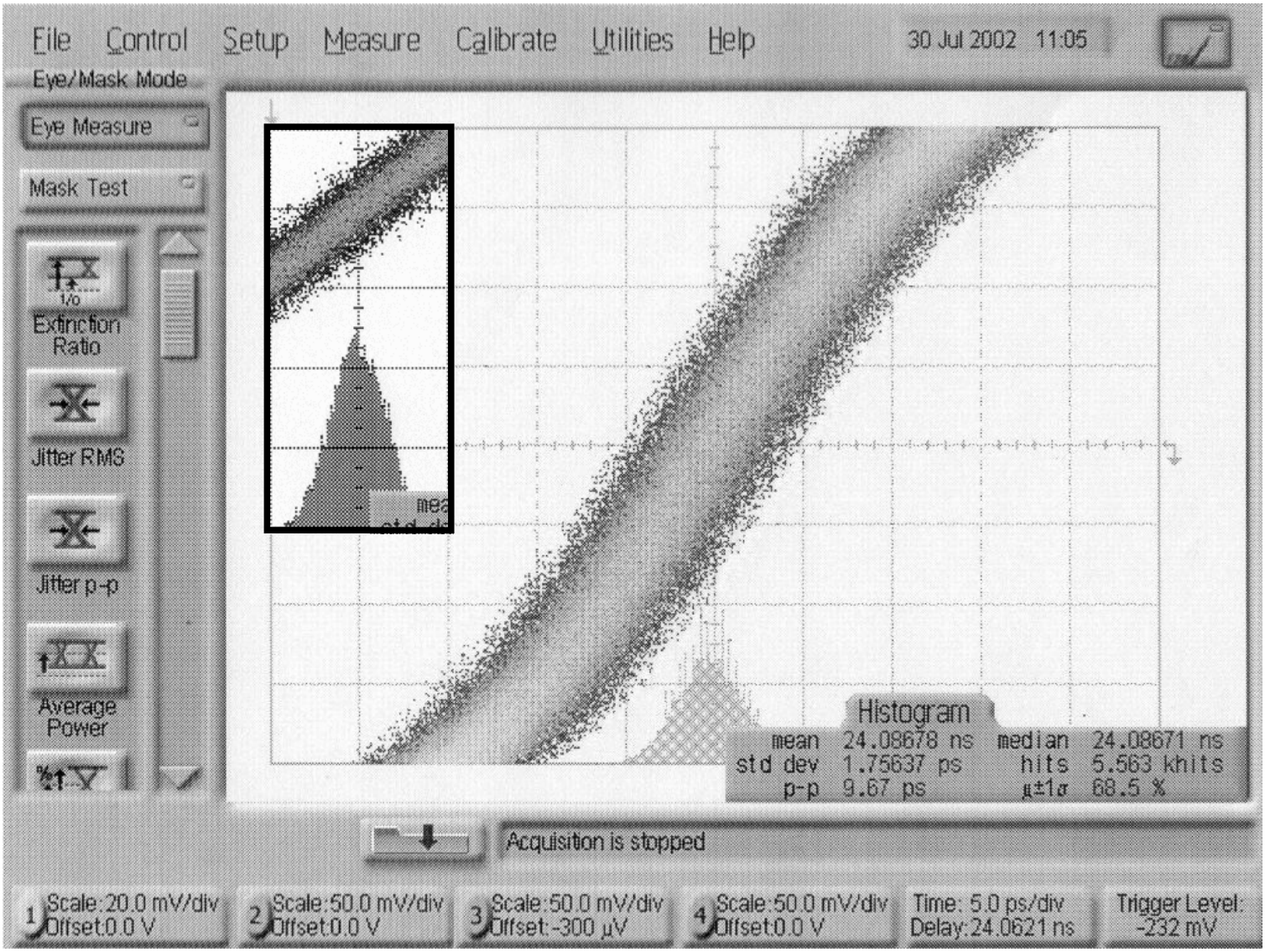

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