8.3 A 40Gb/s TX and RX Chip Set in 65nm CMOS

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Next generation optical and electrical communications such as chip-to-chip serial links or 100GbE require very-high-speed transceivers. At tens of Gb/s, both transmitters and receivers suffer from inadequate bandwidth and high power consumption. One major difficulty arises from the performance degradation of FIR-based FFEs as the FF's *CK-Q* delay becomes significant to one bit period. Using passive components as delay elements [1][2] can relax this issue to some extent, but the untunable delay is quite vulnerable to PVT variations. Traditional DFEs also suffer from speed limitation in its feedback loop, and parallelization schemes usually introduce complex circuits and high power consumption. This paper presents a full-rate 40Gb/s transceiver prototype significantly alleviating the above issues.

Figure 8.3.1 shows the transmitter, which consists of a 20GHz PLL, a 5-tap FFE with tunable delay, and a 1UI delay generator. To create exactly 1-bit delay, conventional FFE approach needs flip-flops, which would either suffer from limited bandwidth or large *CK-Q* delay. Both issues would devastatingly destroy the filter's performance. Even in 65nm CMOS, a flip-flop-based FFE can only operate at 20Gb/s. To increase speed, we propose a 5-tap FFE incorporating delay elements [T_b (=25ps) + remainder Δt], which is made of *LC* networks for each tap, and compensation elements between the nodes of the combiner. In other words, the 40Gb/s input data through the FIR are combined by exactly 25ps separation with different weighting coefficients α_{-2}, α_{-1}, …α_2. The 1UI delay generator is responsible for creating one T_b delay. Each T_b-delay element is actually a voltage-controlled delay line (VCDL) composed of inductors and varactors. By tuning the control voltage (V_{ctrl}), the 1UI delay generator locks the 10GHz input (from the 20GHz PLL and ÷2 circuit) and the delayed version to form a 90° phase difference, forcing T_b delay to be exactly 25ps. As demonstrated in Fig. 8.3.2(b), this "artificial" transmission line provides good matching for broadband and narrowband signals. Distributing V_{ctrl} through the FIR filter, we reproduce the 5-tap 40Gb/s delay line with high accuracy. Note that T_b is immune from PVT variations because of the closed-loop control.

The T_b-delay cell is illustrated in Fig. 8.3.2(a). The differential pair $M_{1\text{-}2}$ propagates input data into an emulated transmission line made of 7 segments of *LC* network. By tuning V_{ctrl} from 0 to 1.2V, the delay from D_{in} to D_{out} varies from 29.7ps to 22.9ps (27.2%). In addition to accuracy, another important advantage of this approach over conventional flip-flop-based delay cell is that most parasitic capacitances are absorbed into the transmission line. By the same token, the 40Gb/s FIR combiner must have resonating elements between taps, or the routing parasitics would degrade the output data considerably. Fig. 8.3.2(b) shows the proposed combiner. Following our layout arrangement, taps are separated by one *LC* element (=Δt). Note that although the 25ps delay is created from the 10GHz clock, the artificial transmission line still provides great consistency for broadband data. The maximum deviation between group delays of 40Gb/s data and 10GHz clock across the whole tuning range is less than 1ps [Fig. 8.3.2(b)].

The receiver is depicted in Fig. 8.3.3. It employs a 3-tap adaptive FIR filter as a front-end equalizer and demultiplexing circuits [3]. A typical DFE suffers from stringent speed requirement in its feedback path, and even though quite a few methods such as sub-rate or loop-unrolled structures have been proposed, they usually involve complicated design and significant power. Here, instead of using a DFE, we place a 3-tap FIR in the RX to overcome the difficulties. Following similar approach as we illustrated in the TX, this adaptive equalizer is capable of providing up to 14dB boosting. Again, driven by an external clock of 40GHz, a 1UI delay generator is responsible for a proper control voltage V_{ctrl}. The 40Gb/s data is therefore sampled by three flip-flops (FF_1, FF_2, and FF_3) and one latch (L_1) with half-rate clock (20GHz), giving rise to three consecutive bits (D_{n-1}, D_n, and D_{n+1}). Note that the operation here is very similar to an Alexander phase detection [4] but with half-rate clock (since only data eyes need to be sampled). Meanwhile, the reference swing generator and the adaptation logic detect the average data swing V_{SW}. For one data bit to be optimally equalized, the eye centers of D_{n-1}, D_n, and D_{n+1} should present a magnitude very close to V_{SW}, otherwise the data is either under or over compensated. Based on this observation, the 3 coefficients α_{-1}, α_0, α_1 can be adjusted accordingly. Here two slicers determine the boosting condition for logic ZERO and ONE. Due to half-rate operation, a 2-to-1 selector picks the corresponding results (E_n) depending on the present bit. After phase alignment, the 4 outputs (D_{n-1}, D_n, D_{n+1}, and E_n) are XORed, 1:8 DEMUXed, and finally sent to the adaptation logic, which is implemented purely in digital domain to save power. Since the overall tail current of the FIR combiner is a constant, the data common-mode level (V_{CM}) must be provided so as to create V_{SW}. Two resistors R_b in Figure 8.3.2(b) (in gray) accomplish this requirement. The averaging length of producing V_{SW} is much longer than the adaptation bandwidth, making the comparing reference very stable.

The adaptation logic is shown in Fig. 8.3.4(a). Since the least-mean-square (LMS) algorithm for eye opening has been realized in the XORs, it takes the majority voting result from the 8×1.25Gb/s inputs to determine the polarity. A 12-bit counter serves as a digital loop filter, in which a 3-bit bandwidth control is included to adjust the convergence speed. The 6-bit MSBs are fed into the iDACs to change the FIR coefficients. As a result, α_{-1}, α_0, and α_1 are tuned in a way that the data ISI is minimized, while 3 iDACs provide current-mode outputs with constant total amount. The voting result for $E_n \oplus D_n$ is to produce present swing information for reference swing generator to create V_{SW} [Fig. 8.3.4(a)]. Here, M_1-M_2 pair is fully tilted, and the third iDAC provides the tail current directly to the reference swing generator. The opamp plus M_3-M_6 loop makes the common-mode level of V_{SW} exactly equal to V_{CM} of the FIR filter. The phase detector in the 1UI delay generator is illustrated in Fig. 8.3.4(b). To lock two 10GHz clocks in quadrature (90° phase difference), we utilize SSB mixer to distill the phase error. That is, for a phase difference θ between two inputs (with magnitudes A_1 and A_2), the output is given by $k_1A_1A_2\cos\theta$, where k_1 denotes the mixer gain. The sinusoidal characteristic forces the phase to lock at $\pi/2$ with an approximately liner behavior in the vicinity. Note that non-idealities (such as second-order harmonic caused by mismatch) are easily suppressed by the *RC* network on the output port.

The transceiver is fabricated in a 65nm CMOS technology. The transmitter consumes 135mW from a 1.2V supply, of which 29mW dissipates in 20GHz PLL (TX side), 77mW in 5-taps FIR, 29mW in 1UI delay generator. The receiver consumes 322mW from a 1.6V supply. To evaluate the performance, the TX and RX are mounted on a Rogers board (RO4003) with different channel lengths. The 20GHz PLL presents an operation range of 20GHz (19.4-21GHz), suggesting the TX output data rate can be tuned from 38.8-42Gb/s. The transmitter's outputs with 0dB and 9.5dB pre-emphasis are illustrated in Fig. 8.3.5(a) and (b). Shown in Fig. 8.3.5(c) is the spectrum of the 20GHz PLL in TX under locked condition. The phase noise measures –91.57dBc/Hz at 1MHz offset, and the integrated jitter (from 10Hz to 6.5GHz) is given by 0.5766ps,rms. For the RX, the equalized data (40Gb/s) for different channel lengths (5cm and 20cm) are depicted in Fig. 8.3.6(a). Figure 8.3.6(b) illustrates the demuxed data (10Gb/s) for a 10cm channel. The BER testing has been conducted as well. For 40Gb/s PRBS of 2^{31}–1, the transceiver achieves BER of less than 10^{-12} until channel length =17.5cm, which has 18dB loss at 20GHz. For 20cm channel (19dB loss at 20GHz), BER begins to increase as the data pattern becomes longer [Fig. 8.3.6(c)]. Figure 8.3.7 shows the die photographs, which occupy 0.9×0.7mm^2 for TX and 1.1×0.6mm^2 for RX, respectively. A table summarizing the performance of this work is also included in Fig. 8.3.7.

Acknowledgment:
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References:

[1] H. Wu, J. Tierno, P. Pepeljugoski, et al., "Differential 4-tap and 7-tap Transverse Filters in SiGe for 10Gb/s Multimode Fiber Optic Link Equalization," *ISSCC Dig. Tech. Papers*, pp. 180-181, Feb., 2003.

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[3] H. Sugita, K. Sunaga, K. Yamaguchi, and M. Misuno, "A 16Gb/s 1st-Tap FFE and 3-Tap DFE in 90nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 162-163, Feb., 2010.

[4] J.D.H. Alexander, "Clock Recovery from Random Binary Data," *Electronics Letters*, vol. 11, no. 22, pp. 541-542, Oct., 1975.

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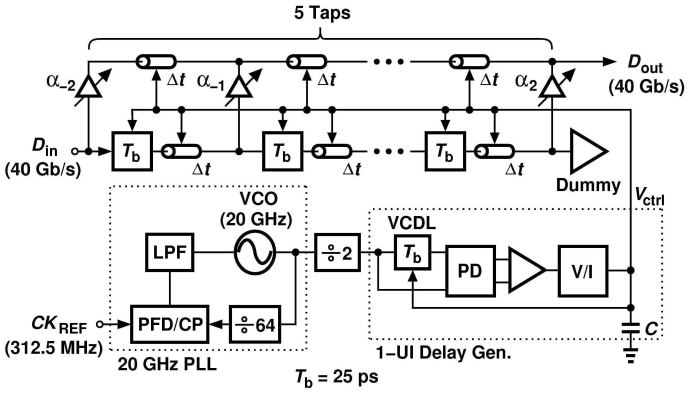


Figure 8.3.1: Transmitter architecture.

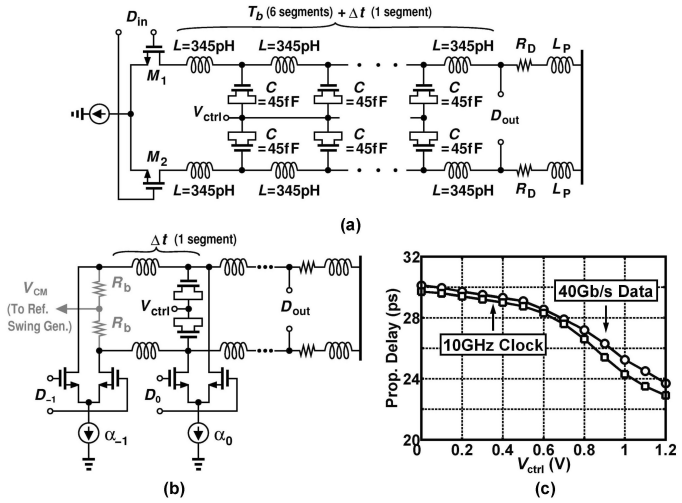


Figure 8.3.2: (a) Voltage-controlled delay line (T_b), (b) Simplified FIR combiner and delay (gray part for RX FIR only), (c) Propagation delay for 40Gb/s data and 10GHz clock.

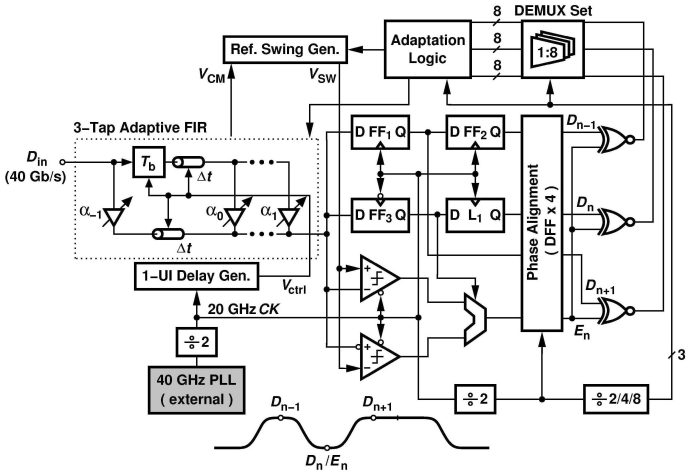


Figure 8.3.3: Receiver with adaptive FIR equalizer.

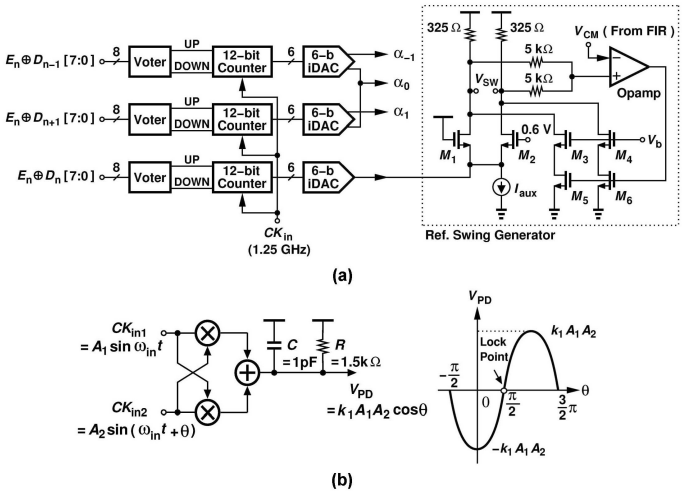


Figure 8.3.4: (a) FIR adaptation circuits, (b) Mixer-based PD.

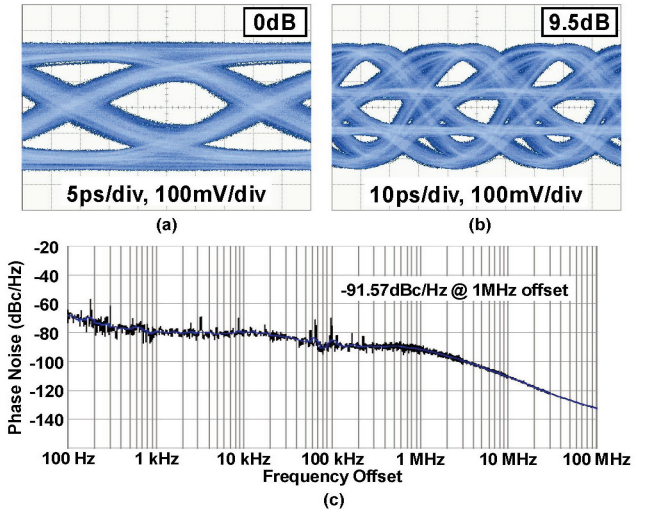


Figure 8.3.5: With (a) 0dB, (b) 9.5dB pre-emphasis, (c) Phase-noise plot of 20GHz PLL.

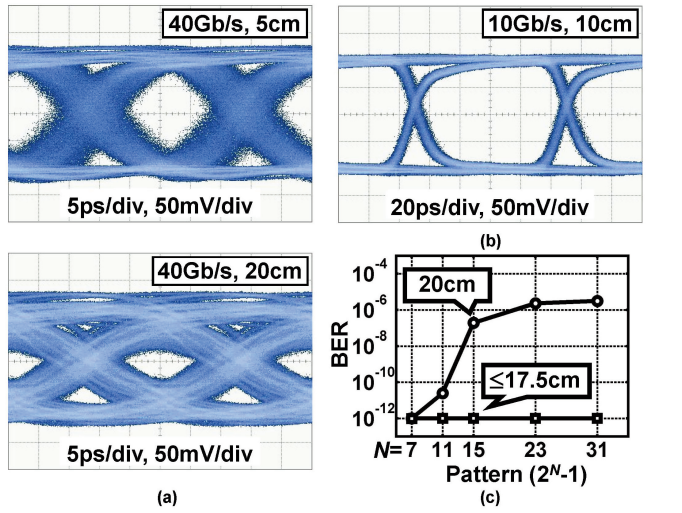
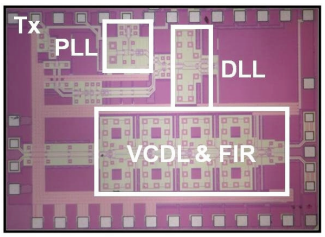
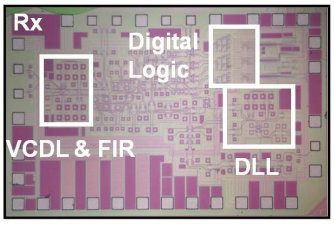


Figure 8.3.6: (a) Equalized 40Gb/s data in RX for 5cm and 20cm channel, (b) Demuxed 10Gb/s data, (c) BER for different channel lengths.





Data Rate	40Gb/s (38.8~42Gb/s)
Architecture	5-Tap FIR (Tx) 3-Tap FIR (Rx)
BER	$< 10^{-12}$, $2^{31}-1$ PRBS for ≤ 17.5cm channel (18-dB Loss @ 20GHz)
	$< 10^{-12}$, $2^{7}-1$ PRBS for 20cm channel (19-dB Loss @ 20GHz)
Output Data Jitter (10Gb/s)	10cm channel: 1.72ps,rms 11.56ps,pp
	20cm channel: 3.88ps,rms 20.44ps,pp
Power	Tx: 135mW, Rx: 322mW
Supply	Tx: 1.2V, Rx: 1.6V*
Chip Area	Tx: 0.9 x 0.7mm^2 Rx: 1.1 x 0.6mm^2
Technology	65nm CMOS

* 1.2V used in Digital Logic

Figure 8.3.7: Chip micrograph and performance summary.

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