6.1 A 56Gb/s PAM-4/NRZ Transceiver in 40nm CMOS

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Ultra-high speed data links such as 400GbE continuously push transceivers to achieve better performance and lower power consumption. This paper presents a highly parallelized TRX at 56Gb/s with integrated serializer/deserializer, FFE/CTLE/DFE, CDR, and eye-monitoring circuits. It achieves BER<10^{-12} under 24dB loss at 14GHz while dissipating 602mW of power.

Figure 6.1.1(a) illustrates the TX structure, which consists of a 64:4 serializer, a 3-tap quarter-rate FFE, a poly-phase filter (PPF) generating quadrature clocks for the latches and selectors, and a combiner (output driver). The low-speed 64:4 serializer can be done in typical CMOS (digital) realization. The 4×14Gb/s inputs coming from it are fed into the quarter-rate FFE, which provides maximum boost of approximately 8dB at 14GHz (Nyquist frequency). Owing to the quarter-rate operation, most of the circuits are realized in CMOS (digital) format, saving significant power. A standalone 14GHz PLL incorporating a mixer-based PFD [1] to minimize jitter and spurs has been included, which is shared with the RX. The TX can be operated with the 14GHz clock either from the PLL or from outside. Sub-rate TXs are prone to output eye distortion, simply because of the imbalanced loading and routing. To overcome this issue, a duty cycle correction (DCC) unit is employed along the clock path. It provides a maximum tunable range of 40%~60%, well beyond any possible eye distortion. The DCC not only corrects the duty cycle, but also converts the CML clock to CMOS levels (i.e., rail-to-rail). The PAM-4 signal combiner is depicted in Fig. 6.1.1(b), where inductors are inserted between the differential pairs and the tail currents. The arrangement increases the high-frequency output impedance seen looking down to the current sources, maintaining relatively constant currents when the differential pairs are switching. As a result, the TX produces less ringing during transitions between levels, and the more eye opening can be achieved. Note that the pre-cursor and post-cursor paths employ a cascode structure, improving isolation between taps. The PAM-4 TX can deliver 28Gb/s NRZ data as well by shutting down half of the circuit (e.g., LSB path and Combiner 1).

The PAM-4 RX is shown in Fig. 6.1.2. Here, the input data is first linearly equalized and amplified by CTLE and VGA, respectively, arriving at a constant signal swing before going into the DFE summers. Both CTLE and VGA are programmable and are governed by system control logic. The CTLE includes 2 stages of RC-degenerated pairs and 1 stage of low frequency equalization [2], providing a maximum of 9dB of boost from 100MHz to 14GHz. The VGA has a tunable range of 8dB. After amplification by the VGA, the incoming PAM-4 signal is divided into two paths, odd and even, with six slicers in each. The data slicers triggered by CK_D convert the PAM-4 signals into three thermometer codes, and the edge slicer samples the edge by CK_E. After being parallelized by the subsequent 1:16 DMUXes, the results are sent to the CDR for phase adjustment. The all-digital CDR consists of parallel bang-bang PDs, determining whether the clock phase is leading or lagging by means of majority voting. Two 7b decoders regulate the phase interpolators (PIs), delivering proper clock phases to the DMUXes and slicers. The demultiplexed thermometer codes are transformed to NRZ by the digital PAM-4 decoders. Note that owing to the low-speed, fully digital operation of CDR, undesired zero-crossing points of the transitions between PAM-4 signal levels are removed in digital domain. Thus, issue of multiple edge points does not exist in the phase tracking of the CDR. Meanwhile, a half-rate DFE with 3 taps is adopted to further provide high-frequency compensation and waveform reshaping. The 14GHz clock can come either from off-chip or the standalone PLL (shared with TX). Finally, an eye-opening monitoring circuit is also incorporated here, which presents real-time on-chip eye monitoring and waveform reconstruction. The control unit takes orders from and sends results to an external FPGA, which connects to a PC for further processing. The PAM-4 RX is fully compatible with the NRZ data format and can process 28Gb/s NRZ data.

The half-rate DFE is shown in Fig. 6.1.3. It is well known that a DFE for a PAM-4 signal requires 3 times more hardware (e.g., flipflops) than for NRZ signal, since we are dealing with thermometer codes. The parallelized architecture helps to minimize power, as no 28Gb/s flipflop is required. Each tap has 3 feedbacks with identical coefficients $-\alpha_1$, $-\alpha_2$, $-\alpha_3$, alternately applied to the summers. To make the DFE adaptive, we need to dynamically track the power level of the PAM-4 signal before the slicer, y(t). Here, the reference generator creates 4 signal levels (V_{ref1}~V_{ref4}, representing 00, 01, 10, and 11) and 3 threshold levels (V_{TH1}~V_{TH3}). The differences between adjacent levels are equal. It operates as follows. The common-mode level of y(t) is first lined up with V_{TH2} by the common-mode feedback. Next, the reference adjuster stretches or squeezes the reference and threshold levels until V_{ref1}–V_{ref4} matches the average peak-to-peak swing. Finally, the sign-sign LMS engine is turned on to optimize DFE coefficients.

The PAM-4 signal can be monitored in real time to achieve the lowest BER. Figure 6.1.4 illustrates the conceptual operation. Suppose the CDR provides a clock phase CK_{data} for data sampling, which is obtained from the above phase detection. Obviously, CK_{data} falls in the nominal center of the data eyes. Now, a variable clock CK_ϕ is created by introducing a tunable delay, ΔT, to check eye openings at different positions, and a variable threshold level V_{TH} is added in the front-end. As a result, it forms a 2-D eye-opening monitor. The three black boxes (■) represent the sampling results from the nominal eye centers, and the white box (□) stands for the checking point. If a certain checking point is error free, its result must be coincident with one of the black boxes. In other words, one XOR gate would always produce logic low whereas the other two must have logic high. For a given testing length, it can be determined whether this checking point is inside the opening area and which eye it belongs to. By sweeping V_{TH} and CK_ϕ we obtain a complete 2-D eye-opening map with a resolution of 64×64 points ("pixels"). Similar to the TX, the RX can actually be operated in NRZ mode by shutting down the upper and lower paths in the DFE. In that case, only two levels are dealt with, saving 47mW of power. The power consumption can be further reduced in low-loss environments, where only 1-tap DFE is needed. Turning off 2 taps corresponds to 32mW of power saving.

The TRX is fabricated in 40nm CMOS technology and tested in chip-on-board assembly. Due to the limited available area, the TRX is taken apart as three separate circuits, i.e., TX, RX, and PLL, which can be assembled as one complete piece with no difficulty. Figure 6.1.5(a) demonstrates the PAM-4 output waveform at 56Gb/s captured by using the internal 2^7–1 PRBS generator. The 14GHz PLL phase noise is plotted in Fig. 6.1.5(b), indicating –98dBc/Hz at 1MHz offset. The integrated rms jitter (from 100Hz to 1GHz) is 688fs. Figure 6.1.5(c) illustrates the measured coefficients of the DFE for different channel losses at 14GHz under 56Gb/s operation. Here, the CTLE boost is set to 9dB and the coefficient settling time is less than 5μs. The RX can deal with NRZ data at 28Gb/s as well. Figure 6.1.5(d) shows the sinusoidal jitter tolerance under such a condition, exceeding the CEI-56G-VSR mask by at least 0.19UI_{PP}. Figure 6.1.6(a) and (b) reveal the reconstructed eyes under 24dB channel loss for 56Gb/s PAM-4 and 28Gb/s NRZ, suggesting an error-free area of 0.26UI×40mV and 0.5UI×110mV, respectively. Clock phase offset has been recorded in Fig. 6.1.6(c). Here, the nominal clock phase is fixed as reference, and the sampling clock phase shifts around the reference. The tolerance ranges of 56Gb/s PAM-4 and 28Gb/s NRZ data are 0.25UI and 0.35UI, respectively. The overall BER test for the whole TRX is shown in Fig. 6.1.6(d). Here, we setup a back-to-back link where the TX delivers a 56Gb/s PAM-4 signal to the RX through a lossy channel. It achieves BER<10^{-12} for any Nyquist channel loss less than 24dB. Figure 6.1.7 depicts the die photographs. The three blocks occupy areas of 0.52×0.48mm^2 (PLL), 1×0.8mm^2 (TX), and 1.4×0.9mm^2 (RX). Performance of this work with the state of the art is summarized in Fig. 6.1.7.

Acknowledgment:
The authors thank TSMC for chip fabrication.

References:

[1] Jri Lee, "A 75-GHz PLL in 90-nm CMOS technology," *ISSCC*, pp. 432-433, Feb. 2007.
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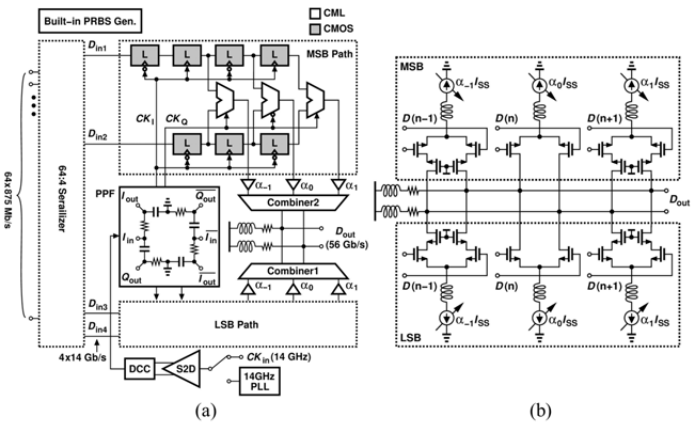


Figure 6.1.1: (a) TX architecture, (b) combiner/driver.

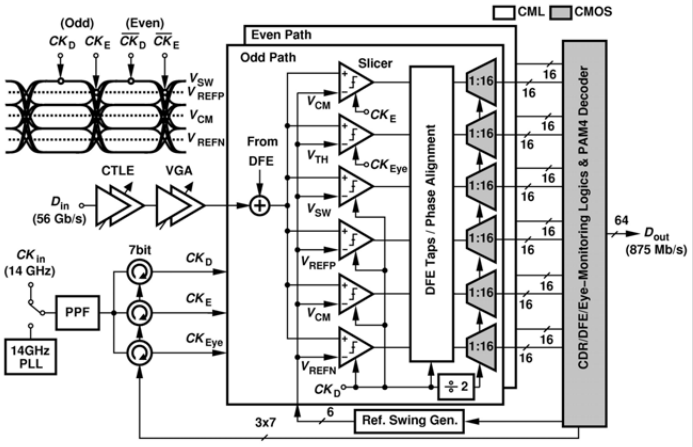


Figure 6.1.2: PAM-4 RX architecture.

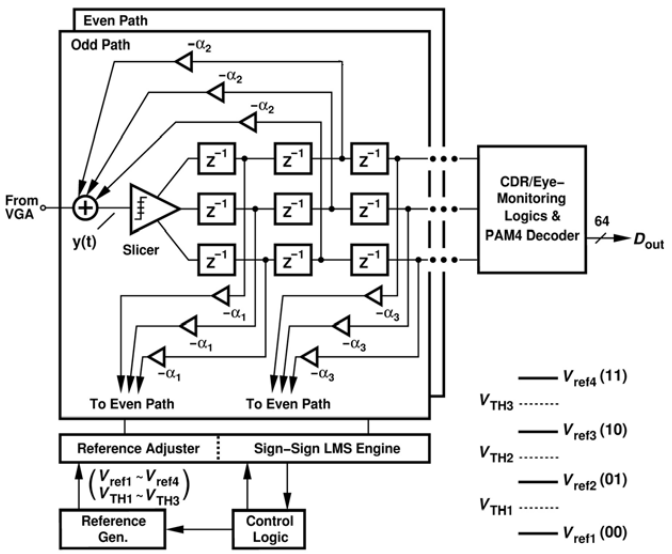


Figure 6.1.3: Half-rate DFE.

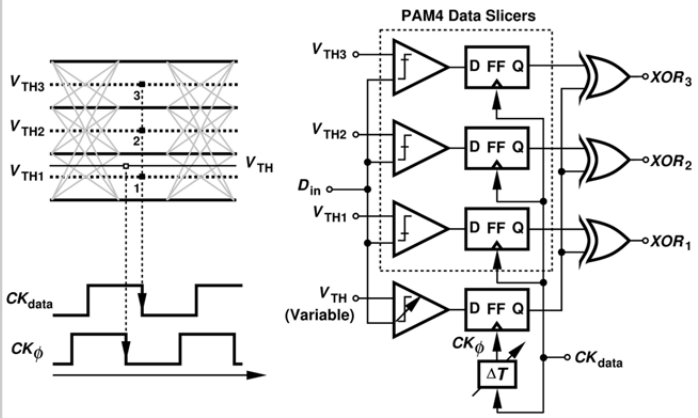


Figure 6.1.4: Simplified eye-monitoring circuit.

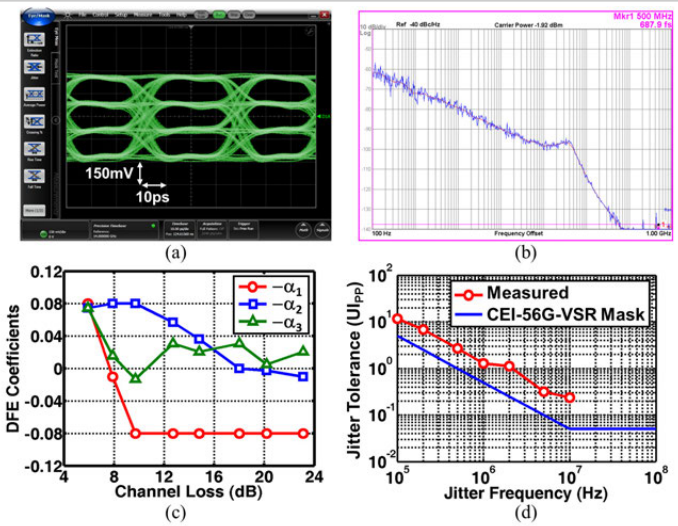


Figure 6.1.5: (a) PAM-4 TX output at 56Gb/s, (b) PLL phase noise plot at 14GHz, (c) DFE coefficients as a function of channel loss, (d) jitter tolerance.

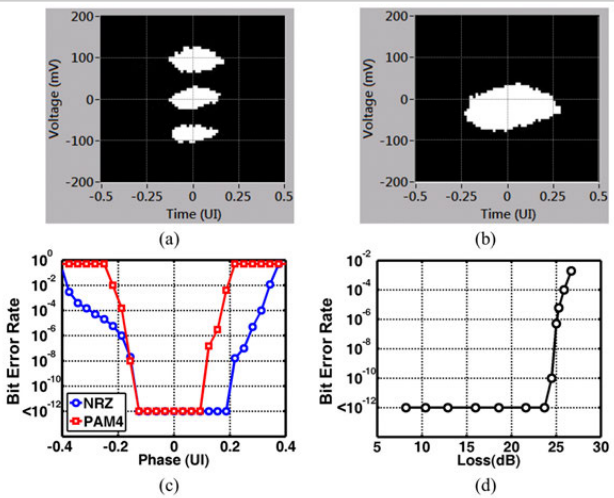
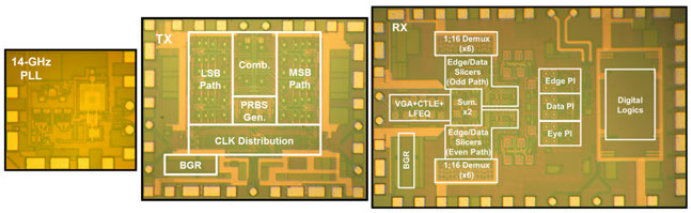


Figure 6.1.6: Eye monitoring results for (a) 56Gb/s PAM-4, (b) 28Gb/s NRZ. (c) Bathtub measurement of clock phase offset, (d) overall BER for different channel loss (TX+RX).



	14-GHz PLL
Supply	1V
Operation Frequency	12.8~14.3GHz
Phase Noise	-98dBc/Hz @1MHz
RMS Integrated Jitter	688fs (100Hz~1GHz)
Output Power	0 dBm
Power Consumption	20mW
Chip Area	0.25mm²
Technology	40nm CMOS

PAM4 TX	[3]	This Work
Supply	1V	1V/1.5V
Function	2:1 Serializer +4-tap FFE	4:1 Serializer +3-tap FFE
Driver Topology	SST	CML
Data Rate	45Gb/s	56Gb/s
Internal PRBS Generator?	No	Yes
Power Consumption	120mW	200mW
mW/Gbs	2.66	3.57
Chip Area	0.28mm²	1.14mm²
Technology	28nm FDSOI	40nm CMOS

RX	[4]	[5]	This Work
Supply	1.2V	0.96V	1V
Data format	PAM4	NRZ	PAM4
Function	CDR, CTLE, 1:2 DMUX	CTLE, 1-tap DFE, CDR, 4:32 DMUX, Eye monitoring, DFE Adaptation	CTLE, 3-tap DFE, CDR, 1:64 DMUX, Eye monitoring, DFE Adaptation
Data Rate	54.1~56.8Gb/s	56.2Gb/s	56Gb/s
Adaptive Threshold?	No	N/A	Yes
Channel Loss @ BER<10^{-12}	N/A	18.4dB @28.1GHz	24dB @14GHz
Power Consumption	420mW	142mW	382mW
Chip Area	1.6mm²	1.4mm²	1.26mm²
Technology	40nm CMOS	28nm CMOS	40nm CMOS

Figure 6.1.7: Die photos and performance summary.

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