A 60-GHz FSK Transceiver with Automatically-Calibrated Demodulator in 90-nm CMOS

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Abstract

A fully-integrated 60-GHz transceiver utilizing analog FSK modulation/demodulation to replace baseband processor has been demonstrated. Employing a discriminator with automatic adjustment and a folded dipole antenna pair (5-dBi gain for each), the transceiver achieves > 1Gb/s data transmission over 1 meter with BER < 10^{-12} while consuming a total power of 500 mW.

I. Introduction

As non-coherent structures prove sufficient for simple wireless data transmission, modulations such as ASK [1] have been used in low-cost low-power 60-GHz transceiver targeting short distance applications. This paper presents a fully-integrated transceiver that incorporates analog FSK modem to avoid carrier recovery and baseband circuitry.

II. Transceiver Architecture

The transceiver architecture is illustrated in Fig. 1. In this prototype, we choose 62.5/57.5GHz as the modulation frequencies, which can be easily modified to fit in with other standards. The transmitter comprises an FSK modulator, a mixer, and a PA. The FSK modulation is accomplished by the 20- and 2.5-GHz clocks, obtained from the 40-GHz frequency synthesizer. The 22.5/17.5GHz IF signal is up-converted to 60-GHz band by means of a mixer, and the PA delivers the RF signal to antenna. The receiver consists of an LNA, a mixer, an IF amplifier, and an FSK demodulator. The input signal from antenna is amplified by the LNA and down-converted to 22.5/17.5GHz. FSK demodulation is achieved by an adaptive frequency discriminator which distills the data output purely in analog domain.

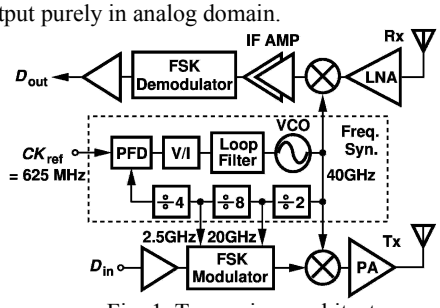

Fig. 1. Transceiver architecture.

III. Building Blocks

Figure 2 depicts the FSK modulator design, which combines two SSB mixers made of CML structures with different loading inductance resonating at 17.5 and 22.5 GHz, respectively. A 2-to-1 selector picks one IF signal based on D_{in} and sends it to the up-conversion mixer. The rail-to-rail input data switches M_5-M_6 and M_7-M_{10} not only speed up the operation but minimize undesired sidebands. The sideband rejection of this pseudo-nMOS topology is superior to that of conventional CML by 10dB. The PA employs similar design as [1].

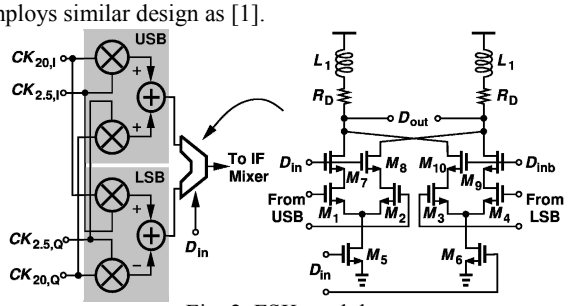

Fig. 2. FSK modulator.

The 40-GHz frequency synthesizer consists of a full-rate *LC* tank VCO, a 40-GHz static divider with inductive peaking and class-AB biasing, a third-order on-chip loop filter, and a linear mixer-based PFD proposed in [2].

The LNA is implemented as a 4-stage topology with matching networks. Fig. 3(a) shows one stage of it. To minimize the internal parasitic capacitance at node *P*, active devices are carefully laid out with round-table and shared-junction techniques [3]. To avoid any possible feedback through V_{DD}, power lines of different stages are not shorted locally, but rather are connected to the global power line with heavy bypass. Multi-pole-filters (MPFs) made of C_1-R_1-C_2-R_2-C_3 network are used to suppress both low- and high-frequency feedbacks [4]. Simulation shows that the *K* factor is higher than 7 for all frequencies of interest.

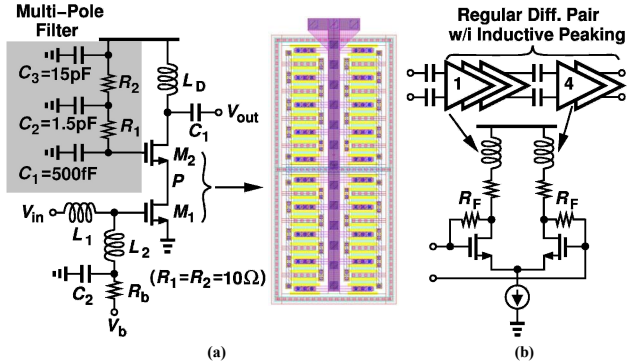

Fig. 3. (a) One LNA stage, (b) IF amplifier.

As shown in Fig. 3(b), the IF amplifier employs five stages of differential pairs with inductive peaking in cascade. The resonance frequencies of different stages are staggered to cover a wider operation range. The 1st and 4th stages comprise local shunt-shunt feedback R_F, allowing ac coupling between stages to suppress offset. The IF amplifier presents a peak gain of 30 dB, and a 3-dB bandwidth of 12 GHz (14~26GHz).

Figure 4 shows the demodulator, where the C_1-*L*-C_2 network forms a frequency discriminator [5]. It can be shown that the ratio of V_2 and V_1 is given by

$$\frac{V_2}{V_1}=\frac{R_p LC_1 s^2}{R_p L(C_1+C_2)s^2+sL+R_p},$$

where R_p denotes the inductor loss (R_p=$Q \cdot \omega L$). The phase of (V_2/V_1) can be derived as

$$\angle\left(\frac{V_2}{V_1}\right)=\begin{cases}180^\circ-\tan^{-1}\dfrac{1}{Q\left(1-\omega^2/\omega_0^2\right)}, & \text{for } 0<\omega<\omega_0\\ \tan^{-1}\dfrac{1}{Q\left(\omega^2/\omega_0^2-1\right)}, & \text{for } \omega_0<\omega<\infty\end{cases}$$

where ω_0= $[L(C_1+C_2)]^{-1/2}$. That is, the two modulation frequencies ω_1 and ω_2 can be distinguished by examining the phase relationship between V_1 and V_2. Note that the maximum SNR occurs when the two phase differences at ω_1 (= 2π×17.5 GHz) and ω_2 (= 2π×22.5 GHz) are symmetric with respect to 90°, which corresponds to $[L(C_1+C_2)]^{-1/2}$ = 2π×20.156 GHz. For Q = 5 and Q = 10, the phase of V_1 and V_2 can be separated by 100° and 136°, respectively, which are large enough for us to obtain the data directly by mixing the two signals. However, in conventional approaches such as [5], the central frequency $[L(C_1+C_2)]^{-1/2}$ would drift over process and temperature variations, degrading performance significantly. Simulation suggests that the output

data swing would be reduced by 50% if L or C_1 deviates by only 8%.

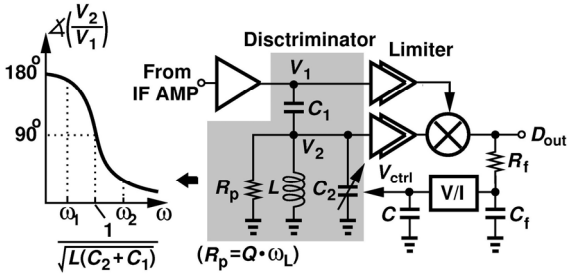

Fig. 4. FSK demodulator.

To overcome the difficulty, a feedback loop is used to dynamically maximize the phase difference (and therefore the output swing). Here, the R_F-C_F network produces the output average (dc) level. Nominally equal to zero, this value is applied to a V/I converter, which injects a positive or negative current into the filter C and adjusts the control voltage V_{ctrl} accordingly. As a result, C_2 (realized as a varactor) is thus changed until ω_1 and ω_2 locate almost evenly at the left- and right-hand sides of $[L(C_1+C_2)]^{-1/2}$. In other words, the loop optimizes the output power and therefore the SNR. Note that the magnitude of (V_2/V_1) varies with frequency. To rule out this effect, V_1 and V_2 must be buffered by limiters before feeding into the mixer. Made of differential pairs with inductive peaking, the limiters provide 11-dB gain and saturate the signals to full CML level (400mV) while introducing negligible phase error. The feedback loop is unconditionally stable. Here, C=60pF is chosen to arrive at a control line ripple less than 10 mV and a power-up tracking time on the order of 2μs. Note that finite frequency offset between Tx and Rx can always be tolerated in such a non-coherent demodulation.

IV. Experimental Results

The FSK transceiver has been fabricated in 90-nm CMOS technology. Figure 5(a) shows the die photograph, which occupies 1.4×0.9 mm^2. Flip-chip technology has been used here [Fig. 5(b)]. To suppress surface wave and reduce unwanted coupling, a λ/4-wide surrounding ground ring is placed around the antenna. A λ/2 gap between antenna and ground ring is chosen such that the reflected wave can constructively enhance the radiation. The transceiver consumes a total power of 500 mW, of which 280 mW dissipates in Tx, 150 mW in Rx, and 70 mW in frequency synthesizer.

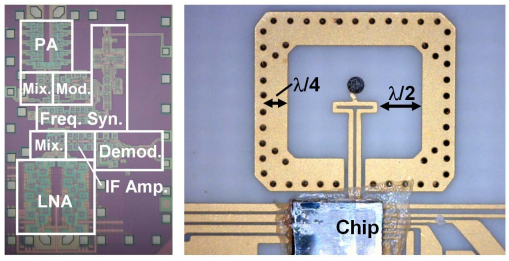

Fig. 5. (a) Transceiver micrograph, (b) flip-chip assembly.

The PA's output power when driving 50-Ω loading is 0 dBm. As shown in Fig. 6, with a 500-Mb/s data input of 2^{31}–1 PRBS, the output spectrum presents two sinc functions located around 57.5 and 62.5GHz, respectively. The sideband spurs of the transmitter are measured as –34dBc and –31dBc, respectively, when the input data is logic 1 and 0. The PA has 9-dB gain, 5-dBm P_{1dB} and 7.6-dBm maximum P_{out}. The LNA reveals 18.9-dB maximum gain and –18-dB minimum S_{11}. The transceiver input and output matching performance is depicted in Fig. 7(a), implying > 9-GHz bandwidth around 60 GHz (for –10-dB threshold). The synthesizer presents an operation range of 39.7~41.7GHz. Figure 7(b) illustrates the 40-GHz clock spectrum, revealing phase noise of –95.3 dBc/Hz at 1 MHz offset. Figure 8(a) shows the recovered data eye at the receiver's output when delivering 1.5-Gb/s 2^{31}–1 PRBS through the folded dipole antennae. A complete BER test has been conducted as well [Fig. 8(b)]. The transceiver achieves an error-free (BER < 10^{-12}) operation at a data rate greater than 2 Gb/s. Table I summarizes the overall performance of this work.

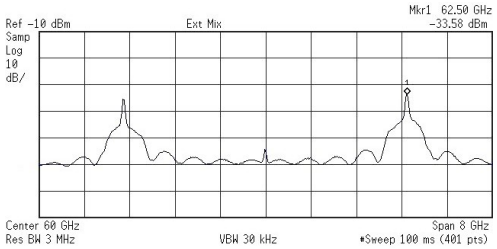

Fig. 6. FSK spectrum with 500-Mb/s 2^{31}–1 PRBS.

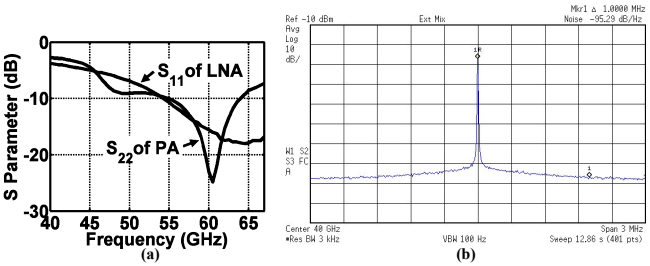

Fig. 7. (a) Input/output matching of the transceiver, (b) output spectrum of 40-GHz clock.

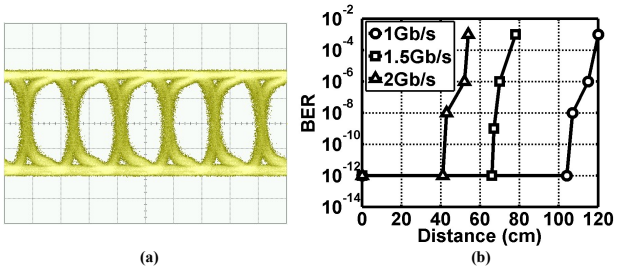

Fig. 8. (a) Rx's recovered data (1.5 Gb/s, horizontal scale = 400 ps/div, vertical scale = 100 mV/div), (b) BER test.

Tx	
S_{22}	–24.8dB
P_{out}	0dBm
Sideband Spur	<–31dBc
Freq. Synthesizer	
Freq. (GHz)	39.7 ~41.7
PNoise @1MHz	–95.3 dBc/Hz
Ref. Spur	–51.3 dBc

Rx	
S_{11}	–18dB
LNA	
Gain	18.9dB
S_{22}	–15.5dB
TRx BER Test	
2^{31}–1 PRBS (BER < 10^{-12})	
1Gb/s	104cm
1.5Gb/s	66cm
2Gb/s	41cm

Supply Volt.	
LNA/PA PLL	1.2V
Others	1.5V
Power	
Tx	280mW
Rx	150mW
PLL	70mW
Area	1.4x0.9 mm^2
Tech.	90nm CMOS

Table. I. Performance summary.

Acknowledgement

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