18.6 A Low-Power Fully Integrated 60GHz Transceiver System with OOK Modulation and On-Board Antenna Assembly

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Emerging research on 60GHz RF transceivers has demonstrated extensive usage of short-distance communications. One key application is the fast file-transfer system for consumer products, e.g., video download from a kiosk or link between a digital camera and a laptop, where high-speed (a few Gb/s) and low-power (<0.3W) wireless communication is required for short distance (<10cm). Existing 60GHz solutions [1] inheriting the well-developed architecture from 2.4/5GHz systems consume significant power primarily because of the interface (ADCs) and the subsequent baseband circuits (DSPs). This paper presents a compact solution for a 60GHz transceiver system including on-board antennae and on-off-keying (OOK) modulation. This prototype avoids the above issues and achieves error-free operation (BER<10^{-12}) for 2^{31}–1 PRBS of 2.5Gb/s over a distance of 4cm while consuming a total power of only 286mW.

Figure 18.6.1(a) illustrates the transceiver architecture. The transmitter consists of a 60GHz VCO (VCO_1), an OOK modulator, and a differential power amplifier (PA). The input data modulates the 60GHz clock before it is delivered to the PA, which incorporates 5-stage class-A architecture to achieve 7dBm differential output with reasonable power consumption. The first PA stage is depicted in Fig. 18.6.1(b). Here, the input and interstage matching of the PA are realized as conjugate matching, whereas the antenna impedance is designed as 100Ω differentially. The measured large-signal performance of the PA at 60GHz is shown in Fig. 18.6.1(c), revealing a peak gain of 9.6dB and P_{1dB} of 5dBm. The receiver comprises a differential LNA, a mixer, an IF amplifier, and an OOK demodulator. The input signal from the antenna is amplified by the LNA and then downconverted by the mixer to about 10GHz. Another on-chip VCO (VCO_2) provides the LO signal of around 50GHz. Note that the choice of VCO_2 frequency is a compromise between the maximum data rate and the IF amplifier bandwidth.

The VCO_1 and modulator designs are shown in Fig. 18.6.2(a). Employing the 3λ/4 technique proposed in [2], the VCO extends the resonating inductors twice between the VCO_1 and the modulator to reduce the capacitive loading seen looking into the M_4-M_5 pair at a cost of slightly higher loss. Without this technique the VCO_1 with the same power and device size will oscillate at only 35.5GHz. The level-boosting transistor M_3 not only raises up the common-mode level of CK_{out}, but facilitates a self-biased dc coupling between the two blocks. That is, with proper scaling, the pair M_4-M_5 experiences optimal input drive from VCO_1, since M_3 imitates the on-resistance of the bottom switch M_8. In the modulator, switches M_6, M_7 and M_8 completely block the input clock when they are turned off, preventing signal leakage to the output. The PMOS switch M_9 is also introduced to achieve a quick shut-off. Simulation shows that such a resetting improves the transitions by 80ps, making the transceiver more robust at high-data-rate operation. Figure 18.6.2(b) reveals the measured OOK signals in time and frequency domains captured from the PA output.

The LNA and mixer designs are shown in Fig. 18.6.3. Similar to the PAs, two identical LNAs are employed to form a pseudo differential operation. Each LNA contains three stages, one of which is illustrated in Fig. 18.6.3 as an example. Cascode topology with shunt-peaking is used to achieve better isolation and higher conversion gain. The peaking inductor L_P not only resonates out the parasitic capacitance associated with the internal node P, but also provides image rejection when the series capacitor C_S is properly chosen. The equivalent impedance of the peaking network is given by

$$Z_{in} = \frac{1 + s^2 L_P C_S}{s[(C_P + C_S) + s^2 C_S C_P L_P]} .$$

That is, the impedance drops to zero at $(L_P C_S)^{-1/2}$ and approaches infinity at $[L_P C_S C_P/(C_S+C_P)]^{-1/2}$. In other words, the circuit allows more RF signal current flowing toward the load, and rejects the image (to some extent) by shorting the current to ground. Again, conjugate matching is used between stages. To achieve a wider operating range, the three stages resonate at slightly different frequencies. A double-balanced mixer capacitively couples the RF signal into the mixer core. Similar to [3], the parasitic capacitances associated with the common-source nodes A and B are resonated out by the loading inductor L_D of the last LNA stage. Resistive loading (R_D) is sufficient here to provide conversion gain while rejecting the undesired LO coupling.

The OOK demodulator is shown in Fig. 18.6.4. Conventional envelope detectors such as common-source rectifiers suffer from small output swing (or equivalently poor SNR) and high parasitic capacitance. In this work, an efficient realization rectifies the differential input (V_{IF}) through the class-AB amplifiers M_1 and M_2, which are properly biased by means of M_3, R_b, and I_b. The R_1-C_1 network corner frequency is located between the data rate and twice the IF frequency in order to filter out the undesired IF ripple (20GHz) while allowing the recovered data to pass through. The single-ended output V_0 is converted back to a differential signal by distilling the dc level through R_2 and C_2. Since V_0 is relatively faint (<100mV), the generated D_{out} is further enlarged to typical logic level (≈500mV) by the subsequent limiting amplifier, made up of differential pairs with resistive loads. The offset-compensation pair M_8-M_9 neutralizes the mismatch along the data path, if any.

The antenna is realized on a low-loss board (Rogers RO4003), which must be at least 500μm high in order to provide 100Ω differential impedance. To minimize the bonding wire distance, we boost the chip by placing BGA tin balls underneath [Fig. 18.6.5(a)]. Each output node on chip has three parallel gold wires (with 20μm diameter) connected to the antenna trace on board, presenting parasitic wire inductance of less than 100pH. All the low-speed, dc, and power lines are directly wire bonded to the main board. Figures 18.6.5(b) and (c) show the measured performance of the antenna, revealing a –10dB S_{11} bandwidth of 7.5GHz and a gain of 5dBi. The beamwidths in the E-plane and H-plane are 78° and 76°, respectively.

The transceiver is fabricated in 90nm CMOS technology. The transmitter consumes 183mW and the receiver 103mW. The input/output matching (S_{11} of LNA and S_{22} of PA) is depicted in Fig. 18.6.6(a), suggesting –10dB bandwidth of more than 13.6 and 15.8GHz, respectively (measurement limited to 65GHz). To gain more insight, a standalone 60GHz LNA+mixer combination has been designed and tested independently, which achieves 25dB peak conversion gain, 7dB NF, –26dBm P_{1dB}, and –16dBm IIP3 for the band of interest. Figure 18.6.6(b) illustrates the receiver output in response to a 3Gb/s PRBS of length 2^{31}–1. A complete BER test is shown in Fig. 18.6.6(c). Note that longer distance can be achieved by increasing the power. Figure 18.6.7 shows the die micrographs, where the transmitter occupies 0.43mm^2 and the receiver 0.68mm^2, including pads. A photo of the TX test board assembly and a table summarizing the performance are also shown in Fig. 18.6.7.

Acknowledgment:
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References:
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[2] Jri Lee et al., "A 75GHz Phase-Locked Loop in 90nm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1414-1426, June 2008.
[3] Behzad Razavi, "A mm-Wave CMOS Heterodyne Receiver with On-Chip LO and Divider," *ISSCC Dig. Tech. Papers,* pp. 188-189, Feb. 2007.

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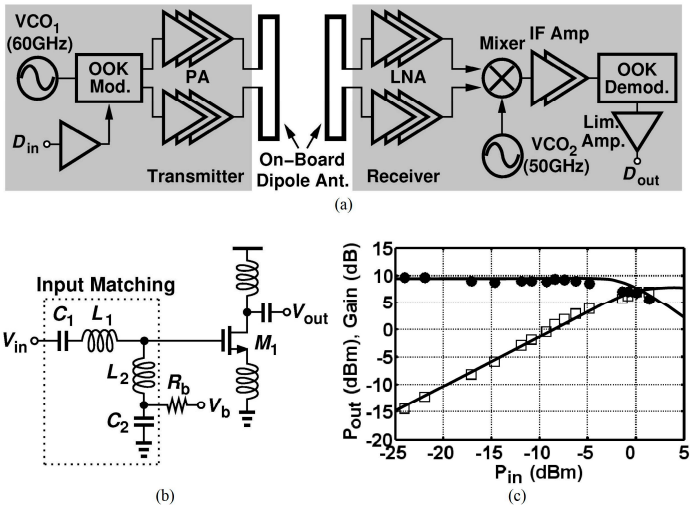

Figure 18.6.1: (a) Transceiver architecture, (b) one PA stage, (c) measured gain and P_{out} of PA.

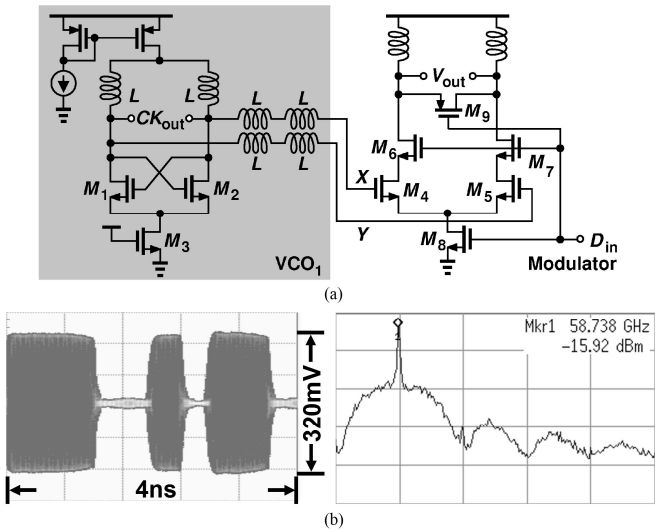

Figure 18.6.2: (a) VCO1 and OOK modulator, (b) measured OOK signals at PA output (left: 2.5Gb/s, right: 1Gb/s).

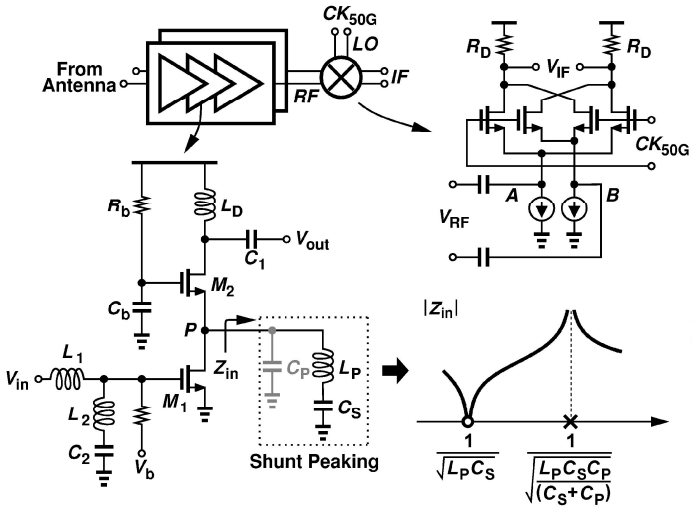

Figure 18.6.3: LNA and mixer design.

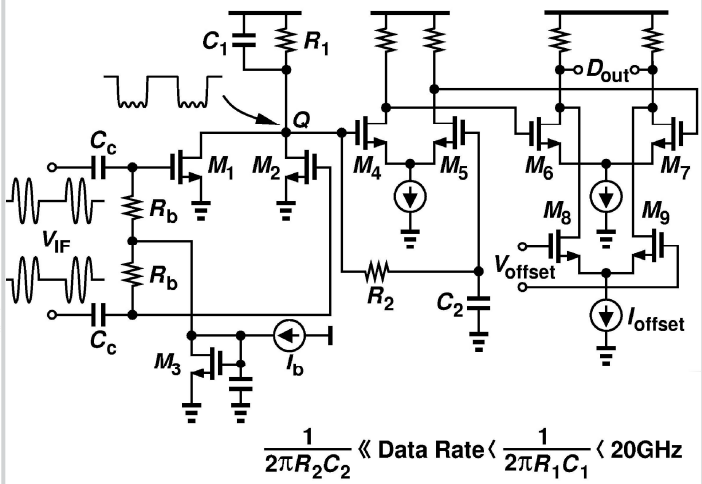

Figure 18.6.4: OOK demodulator.

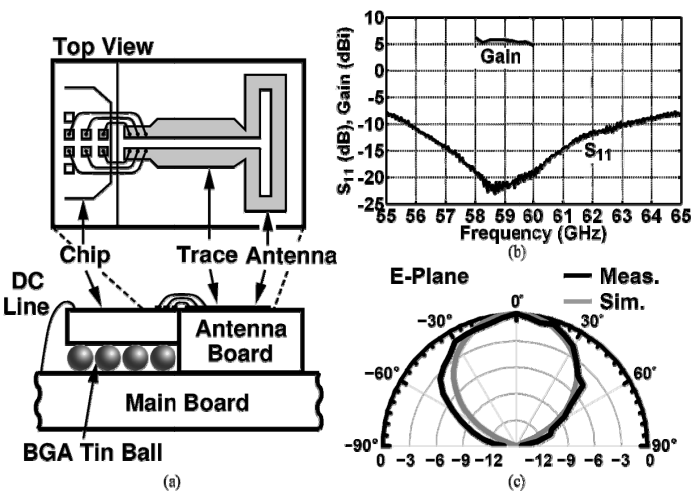

Figure 18.6.5: (a) Chip and antenna assembly, (b) S_{11} and gain of the dipole antenna (equipment limited), (c) antenna pattern (E-plane).

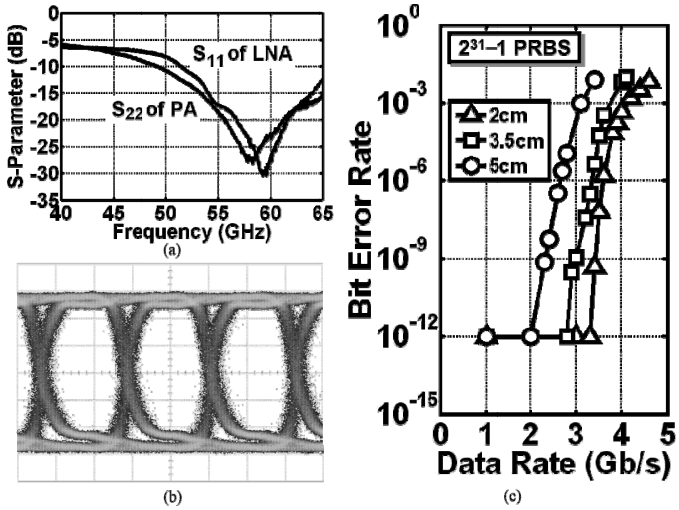

Figure 18.6.6: (a) Input/Output matching of the transceiver, (b) recovered data at 3Gb/s (vertical scale: 60mV/div, horizontal scale: 150ps/div), (c) BER test.

Tx	
S_{22}	−28.1dB
VCO_1	
Freq.	59.5GHz
PA	
P_{1dB}	5dBm
$P_{out,max}$	7.6dBm
Gain	9.6dB

Antenna	
Gain	5dBi
S_{11}	−23.5dB
Beamwidth	78° (E) 76° (H)
Bandwidth	7.5GHz
Estimated Efficiency	83 %

Rx	
S_{11}	−30.4dB
VCO_2	
Freq.	51.1GHz
LNA+Mixer (standalone)	
NF	7dB
Gain	25dB (with IF amp.)

Overall	
Supply	LNA & PA: 1.2V Others: 1.5V
$2^{31}-1$ PRBS, BER<10^{-12}	
2Gb/s	5cm
2.5Gb/s	4cm
Area	Tx: 0.43mm^2 Rx: 0.68mm^2
Power	Tx:183mW Rx:103mW
Tech.	90nm CMOS

Figure 18.6.7: Die micrograph, testing board, and performance summary.

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