A 6-b 1-GS/s 30-mW ADC in 90-nm CMOS Technology

Yuan-Ching Lien and Jri Lee

National Taiwan University, Taipei, Taiwan

***Abstract*-A 6-b 1-GS/s subranging ADC with THA is implemented in 90-nm CMOS technology. This circuit incorporates folded input for the fine ADC as well as offset calibration and digital correction techniques, achieving greater than 5.2 ENOB and 40-dB SFDR up to the Nyquist, and 1.1-GHz ERBW with power consumption of only 30 mW.**

I. Introduction

High-speed low-power ADCs have found extensive usage in ultra-wideband (UWB) systems, 60-GHz RF, disk drive front-ends, and advanced backplane receivers. In most applications, it is desirable to have an ADC with at least 6-bit resolution and 1-GS/s sampling rate. A two-step subranging architecture manifests itself in embedded systems due to the compact structure and power efficiency.

This work describes the design of a 6-bit 1-GS/s subranging ADC in 90-nm CMOS technology. Incorporating offset calibration and digital error correction techniques to further improve the performance, this work achieves greater than 5.2 effective number of bits (ENOB) and 40-dB spurious free dynamic range (SFDR) across the whole Nyquist band with only 30 mW. The high effective resolution bandwidth (ERBW) of 1.1 GHz facilitates its application in both Nyquist and sub-sampling operations.

This paper is organized as follows. Section II introduces the ADC architecture. Section III describes the individual building blocks as well as their design considerations. Section IV presents experimental results and performance comparison.

II. ADC Architecture

Fig. 1 shows the ADC architecture. The fully-differential circuit consists of two THAs, a 2-bit coarse ADC, a 4-bit fine ADC with over-range slices, and error correction circuits. To minimize timing skews and input-dependent distortion, THAs with bootstrapped switches are employed to present a static voltage to the ADCs. After the coarse conversion, the quantized output selects an appropriate sub-range from the reference ladder by means of an array of switches. Conventional approach would require 4 pairs of switches for each reference level, causing large parasitic capacitance, complicate routing, and long settling time on the reference selection. We here propose a folded structure to alleviate the difficulties. The operation of the 2 lower sub-ranges can be degenerated into the 2 upper ones, if the THA's output is rectified before being sent to the fine ADC. That is, we swap the connection of the differential signal if the output is negative. As a result, the number of switches as well as the routing complexity reduces by a factor of 2. The input-folded scheme also halves the

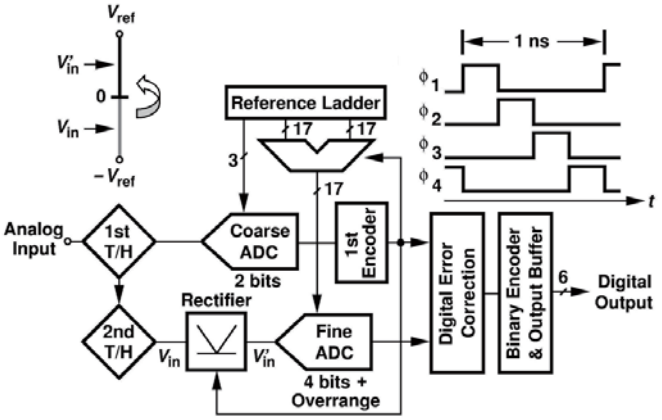


Fig. 1. ADC architecture.

maximum voltage swing at V'_{in} in the fine ADC. The bandwidth requirement of the buffer in the 2nd T/H used to drive the preamplifiers is relaxed. It also improves the performance of near-Nyquist operation since the preamplifiers and comparators need not experience large difference between two consecutive inputs. Because the operation time for different blocks is not equal, it is desirable to partition the clock into more segments with an imbalanced duty cycle. Here, 4 non-overlapped clock phases ϕ_1-ϕ_4 manage the timing of the whole ADC. The THAs, preamplifiers, and comparators of the coarse and fine ADCs are driven by different phases, forming a tight pipeline along the data path. Foreground offset calibration is executed at power up in both stages. The fine converter has additional preamplifier+comparator slices on both edges to accommodate possible over range. Note that some reference nodes close to the edges require no switches, lightening the load of selection signals by approximately 20%. The error correction unit collects the thermometer codes of length 20 (3 for coarse and 17 for fine) and cleans up bubbles by a democratic decision circuit, yielding a 6-bit synchronized output in parallel.

Another design issue of subranging ADCs arises from the reference voltage switching. The switching connection between the resistor ladder and the preamplifiers may lead to significant parasitic capacitance and slow down the circuit. To minimize the routing, we place the connection as shown in Fig. 2. Here, the ladder is double-folded, simplifying the subsequent routing considerably. The MUX array serves as a rectifier that reduces the number of connections to the preamplifiers of the fine ADC by a factor of 2. In such an arrangement, the topmost MUX experiences the largest swing, whereas the bottom one the smallest during switching. We apply the control signal V_{sel}

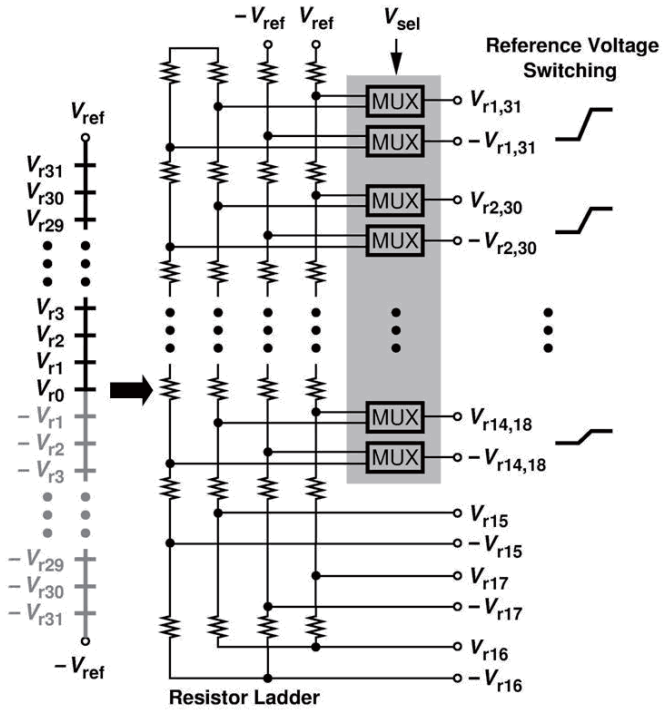


Fig. 2. Layout floorplan of the resistor ladder.

from the top to compensate for the unequal settling time to some extent. Note that in order to conduct the error correction, the four subranges are overlapped and only 14 MUXs are required.

III. Building Blocks

A. Preamplifier

As the device size goes down, the offset issue becomes unbearable in advanced CMOS technologies. In this design, the raw offset of the preamplifier-comparator combination reaches 25 mV, which is equivalent to 2 LSB. Resistive averaging could suppress the mismatch effect, but it works only if the voltage headroom is sufficient. In a low supply environment, the gain of the first differential difference stage is limited to about 4, making the offset of the comparator following the preamplifier dominate. In other words, resistive averaging would be useful if it is can be applied to both the preamplifier and the comparator stages, but it in turn degrades the bandwidth and consumes more power.

Our preamplifier incorporates digital offset cancellation to overcome the intrinsic mismatch. Fig. 3(a) depicts one slice of the fine ADC, where an offset calibration unit detects the comparator's output and adjusts the preamplifier's balance accordingly. In a manner similar to that in [1], the calibration unit consists of a 6-bit DAC and up/down counter to tune the current sources αI_A and $(1-\alpha)I_A$ in the preamplifier [Fig. 3(b)], arriving at a residual offset of 0.1 LSB after calibration. With offset calibration, the device sizes as well as the consumed currents are substantially reduced. Note that all slices in the coarse and fine ADCs undergo this procedure simultaneously at power up. The two-stage preamplifier provides a voltage gain

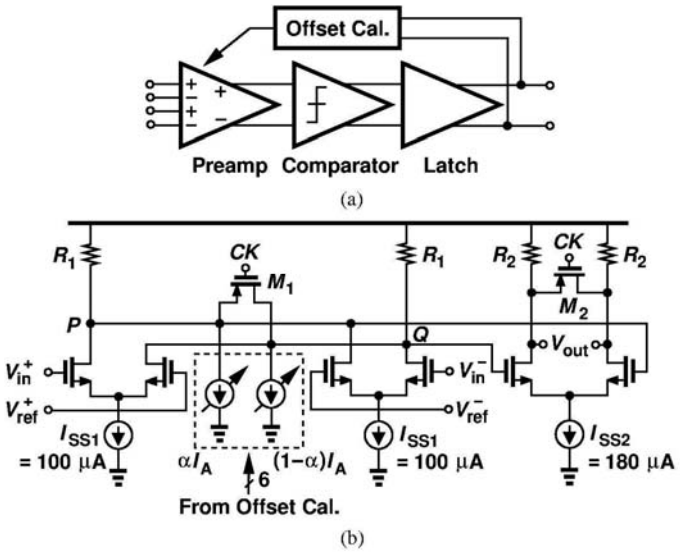


Fig. 3. (a) One segment of fine ADC, (b) preamplifier.

of 15 dB, and the reset switches M_1 and M_2 are employed to achieve fast overdrive recovery.

B. Track-and-hold amplifier (THA)

Fig. 4 illustrates the THA design, where bootstrapped switch M_1 ensures a constant overdrive and eliminates the signal-dependent distortions. Resembling that in [2], a dummy transistor M_3 (identical to M_1) along with switches S_1 and S_2 cancels out the input-dependent feedthrough, leaving only common-mode deviation on V_{out} when the THA goes from sample to hold. With deep N-well devices available, an NMOS-based source follower (M_2 and I_b) is used here to extend the bandwidth. For C_H = 250 fF, $(W/L)_1$ = (13/0.1) and $(W/L)_2$ = (80/0.1), the THA achieves a linearity of greater than 8 bits and a settling time of less than 30 ps.

C. Comparator

Fig. 5 reveals the comparator design, which along with the subsequent SR-latch provides rail-to-rail output for the digital circuits and reduces the metastability. The timing diagram of the fine ADC is also shown here. With the help of 25% duty-cycle clocks, the preamplifier amplifies the signal in the first 3/4 cycle, and the comparator further regenerates it in the last quarter of a clock period.

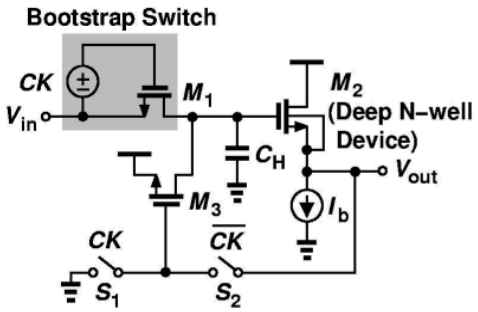


Fig. 4. The THA.

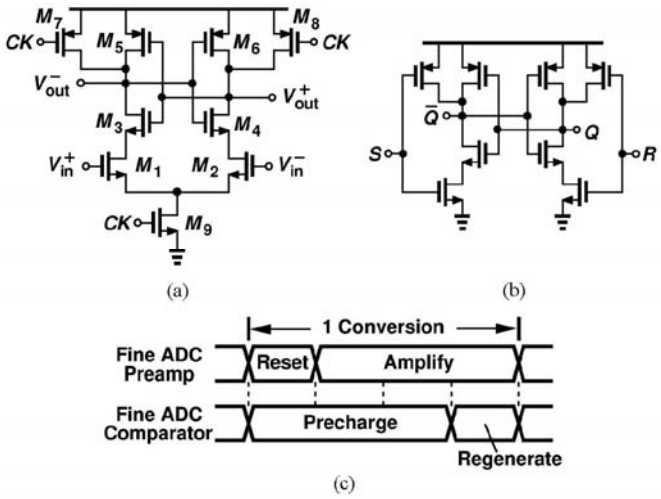


Fig. 5. (a) Comparator, (b) SR-latch and (c) its operation.

D. Clock buffer

The input clock buffer is depicted in Fig. 6, which consists of two stages of tapered inverters with deskew coupling between CK and $\overline{CK}$. The input nodes are terminated with two 50-Ω resistors on chip to suppress any possible reflection which may upset the clock duty cycle. The 4-phase clock generator is based on true single-phase clocked (TSPC) circuits to minimize the power consumption.

E. Inter-stage error correction

A potential problem of the two-step subranging architecture is the mismatch between the coarse and fine ADCs. The mismatches can be categorized as offset and gain errors. While the offset error results in a dc tone and can be removed by the subsequent digital processing circuit, the gain error would lead to an inter-modulation tone between the input frequency and half sampling rate. In this work, we put two additional comparators at each edge of the comparator array in the fine ADC to accommodate the out-of-range operation. Once the inter-stage gain error occurs, a digital logic circuit would correct the 2-bit MSB output from the coarse ADC accordingly.

IV. Experimental Result

The ADC has been fabricated in 90-nm 1P9M CMOS technology and tested on a chip-on-board assembly with 1.2-V analog/1.0-V digital supplies and a 800-mV differential input swing. Fig. 7 shows a photo of the die. The input signal is generated by Agilent 8644B (for frequency under 1030 MHz) and R&S SMA100A for (frequency above 1030 MHz). A

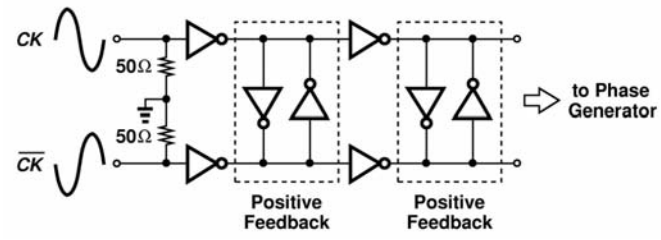


Fig. 6. Clock buffer.

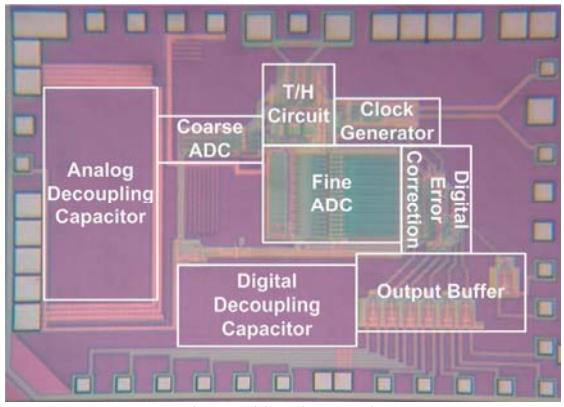


Fig. 7. Chip micrograph.

tunable band-pass filter (BPF) with center frequency from 65 MHz to 2000 MHz is used to suppress the harmonics of the input signal, resulting in an input with about –55 dBc THD. A passive balun converts the single-ended output of the BPF to differential analog signal, and the differential clock signal is generated by Agilent 81134A pulse pattern generator. The 6-bit digital output is directly captured and analyzed by the Agilent 16900A logic analyzer with E5381A probes without down sampling.

The circuit consumes a total power of 30 mW, of which 8 mW is dissipated in the THA, 12 mW in the coarse and fine ADCs, and 10 mW in the digital circuits and the clock generator. The measured DNL and INL are shown in Fig. 8. The offset calibration improves the DNL from +1.78/−1.00 LSB to +0.35/−0.27 LSB, and the INL from ±2.67 LSB to ±0.61 LSB, respectively. Fig. 9(a) and (b) depict the output spectrum for 69-MHz and near-Nyquist (502-MHz) inputs, presenting SNDR of 34.61 and 33.18 dB, respectively. The SNDR and SFDR as a function of the analog input frequency are plotted in Fig. 10(a) and (b). The offset calibration technique improves the SNDR by approximately 5 dB (0.83 effective bits). At 1 GS/s, the SNDR stays greater than 33 dB (ENOB = 5.2 bits) for the full Nyquist band and rolls off to 29 dB at 1.4 GHz. The SFDR remains above 40 dB up to the Nyquist and above 37 dB up to 1.3 GHz. Fig. 11 shows the dynamic performance of the prototype as a function of conversion rate. With a fixed input frequency of 70 MHz, the ADC maintains a flat SNDR of about 35 dB (ENOB = 5.5 bits)

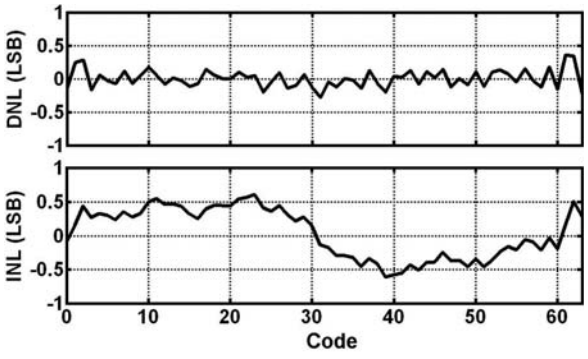
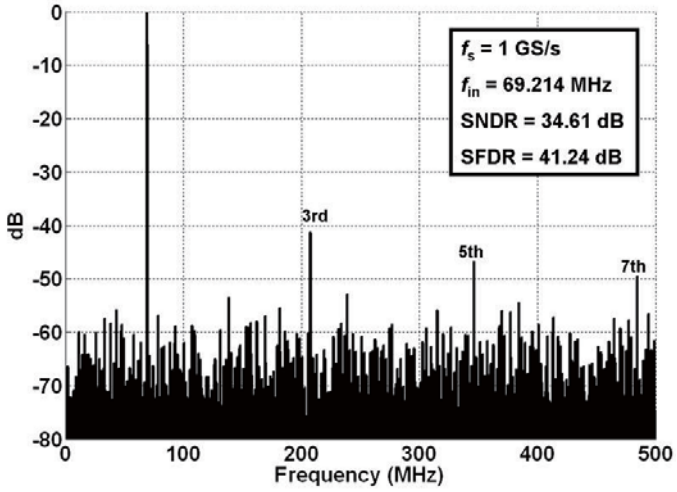
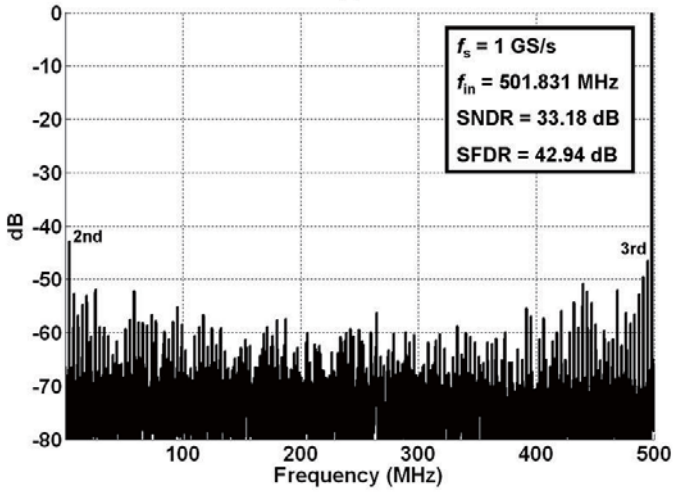


Fig. 8. Measured DNL and INL with calibration (f_s = 1 GHz)



(a)



(b)

Fig. 9. (a) Output spectrum of 69-MHz and (b) 502-MHz inputs.

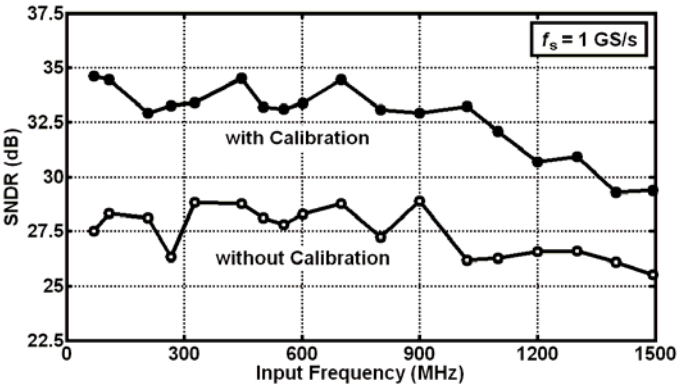


Fig. 10. (a) SNDR as a function of analog input frequency.

at low sampling rate and begins to fall at 1.2 GS/s. The ERBW measures greater than 1.1 GHz at a sampling rate of 1 GS/s. The FOM [defined as power/(sampling rate×2ENOB)] is equal to 0.8 pJ/conv., and the active die area occupies 0.18 mm^2. The performance of this work and some other previously published ADCs is summarized in Table I.

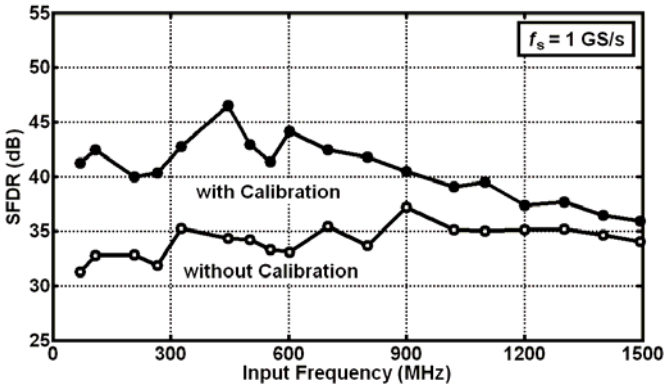


Fig. 10. (b) SFDR as a function of analog input frequency.

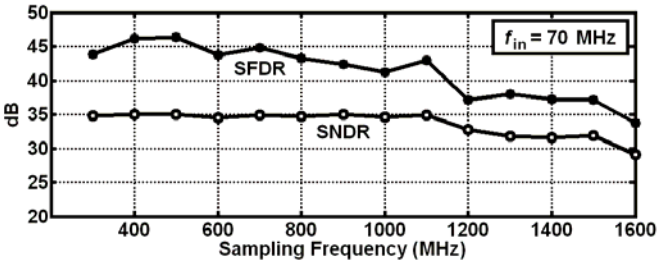


Fig. 11. Dynamic performance as a function of sampling rate.

TABLE I
ADC PERFORMANCE SUMMARY

	[3]	[4]	This Work
Resolution	6 bits	6 bits	6 bits
Conversion Rate	1 GS/s	1.2 GS/s	1 GS/s
DNL	+0.22/−0.28 LSB	<0.4 LSB	+0.35/−0.27 LSB
INL	+0.25/−0.28 LSB	<0.6 LSB	+0.61/−0.61 LSB
SFDR (up to Nyquist)	N/A	N/A	>40 dB
ENOB (DC/Nyquist)	5.5/5.3 bits	5.7/5.2 bits	5.5/5.2 bits
ERBW	N/A	700 MHz	>1.1 GHz
Input Range (Differential)	1 V_{pp}	N/A	0.8 V_{pp}
Power Consumption	55 mW	160 mW	30 mW
Core Area	0.13 mm^2	0.12 mm^2	0.18 mm^2
Supply Voltage	1.2 V	1.5 V	Analog: 1.2 V Digital: 1.0 V
FOM	1.4 pJ/conv.	3.6 pJ/conv.	0.8 pJ/conv.
Technology	90–nm CMOS	130–nm CMOS	90–nm CMOS

ACKNOWLEDGEMENT

The authors thank Szu-Kang Hsien in ITRI for testing assistance and TSMC for chip fabrication.

REFERENCES

[1] Y. Tamba, and K. Yamakido, "A CMOS 6b 500MSample/s ADC for a Hard Disk Drive Read Channel," *ISSCC Dig. Tech.* pp. 324-325, Feb. 1999.

[2] K. Nagaraj et al., "A Dual-Mode 700-Msample/s 6-bit 200-Msample/s 7-bit A/D Converter in a 0.25-µm Digital CMOS Process," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1760-1768, Dec. 2000.

[3] P. Figueiredo et al., "A 90nm CMOS 1.2V 6b 1GS/s Two-Step Subranging ADC," *ISSCC Dig. Tech. Papers,* pp. 568-569, Feb. 2006.

[4] C. Sandner, M. Clara, A. Santner, T. Hartig, and F. Kuttner, "A 6-bit 1.2-GS/s Low-Power Flash-ADC in 0.13-µm Digital CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1499-1505, Jul. 2005.