11.2 A Fully Integrated 77GHz FMCW Radar System in 65nm CMOS

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Millimeter-wave anti-collision radars have been widely investigated in advanced CMOS technologies recently. This paper presents a fully integrated 77GHz FMCW radar system in 65nm CMOS. The FMCW radar transmits a continuous wave which is triangularly modulated in frequency and receives the wave reflected from objects. As can be illustrated in Fig. 11.2.1, for a moving target, the received frequency would be shifted (i.e. Doppler shift), resulting in two different offset frequencies f^+ and f^- for the falling and rising ramps. Denoting the modulation range and period as B and T_m, respectively, we can derive the distance R and the relative velocity V_R as listed in Fig. 11.2.1, where f_c represents the center frequency and c the speed of light.

The transceiver includes an RF front-end (PA, LNA, and mixer), two horn antennaes with exciters, an FMCW generator, and an FPGA-based signal processor. Structures using an integer-N PLL together with a programmable DDFS as the reference input are popular in FMCW designs [1]. However, this approach usually suffers from severe power and area penalty. The DDFS also requires delicate DACs and large ROM table to arrive at fine frequency tuning (e.g., < 50kHz per step). In this prototype, we employ fractional-N PLL with a fixed reference (700MHz), in which the frequency modulation is accomplished by tuning the divide modulus. Here, the 77GHz VCO provides carrier signal directly to the RF front-end as well as the first divider stage, avoiding frequency doublers and other mm-wave circuits. A 16-bit $\Delta\Sigma$ modulator produces a 3-bit modulation signal to the ÷24~31 divider, which follows the 2nd divider. Note that the power consumption of this architecture is at least 2 orders less than that with DDFS. The $\Delta\Sigma$ resolution is given by $4\times700\text{MHz}/2^{16} = 42.72\text{kHz}$ and a stepping rate of 10MHz is chosen. As a result, one step corresponds to increasing or decreasing 2 LSBs in the $\Delta\Sigma$ modulator. The loop bandwidth of the frequency synthesizer must be much greater than the modulation frequency ($1/T_m$) and less than the stepping rate. We set the loop bandwidth to be 1MHz as an optimal value. Amplified by the on-chip PA, the output clock is delivered to the antenna by means of an mm-Wave coupler (exciter). Another antenna captures the reflected signal and couples it to the LNA. After mixing, the IF signal is distilled and processed by the subsequent DSP. We digitize the IF signal and conduct an FFT to calculate R and V_R. Note that Tx-Rx isolation is not an issue since the dc output will be eliminated in FFT. Algorithms are coded in an FPGA to achieve higher sensitivity and multi-target tracking.

Figure 11.2.2 depicts the VCO and the 1st frequency divider. The VCO is implemented as a standard LC tank structure with thick-oxide (5.6nm) varactors to suppress the leakage. To drive a large loading of 66fF for the divider, the PA, and the mixer at 77GHz, we employ a tuned amplifier pair M_3-M_4 as a buffer. The 1st divider is realized as a direct injection-locked topology, where the injection signal is ac-coupled to the gate of the switch M_7. The bias voltage V_b affects the lock range significantly. Higher V_b produces a larger lock range by degrading the tank Q, which in turn also decreases the output swing. The divider fails for $V_b \geq 1.0\text{V}$, where the equivalent tank loss exceeds $1/g_{m5,6}$. Here we choose $V_b = 0.8\text{V}$ to arrive at a lock range of 4GHz. The 2nd divider is implemented as a static topology made of CML flipflops with class-AB biasing and inductive peaking [2]. The ÷24~31 prescaler adopts the structure in [3], where four ÷2/3 cells are placed in cascade. Different types of latches (CML and TSPC) are employed to achieve high speed and low power consumption. The 16-bit $\Delta\Sigma$ modulator adopts MASH 1-1-1 structure.

The LNA is made of three identical cascade amplifiers, and each of them contains a cascode structure with conjugate matching networks [Fig. 11.2.3(a)]. In 65nm CMOS, the thickness of M1 (=0.18μm) is less than copper's skin depth at 77GHz (=0.25μm), leading to significant substrate leakage. Here, we shunt M1 and M2 with vias to form a thicker ground plane with no penetrating slot. The devices M_1 and M_2 are laid out with shared junction to minimize the parasitic capacitance of the internal node. Figure 11.2.3(b) depicts the PA design, which follows the design principle of [4] as a 5-stage structure with conjugate matching in between. A local bypass network C_1-R_1-C_2 (C_1 for in band, R_1-C_2 for out of band) is used to maintain high-frequency ac ground while ensuring low-frequency stability.

The mixer design is illustrated in Fig. 11.2.4(a). To conform to the 1.2V supply and ensure abrupt switching on M_3 and M_4, we separate the gain and switching stages [5], i.e., a tuned amplifier couples the output to the common-source node of the switching pair M_3-M_4. A single-balanced structure is used to reduce the LO port loading. Since IF is less than LO frequency by approximately 5 orders of magnitude, the LO feedthrough can easily be eliminated. Most RF current flows into the switching pair M_3-M_4 since the tail current I_b provides an output resistance much greater than $1/g_{m3,4}$. Parasitic capacitance associated with node P is absorbed as part of the matching network.

To feed transmission line signal into a waveguide, the PA's output (and the LNA's input) are connected to a quasi-Yagi antenna. It serves as an adaptor, to convert coplanar strip (CPS) to coplanar waveguide (CPW) by coupling the energy to (from) TE_{10} mode. As illustrated in Fig. 11.2.4(b), one slot line is terminated by a $\lambda/4$ slotline radial stub while the other is fed into the antenna. The transceiver chip is flipped on the same substrate of AIN (Aluminum Nitride). The high dielectric constant (ε_r=8.8) helps to reduce the exciter size. The quasi-Yagi antennaes are inserted into waveguides. Two W-band horn antennaes with 24dBi gain for each are used in this system.

The transceiver chip has been fabricated in 65nm CMOS technology. The circuit (FPGA not included) consumes a total power of 243mW, of which 73mW dissipates in the frequency synthesizer, 115mW in the PA, 30mW in the LNA, and 25mW in the mixer and buffers. For integer-N and fractional-N operations, the synthesizer presents phase noise of –85.3 and –84.6dBc/Hz, respectively, at 1MHz offset. Figure 11.2.5(a) shows one measured FMCW characteristic. The rms frequency error including turn-around points is less than 300kHz. The spread spectrum is also demonstrated in Fig. 11.2.5(b). Note that Fig. 11.2.5(a) is obtained from a standalone synthesizer that provides slightly lower (approximately 500MHz) modulation range. To verify the performance of each block, we have tested the LNA and PA individually. The LNA achieves 17.5dB gain, 7.4dB NF, –22dBm P_{1dB}, and –12.5dBm IIP_3 at 77GHz. Figure 11.2.5(c) depicts the LNA gain and NF around the band of interest. The PA reveals a peak gain of 13.7dB, P_{1dB} of 6.7dBm, and maximum PAE of 8.4% [Fig. 11.2.6(a)]. Using $B = 700\text{MHz}$ and $T_m = 1.5\text{ms}$ (range resolution $c/2B = 21.4\text{cm}$), we obtain the IF spectrum for detecting a stationary object at a distance of 33 meters [Fig. 11.2.6(b)]. The peak at 208.5kHz is observed as expected. Note that the undesired stepping modulation spur does not appear because of the low IF and high modulating resolution. Figure 11.2.6(c) shows the measured distance and relative velocity with an object of $40\times60\text{cm}^2$. The maximum detectable R is 106m, where the rms error is much less than the resolution. Figure 11.2.7 shows the die micrograph, which occupies $0.95\times1.1\text{mm}^2$. A table summarizing the performance is also shown in Fig. 11.2.7.

Acknowledgment:
This work is supported in part by NSC, MOEA, and MediaTek. The authors thank the TSMC University Shuttle Program and Dr. Sheu for chip fabrication.

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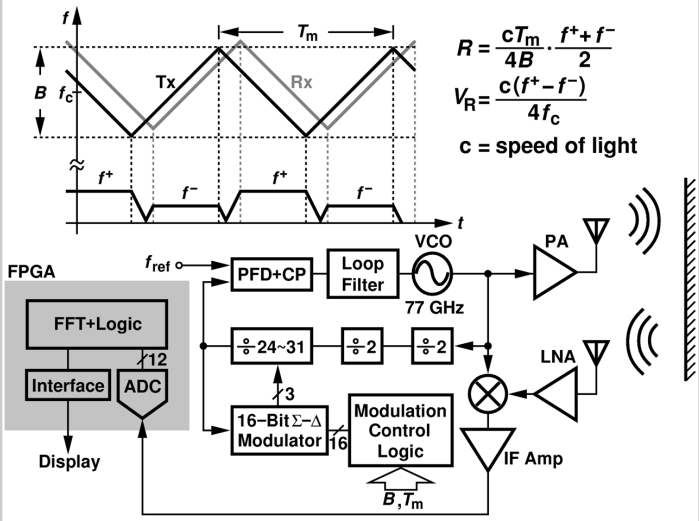


Figure 11.2.1: FMCW radar and proposed architecture.

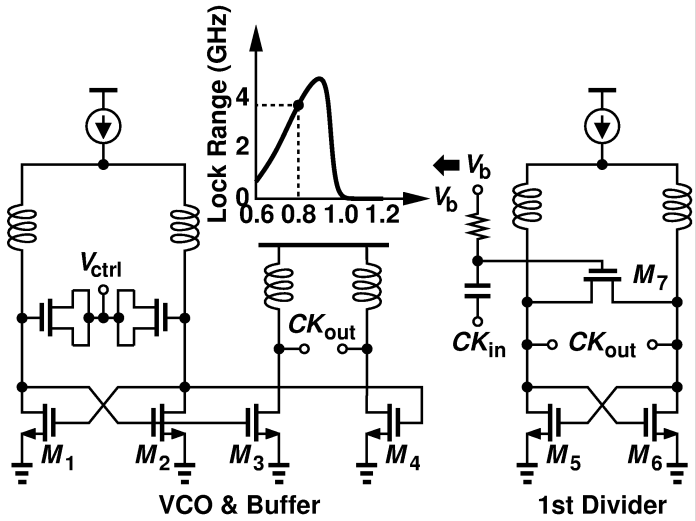


Figure 11.2.2: VCO, its buffer, and the 1st divider.

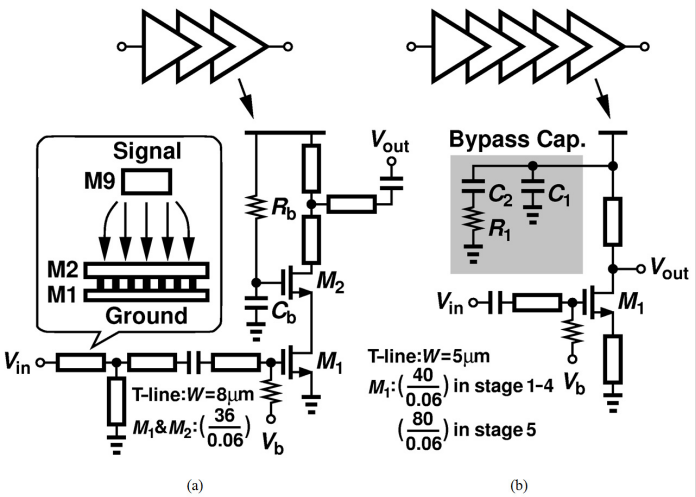


Figure 11.2.3: (a) LNA, (b) PA.

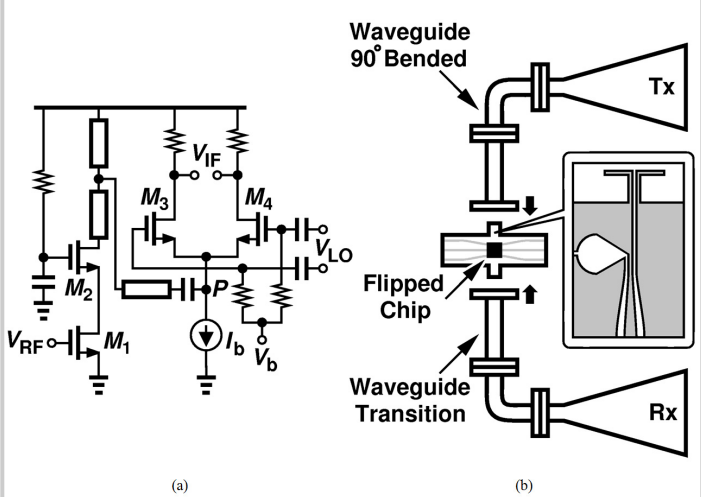


Figure 11.2.4: (a) Mixer, (b) system assembly.

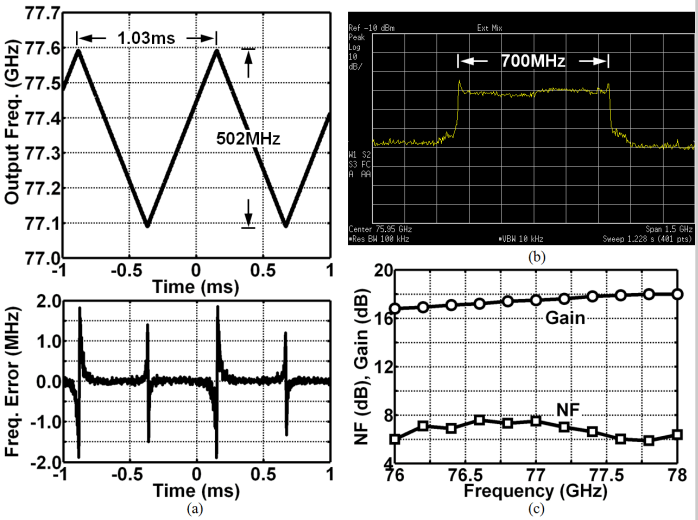


Figure 11.2.5: (a) Measured FMCW modulation B = 502MHz, T_m = 1.03ms, (b) spectrum for B = 700MHz, T_m = 1.5ms, (c) LNA gain and NF.

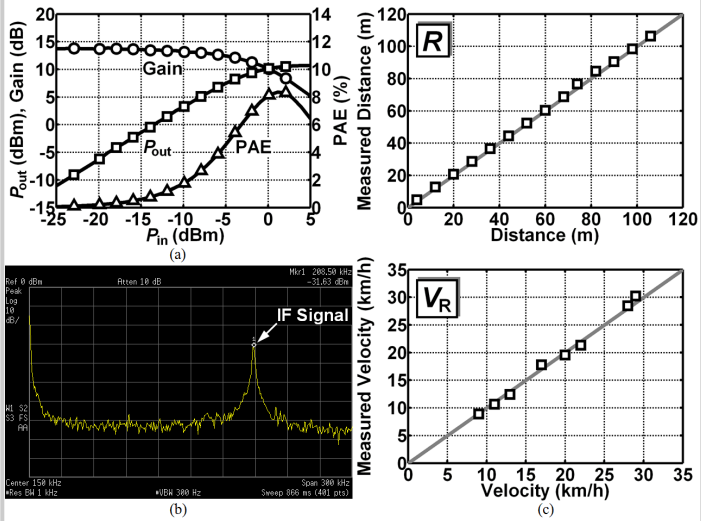
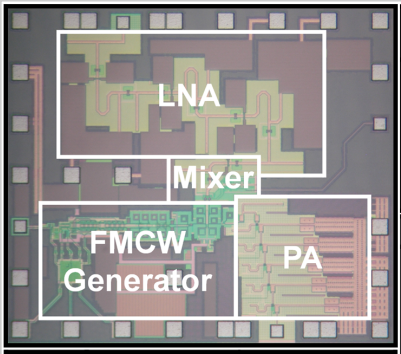


Figure 11.2.6: (a) Measured PA performance, (b) IF spectrum, (c) distance and velocity accuracy.



Overall	Supply	1.2V
	R_{max}	106m
	Area	0.95x1.1mm^2
	Power	243mW
	Tech.	65nm CMOS

Rx	Conv. Gain	38.7dB
LNA	Gain	17.5dB
	NF	7.4dB
	P_{1dB}	–22dBm
	IIP_3	–12.5dBm
	Power	30mW
Tx	P_{out}	5.1dBm
Freq. Syn.	Freq.	75.6~76.3GHz
	PN @1MHz	–85.3dBc/Hz
	Power	73mW
PA	Gain	13.7dB
	P_{1dB}	6.7dBm
	P_{sat}	10.5dBm
	PAE	8.4%
	Power	115mW

Figure 11.2.7: Die micrograph and performance summary.

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