A Fully-Integrated 77GHz Phase-Array Radar System with 1TX/4RX Frontend and Digital Beamforming Technique

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Abstract

This work presents a novel 77GHz automotive radar providing detection distance and angle up to 100m and ±8°, respectively. Using a 1TX/4RX array, this radar system employs various mmWave techniques to fulfill the expected SNR.

I. Introduction

77GHz automotive radar emerges to dominate the market of next generation long-range anti-collision devices. This paper presents an array-based system with LTCC antennae, which simultaneously detects the object's distance, relative speed, and angle.

II. Transceiver Architecture

Figure 1 shows the radar architecture, where 1 TX and 4 RX frontends are incorporated in one chip. A 38.5GHz FMCW clock generator reveals sawtooth-frequency modulation with a trigger signal for synchronization. After doubling the frequency, we have 77GHz signal fed into a PA and coupled to a power splitter. In contrast to the full-rate structure in [1], this arrangement obviates the possibility of injection pulling from the PA to the synthesizer. We also need PAs with high PAE so as to avoid high power consumption or possible heat issue in flip-chip assembly. An adaptively-biased PA has been proposed here, generating 12% PAE and 9dBm OP1dB with only 30mW of power. It is well known that phase arrays with RF shifting suffer from path loss and shifter nonlinearity, and those with LO shifting undergo complicated LO distribution and possible interference. Here, we adopt digital phase shifting architecture, which digitizes the IFs and realizes beamforming in DSP. Such a structure presents minimum signal loss, lowest power, and smallest chip area. An 1-to-4 power splitter evenly distributed the 77GHz local clocks, which, after converting to quadrature mode by 90° couplers, mix with the 4 incoming RF signals to obtain the beat frequencies and phase differences.

In this work, the object's angle is determined in an agile yet accurate way. As illustrated in Fig. 1, for a given angle θ, the two incident waves presents a phase difference $\Delta\phi=2\pi(d\sin\theta/\lambda)$, where d and λ denote antenna spacing and carrier wavelength, respectively. Since Δϕ is preserved after down conversion, we can easily obtain the object's angle θ in DSP. It also justifies the use of digital phase shifting structure. IF amplifiers as well as filters are buffered between mixers and ADCs to enlarge the dynamic range and reject undesired noise.

III. Building Blocks

Figure 2 depicts the PA design. To improve PAE, we need to bias the PA dynamically depending on the input power. Here, three staggered amplifier stages (with a crescendo factor of 1.6) are employed to create power gain of higher than 20dB. A coupler in the input port splits 25% of RF power into the power detector. After a 50Ω matching network, M_1 converts the RF power level into current mode, while M_2 produces a small quiescent current. The current is therefore transferred into proper voltage level by means of M_3-M_5 and R_1. It is

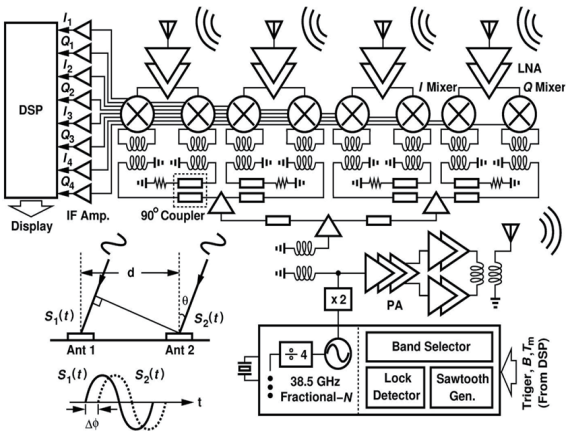


Fig. 1. Radar architecture.

obvious that once PA bias voltage V_b goes beyond certain level (≈0.8V), the output power does not increase significantly whereas the dc power does rise dramatically. As a result, a voltage-clamping transistor M_6 is placed to limit the highest V_b to around 0.8V. Note that low-pass filters ($1/g_{m3}$ and C_1, R_2 and C_2) are introduced along the bias circuit to stabilize power detection. Linearity is expected to be improved as well, since V_b will be increased in the gain compression region. In other words, AM-to-AM distortion can be minimized. As compared with feedback biasing control [2], this feedforward approach achieves much better power efficiency. The feedback biasing control must take part of the PA output to the power detector. Our all-analog adaptive biasing technique does not need any data converter and digital logic.

The FMCW generator consists of a 38.5GHz fractional-N synthesizer governed by control logics. The synthesizer incorporates a VCO, a third-order loop filter, a ÷4 circuit, a ÷24~31 prescalar commanded with 3 bits by a 1-1-1 Σ-Δ modulator, and a SSB-mixer based PFD to lock the frequency and phase with minimum reference spurs. A 700MHz PLL in front filters out the unwanted noise and coupling, and provides quadrature reference input.

A power splitter plays an important role in a multi-element transceiver. Even at 77GHz, a passive splitter is still quite big in size. A novel CMOS design with 1:4 active power division

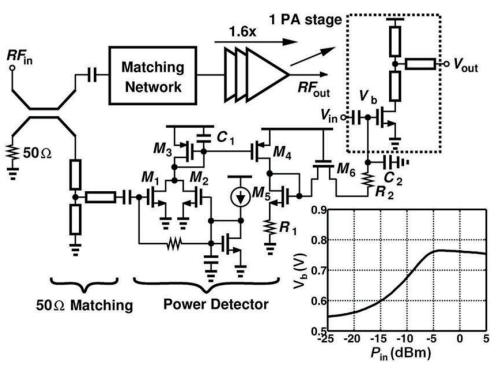


Fig. 2. Proposed adaptive biasing PA.

is shown in Fig. 3(a). After a 50Ω matching network, the input signal is transformed into current mode by means of the common-source amplifier M_1. The 2 equally-distributed RF currents are applied into 2 common-gate amplifiers with proper matching. Due to the very little reverse gain of common-gate devices (e.g., M_2 and M_3), the 1:4 splitter achieves a port-to-port isolation of 30dB. Shown in Fig. 3(b) is the IF amplifier. A self-biased, active-loading pair $M_{1,2}$ is source degenerated by R_S and switch M_3, performing low and high gains of 20 and 35dB, respectively. Second stage M_4 and R_D creates additional gain of 0 dB. Unlike typical 2-stage amplifiers which suffer from right-hand side zero, adding R_{S2} here simplifies biasing of M_4 and maintains 70˚ phase margin in a cost of slightly lower gain. Finally the system is assembled as illustrated in Fig. 3(c). The TRX chip is flipped on one side of the 9-layer LTCC through GGI process, and the LTCC board is mounted on a FR4 board (4 layers) by BGA balls. DSP, power, and other peripheral circuits sit on the back-end side of the main PCB. The antenna design is also shown here. The TX adopts 8 series-fed tapered antenna in parallel, and the RX connects to 4 identical 2×8 arrays for the 4 channels. The overall module volume is less than 4cm×2.5cm×0.7cm.

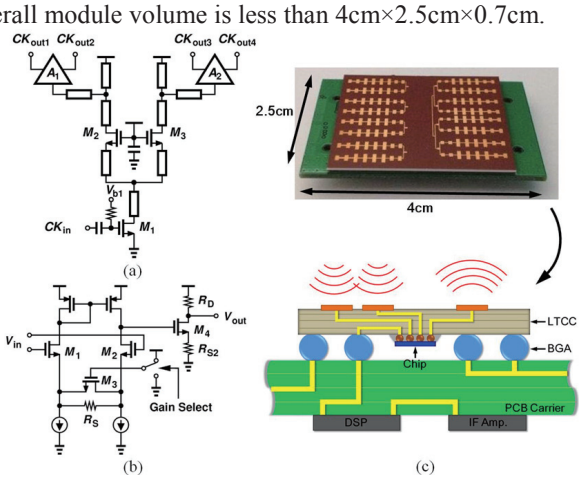


Fig. 3. (a) Power splitter, (b) IF amplifier, (c) system assembly and antenna layout.

IV. Experimental Results

The radar TRX has been fabricated in 65nm CMOS technology, dissipating 360mW of power from 1.2V supply. Figure 4(a) depicts the measured gain, P_{out}, and PAE of a single PA. Unlike typical PAs, the PAE stays at 12% from P_{in} = 13dBm all the way to P_{in} > 0dBm. PAEs at OP_{1dB} (=9.2dBm) and OP_{1dB} back off 6dB are 12.1% and 6.5%, respectively. These values are significantly better than those of other PAs recently published. In quiescent state, its power consumption drops to 30mW, revealing power efficiency. OP_{1dB} with and without the adaptive biasing is also shown here. As expected, it improves by 1.5dB~3.7dB for the band of interest. The PA presents a gain of 22dB, S_{11} < 8dB and S_{22} < 11dB for the band 70~90GHz. The phase noise plot of 77GHz clock in fractional-N mode is shown in Fig. 4(b), presenting phase noise of 83dBc/Hz at 1-MHz offset. The integrated jitter from 100Hz to 1GHz is given by 452fs. The 80MHz bandwidth allows the IF signals under any condition to pass through and rejects out-of-band noise. Figure 5(a) shows the RX recovered radiation patterns for ˜20˚, 0˚, and 20˚ beam-steering along H-plane. No side lobe higher than 6dB is observed. The angle measurement accuracy is reported in Fig. 5(b), demonstrating error of less than 0.6˚ for [-8˚, 8˚] range. For an object of 1600cm^2, we plot the measured SNR for different distance with 0˚ and ±5˚, which follows the trend of 4th-order radar equation [3]. The 4 RX frontend channels present isolation greater than 35dB among them, and the maximum I/Q mismatch are less than 2.5dB and 5˚. Figure 7 plots a photo of the die, which occupies 2.1×1.6 mm^2. Performance of this work is also summarized.

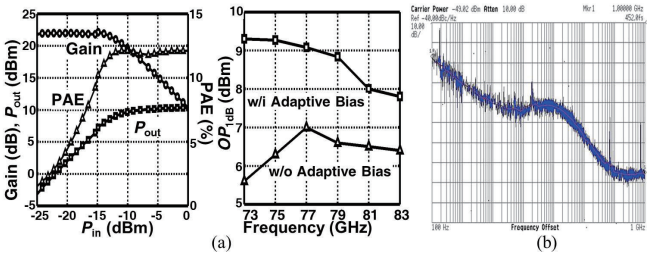


Fig. 4. (a) PA large-signal measurements and OP_{1dB}, (b) phase noise of 77GHz clock.

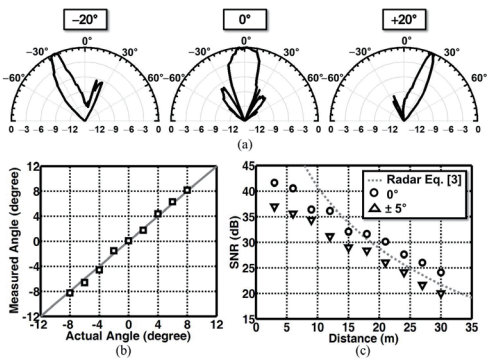
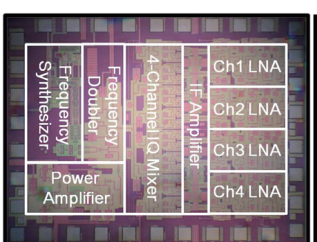


Fig. 5. (a) Normalized 4-element combined pattern in RX for 0^o, 20^o, and 20^o, (b) angle measurement accuracy, (c) SNR plot.



Overall	Supply	1.2V
	Area	2.1×1.6mm^2
	Power Consumption	360mW
	Technology	65nm CMOS
	Max. Det. Distance	100m
	Max. Det. Angle	±8°
	Min. Dist. Resolution	21cm
	Phase Shifting	Digital Baseband
	Package	LTCC

Tx	S_{22}	−10dB
	P_{out}	9dBm
	PA Gain	22dB
	PA OP_{1dB}	9dBm
	PA PAE@P_{1dB}	12%
FMCW Gen.	Carrier Frequency	77GHz
	Mod. Bandwidth	700 MHz
	VCO Max. Tuning	6GHz
	PNoise @1MHz	−83dBc/Hz
	Integrated Jitter	452fs
	Ref. Spurs	<−50dBc
Rx	Elements	4
	S_{11}	−11dB
	Conversion Gain	60dB (high) 45dB (low)
	Noise Figure	11dB
	3-dB Bandwidth	80MHz
	Ch-Ch Isolation	<35dB
	I/Q mismatch	2.5dB 5°

Fig. 6. Chip photograph and performance summary.

References

[1] Y. Li *et al.*, "A Fully-Integrated 77GHz FMCW Radar System in 65nm CMOS," *ISSCC*, pp. 216-217, Feb. 2010.

[2] A. Valdes-Garcia *et al.*, "A SiGe BiCMOS 16-Element Phased-Array Transmitter for 60GHz Communications," *ISSCC*, pp. 218-219, Feb. 2010.

[3] M. I. Skolnik, Introduction to Radar Systems. New York: McGraw Hill, 2001.