8.6 A 94GHz 3D-Image Radar Engine with 4TX/4RX Beamforming Scan Technique in 65nm CMOS

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Millimeter-Wave and sub-THz imaging sensors have been demonstrated in CMOS technology recently. Mechanical scanners are still required to capture the whole image, making the systems bulky and costly. The limited resolution of the third-dimension (z-direction) also leads to a vague 3D picture. Other 2D solutions need not only focal lens, but large chip area to accommodate more pixels. This paper presents a 94GHz 3D image radar with electronic scanning. Using a 4TX/4RX beamforming technique and a modulated time-of-flight (ToF) algorithm, this prototype achieves ±28° scanning range, 2m maximum distance, and 1mm depth resolution with 960mW of power.

The imaging radar is set up as illustrated in Fig. 8.6.1. Two dishes are mounted side by side, and both TX and RX chips are fixed around the focal points. Each of the 4 RF I/O ports of TX and RX drives a single patch antenna. Collecting the EM wave radiated from the TX, the first dish converges the beam to 1.5°. After reflection by the object, the returned waves are captured by the 2nd dish and thus the RX. Since the reflected wave can be characterized in strength, we can obtain the xy-plane information by beamforming. The TX structure is also shown in Fig. 8.6.1, where a 31.3GHz fractional-*N* synthesizer is adopted to create a fundamental clock. A wide-range ×3 circuit together with the enable pulse generator produces a 94GHz clock in continuous on-off mode. After amplification by the VGA, the RF signal is distributed into 4 paths by means of the power splitter. Based on the required angle, four phase shifters delay the RF signals accordingly, and the 4 PAs deliver the power to corresponding antennae. By changing the incident angle, we carry out 2-dimensional scanning with a maximum range of ±28°.

In order to capture the third-dimension profile, the TRX must calculate the time of flight of the wave traveling between TRX and the object. Using a fixed counting clock achieves poor resolution of only several centimeters. Here we follow the variable clock method presented in [1], i.e., by gradually altering the counting frequency, we narrow down the possible solution into a much smaller region. The fractional-*N* synthesizer provides precise clock frequency with fine tuning, allowing very accurate distance detection with only 1mm error.

The RX is depicted in Fig. 8.6.2. The same 31.3GHz fractional-*N* synthesizer is used here to provide LO signals. The input RF signals coming from the 4 antennae are amplified (by the VGLNA) and shifted in phase (by the phase shifter). The VGLNA is realized as cascade stages with distributed switches at the internal nodes to short-circuit a certain amount of RF current into ground. After power combination, the 94GHz RF signal is fed into a power detector to determine the amplitude of the reflected wave. The 94GHz RF also goes into a 2nd-order harmonic mixer and subsequently a fundamental mixer for downconversion. As a result, the IF signal (1/6 RF frequency) is generated and further amplified by an IF amplifier. This path is essential for the depth detection: after detecting the arrival time of the returned wave by different counting clocks, the distance of the RF signal path can be obtained and therefore the 3D profile is obtained. Note that to minimize walk error, two thresholds are provided to the pulse detector [1]. Other errors caused by TX/RX synchronization or incident angle are static and can be removed in DSP.

The 94GHz frequency tripler in the TX must provide large output swing and wide operation range. Conventional approaches use capacitor arrays or varactors to extend the resonance frequency of the tripler, which in turn limits the output swing significantly. The proposed ×3 circuit introduces a transformer between the 3rd-order harmonic and output stages to relax this issue. As shown in Fig. 8.6.3, a pseudo-differential pair $M_{1,2}$ along with a wideband matching network converts the fundamental signal (f_0) into its 3rd-order harmonic ($3f_0$). A transformer delivers RF power to the resonating stage $M_{3,4}$, whose resonance loading also filters out fundamental coupling. Since parasitics of $M_{1,2}$ are absorbed into the matching network, more $3f_0$ signal power can be injected into the resonating stage. A standalone tripler has been fabricated to verify its performance. With P_{in} = 0dBm, it presents a lock range of 13GHz, much wider than its bipolar counterparts [2]. The tripler is operated at $P_{out} \approx$ 0dBm, which operates from 88 to 96GHz with less than 1dB degradation. The fundamental and 2nd-order rejections are greater than 35 and 25dB, respectively.

Figure 8.6.4(a) depicts the 94GHz 7-bit phase shifter with two-step phase interpolation. The vector generator consists of a 90° coupler and 2 baluns, converting RF input into differential quadrature signals. The desired phase can be synthesized by properly adjusting the amplitude of quadrature signals. In the first step, the differential quadrature signals are parallelized into two coarse phase selectors. Each is driven by a DAC with 3 current sources, allowing 16 phase states with resolution of 22.5°. In the second step, a fine phase selector driven by a DAC with 5 current sources synthesizes another 3-bit fine phase state. The logic encoder is utilized with static CMOS gates such that the phase shifter can be controlled by 7-bit binary codes. The corresponding phase resolution is $360°/2^7 \approx 2.8°$. Using the two-step phase interpolation technique, the current DAC design can be much more relaxed. This is in contrast to the traditional one-step interpolation design, which needs a very high resolution DAC for the high current ratio of the two quadrature paths.

The power detector circuit in the RX must deal with very short pulse duration, implying the use of a sample-and-hold amplifier (SHA). The variable pulse arrival time also requires a gating clock, which enables SHA on occurrence of RF signal arrival. Figure 8.6.4(b) reveals such a design. After rectification, the averaged RF power gets sampled and held by the switch $M_{1,2}$ and capacitor C_1. The RF signal arrival is detected by limiting the rectified output and creating a proper timing window through a NAND gate, an inverter, and a delay $\Delta T(\approx 2ns)$. Such a simple yet efficient design relaxes the stringent speed requirement for the ADC. Meanwhile, due to the large input dynamic range, the pulse detector in RX needs to suppress the walk error caused by different power levels. The pulse detector design shown in Fig. 8.6.4(c) follows that in [1], incorporating two threshold voltages V_H and V_L and two comparators. By extrapolation we obtain the original point of pulse arrival in the time domain. An 8-bit TDC with 1ps resolution accomplishes this task by sweeping 256 frequency points. Offsets on z-axis measurement due to different angles can be compensated in DSP.

The TRX has been fabricated in 65nm CMOS technology. The TX consumes 600mW and the RX 360mW, respectively, from a 1.2V supply. Both TX and RX are flipped on one side of an LTCC board. The front-end is further attached to an FR4 board with BGA to form a compact assembly. The whole assembly is thus mounted on an xyz positioner located around the focal point of a dish. Figure 8.6.5(a) illustrates the phase noise of the 94GHz clock, presenting –85.6dBc/Hz at 1MHz offset. The modulated spectrum at the TX output is also shown in Fig. 8.6.5(b). With pulse width = 3.5ns and duty cycle = 3.5%, a sinc function around the 94GHz carrier is demonstrated. The phase and gain error of the phase shifter at 94GHz measure 1.4° and 0.73dB, respectively [Fig. 8.6.5(c)]. The S_{21} and S_{11} of the VGLNA are also plotted in Fig. 8.6.5(d), implying a tunable range of 13dB. Figure 8.6.6(a) reveals the power detector responsivity. The detectable range is about 30dB as expected. Figure 8.6.6(b) shows the normalized 4-element transmitted radiation pattern for two extreme cases of 2° and 28°. The testing setup for whole object scanning and one detected image are demonstrated in Fig. 8.6.6(c). Due to the limited gain of the dishes, our xy pixel size is about 5.4cm^2 at 1m. The 3.6×2.1mm^2 die micrograph is shown in Fig. 8.6.7. Performance of this prototype and some other works previously published is also summarized.

Acknowledgment:
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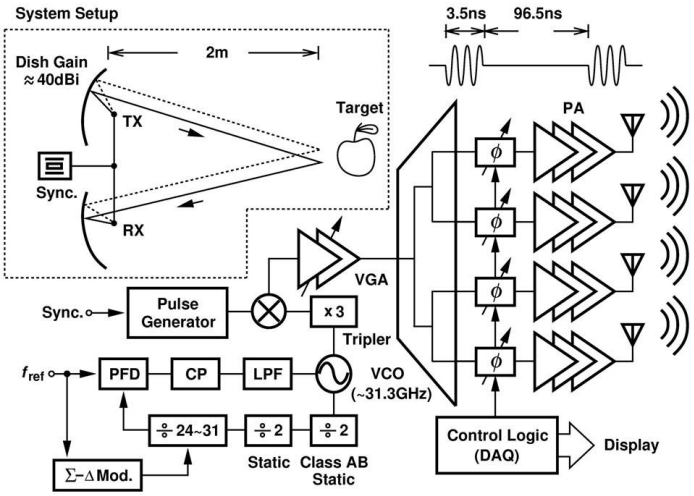


Figure 8.6.1: Imaging radar structure, TX architecture.

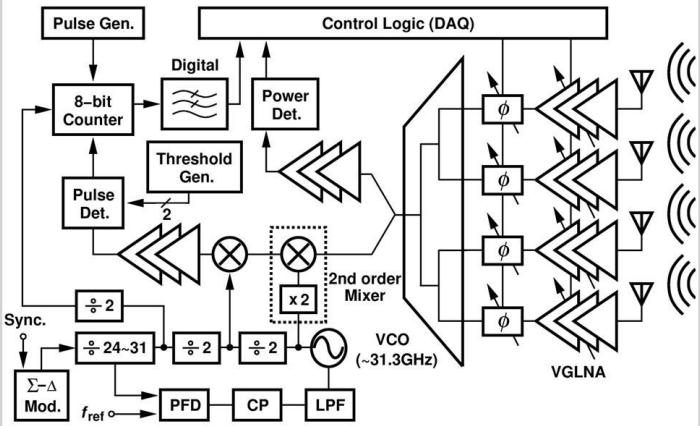


Figure 8.6.2: RX architecture.

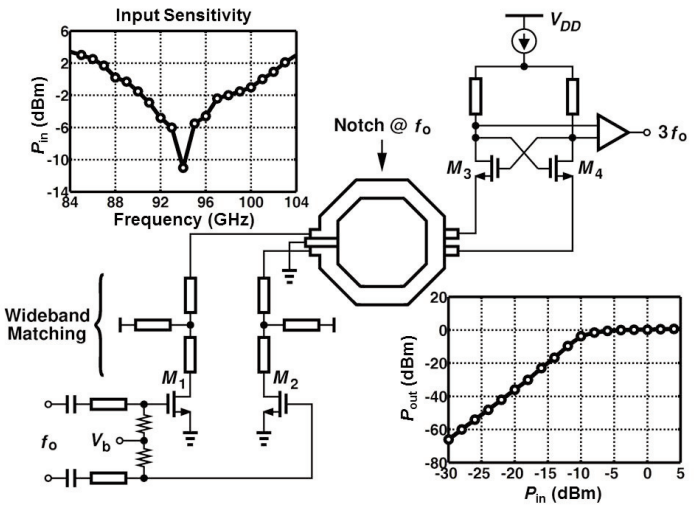


Figure 8.6.3: 94GHz frequency tripler with measured performance.

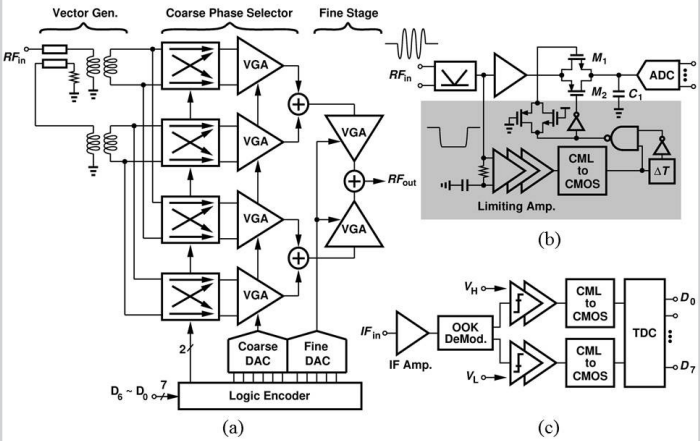


Figure 8.6.4: (a) 94GHz phase shifter, (b) power detector, (c) pulse detector.

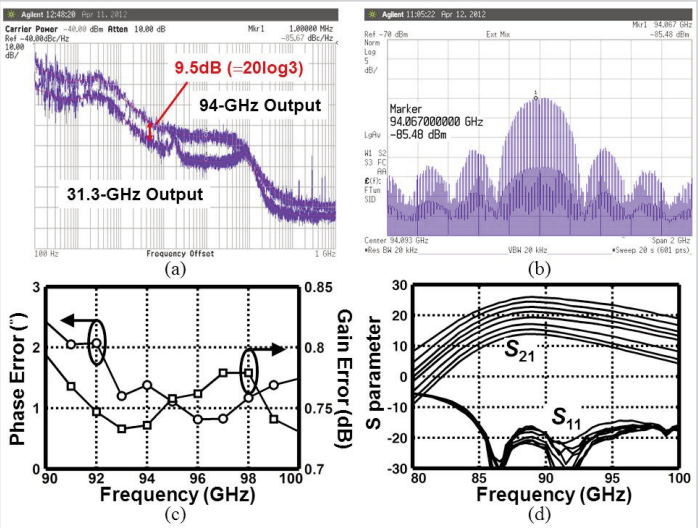


Figure 8.6.5: (a) Phase noise of 94GHz clock, (b) TX output spectrum, (c) phase and gain errors of phase shifter, (d) VGLNA gain.

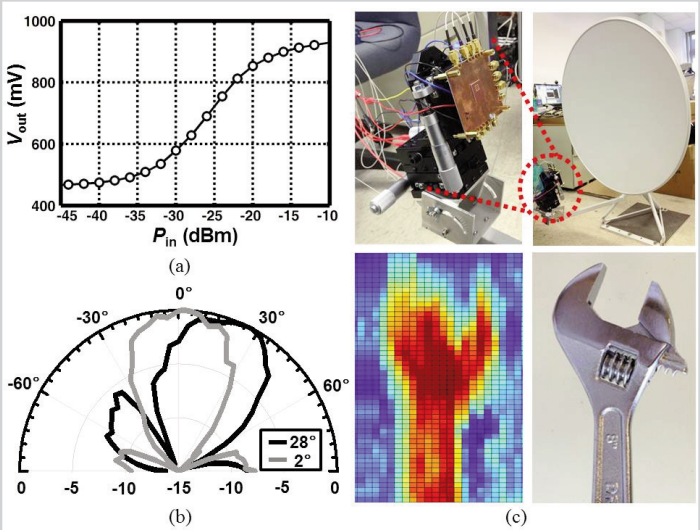
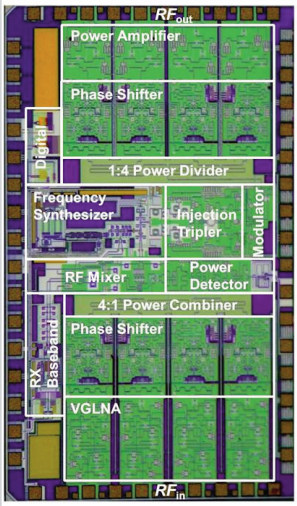


Figure 8.6.6: (a) Power detector responsivity, (b) patch antenna radiation pattern, (c) testing setup.



TX Performance		RX Performance	
S_{22}	−12dB	S_{11}	−15dB
PNoise @1MHz	−85.6dBc/Hz	Sensitivity	−45dBm
Ref. spur	<−42dBc	NF	10dB
P_{out}	−5dBm	Conv. Gain Range	27~40dB
Power Consumption	600mW	Power Consumption	360mW

3D Imaging Sensor	[3]	[4]	This Work
Frequency	144 GHz	600 GHz	94 GHz
Sensor Type	Phase Radar	FMCW	Pulse Radar
XY Resolution	3.3cm²@1m	0.2cm²@1m	5.4cm²@1m
Depth Resolution	0.76 cm	3.0 cm	1mm
Range	< 2m	4 – 25m	< 2m
Scanner	Mechanical	Mechanical	Electrical
Total Area	4.38 mm²	Discrete	7.6 mm²
Power Consumption	457mW	> 10W	960mW
Tech.	65nm CMOS	III-V HBT	65nm CMOS

Figure 8.6.7: Die micrograph and performance summary.

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