A Laser Ranging Radar Transceiver with Modulated Evaluation Clock in 65nm CMOS Technology

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Abstract

A novel ranging method utilizing modulated clock to count the time of flight (ToF) has been proposed. Substantially reducing the hardware and software complexity, this transceiver prototype achieves ranging resolution of less than 1.3mm while consuming only 50mW from a 1.2V supply.

I. Introduction

Pulsed laser has been used in ranging such as accurate positioning and automotive radars. It measures the time interval during which the laser pulse travels a round trip between the transceiver and the target. Conventional ranging technique calculates the ToF by counting cycles of a fixed-frequency clock, leading to limited resolution. For example, using a 2.5GHz clock as counting reference would introduce a maximum error of 400ps (or equivalently 6cm). This value is not sufficient for precise measurements. Other high accuracy approaches such as multiphase method require complex algorithm and circuit design. The ranging distance is also limited because the power of continuous lasers is much lower than that of the pulsed ones. This paper presents a pulsed laser radar based on continuously-tuned clocks produced by a fractional-*N* synthesizer, creating 1.5mm ranging accuracy. This novel approach provides a simple yet efficient solution for different ranging applications.

II. Radar Architecture

Figure 1 illustrates the proposed range finding algorithm. We here vary the counting clock frequency (≈2.5GHz) and repeat the measurement to narrow down the quantization error. For example, for a stationary object, if the first ToF measurement results in $N-1$ cycles of clock period T_1 and the second one gives rise to N cycles of clock period T_2, then the possible range must locate between NT_1 and NT_2 [Fig. 1(a)]. By the same token, we can substantially reduce the ranging error with different clock period. As shown in Fig. 1(b), if we continuously increase the counting clock period T, the actual ToF will locate between the "read-number line" (solid) and "the read-number + T line" (dashed). As a result, the possible solution can be easily found around the turn-around point, i.e., the tiny band which is always within the two boundary lines. The measuring resolution can therefore be shrunk by 1~2 orders.

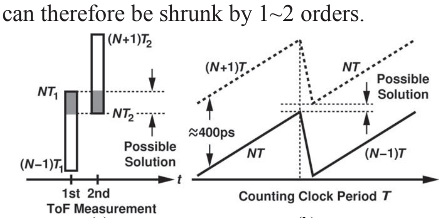


Fig. 1. Illustration of range finding by (a) 2 clock periods, (b) continuously-changing period.

Based on this observation, we implement a laser radar architecture as shown in Fig. 2. Here, a fractional-*N* frequency synthesizer provides the fundamental counting clock (≈2.5GHz). The synthesizer consists of an *LC* VCO, a ÷2 divider, a ÷24~31 prescaler driven by an 8-bit Σ-Δ modulator, a 3rd-order loop filter, a V/I converter, and a type-IV phase and frequency detector. The relatively high synthesizer frequency [$= f_{ref} \cdot (27 + M/2^8) \approx 2.5$GHz] reveals a basic accuracy of 6cm[1] in integer-*N* mode, and mm-level in fractional-*N* mode. A two-level pulse detector with calibration unit is proposed here to examine the arrival of incoming pulses. To minimize the deviation caused by walk error [1] and device offset, we adopt two-threshold method [2] and fore-ground calibration. Two 16-bit counters calculate the time interval from the pulse detector and send the digital results to the control logic for signal processing, which is realized in an FPGA prototype. The pulse detector and counter actually behave as a time-to-digital converter (TDC) with variable clock frequency.

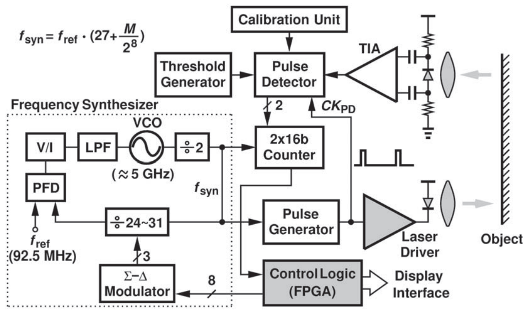


Fig. 2. Laser radar architecture (laser driver and lens are subject to change for different applications).

For high accuracy operation, the radar sweeps the counting clock period (i.e., the fractional-*N* divide modulus) to obtain the data of Fig. 1(b), and the FPGA logic yields the estimated ToF or distance accordingly. The sweeping of the frequency synthesizer is 100MHz. Since a pulsed laser's repetition rate is usually as high as several tens of kHz (e.g., 20kHz in IL30C [3]), a full-scale frequency scan can be accomplished within 100ms. The finer we alter the counting clock f_{syn}, the more precisely we can achieve. As demonstrated in Fig. 3(a), the rms error is almost inversely proportional to the number of sampling across the 100MHz range. For longer ranging distance, however, the counting results may wander 1 or 2 LSBs due to noise, which can be suppressed by averaging. Figure 3(b) shows the measured rms error as a function of averaging effect. For a given distance, if we repeat the sweeping process by more than 32 times, the rms error drops dramatically. For low-resolution applications such as automotive ranging, we can simply conduct one shot measurement and obtain an immediate result of 6cm resolution.

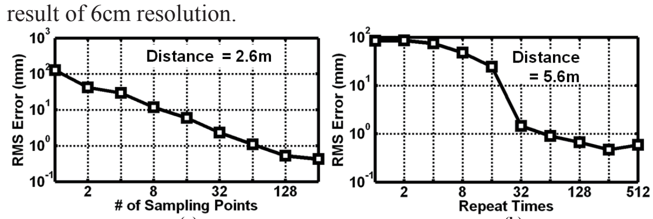


Fig. 3. Measured rms error as a function of (a) number of sampling points, (b) number of averaging.

[1] Roundtrip ToF.

Walk error, primarily caused by different crossover points for strong and weak return pulses, serves another source that introduces inaccuracy. Here, we adopt two-threshold method to eliminate this error. As shown in Fig. 4(a), the detected pulse coming from the TIA gets amplified by a two-stage preamplifier (voltage gain = 18dB), and is examined by two comparators with different threshold levels V_{TH1} and V_{TH2}. By calculating their crossover points t_1 and t_2, respectively, we obtain the initial point t_0 of the arrival time. That is, $t_0 = (t_1 V_{TH2} - t_2 V_{TH1}) / (V_{TH2} - V_{TH1})$. This value is independent of pulse rising slope, suppressing possible error caused by magnitude variation. The response of the TIA + preamplifier is shown in Fig. 4(b), presenting a gain of 99dBΩ and bandwidth of 300MHz.

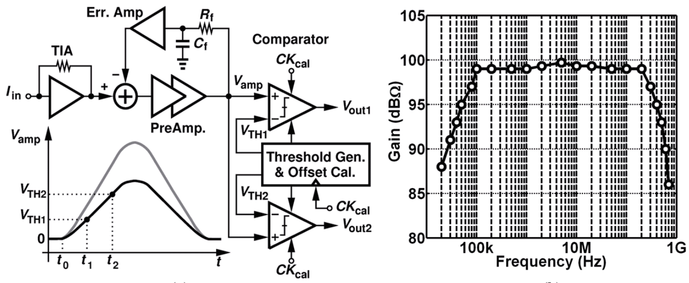


Fig. 4. (a) TIA + pulse detector (only single-ended is shown), (b) its response.

The above method proves useful only if the circuit has negligible offset in both the pre-amplifier and the comparator. A negative feedback path has been added around the pre-amplifier, which reduces the input-referred offset from $2.82\text{mV}_{\text{rms}}$ to $125\mu\text{V}_{\text{rms}}$. The comparators require delicate offset calibration as well. First, two threshold levels (artificial offsets) are generated symmetrically with respect to the common-mode level of V_{amp}. The comparators, as depicted in Fig. 5, are made of current-mode logics with current-steering calibration (M_5-M_{10}). The dual-differential amplifier M_1-M_4 together with loading R_1 creates a dc gain of 2.1dB with −3-dB bandwidth of 5.7GHz, and the degeneration resistor R_2 gentles the calibration adjustment. At power up, a calibration procedure is executed to cancel out the intrinsic offset of the comparators. Following the concept in [4], the comparator's inputs are shorted whereas the calibration unit, originally tilted to one side, increases the offset gradually until the output flips. At this moment, the circuit's asymmetry is fully compensated, and this result is therefore stored digitally. Note that to help digitize the output during calibration, we have an auxiliary comparator in the feedback loop, and its offset is corrected by the same procedure.

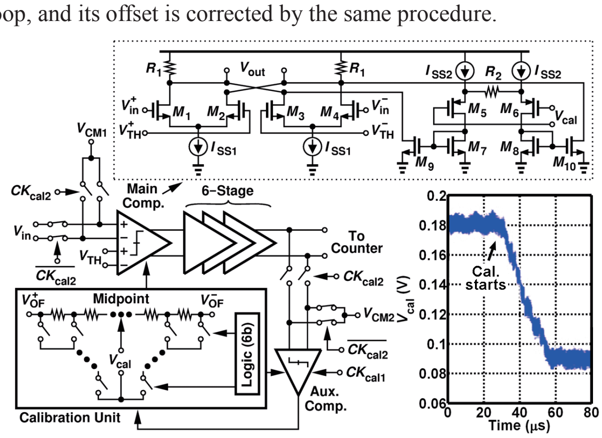


Fig. 5. Comparator and calibration unit.

The counter design involves a chain of dividers, which must be controllable and resettable. Shown in Fig. 6(a) is the proposed counter, where the first divider gets enabled when the ToF signal is high and stays in lock when it is low. To save power, the whole divider chain is made of static single-transistor-clocked structure [5]. Note that the long ripple (≈1ns) here is not an issue at all since the laser pulse comes every 50µs.

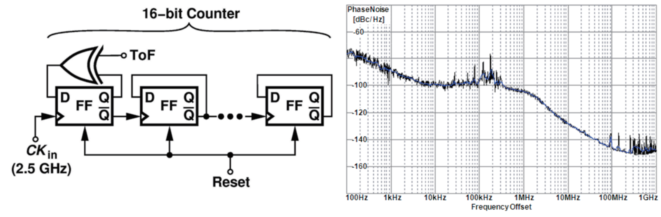
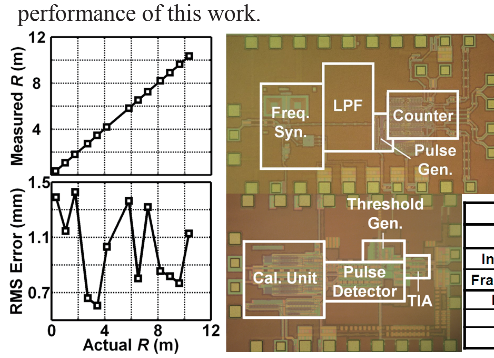


Fig. 6. (a) 16-bit counter, (b) measured output phase noise of the synthesizer in fractional-*N* mode.

III. Experimental Results

The radar transceiver has been designed and fabricated in 65nm CMOS technology. The transceiver consumes 50mW from a 1.2V supply. Figure 6(b) reveals the measured output phase noise of the 2.5GHz clock under fractional-*N* operation, suggesting phase noise of −104dBc/Hz at 1-MHz offset. The rms jitter integrated from 100Hz to 1GHz is approximately equal to 1.21ps. Using a broadband phase shifter to gradually increase the signal travel distance, we obtain the minimum detectable resolution as 8.8ps (or equivalently 1.3mm). Figure 7(a) shows the measured equivalent distance R and the corresponding rms error for 256 frequency points and average = 32 for each. Figure 7(b) depicts the die micrograph, which measures $2\times0.7\text{mm}^2$, and summarizes the performance of this work.



TIA + Pulse Detector	
Gain	99dBΩ
Bandwidth	300MHz
Freq. Synthesizer	
Freq.(GHz)	2.5~2.6
PNoise @1MHz	−104 dBc/Hz
RMS Jitter	1.21ps
Overall	
Resolution	
Integer-*N*	6cm
Fractional-*N*	1.3mm
Power	50mW
Area	2x0.7mm²
Tech.	65nm CMOS

Fig. 7. (a) Distance measurement result, (b) die micrograph and performance summary.

Acknowledgment

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