5.2 Subharmonically Injection-Locked PLLs for Ultra-Low-Noise Clock Generation

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High-speed low-noise clocks are essential in numerous applications. In this paper, complete analysis and validation of subharmonic injection locking that can substantially reduce the PLL phase noise at negligible cost is presented. Two 20GHz PLLs based on this technique demonstrate 149 and 85fs_{rms} jitter while consuming 38 and 105mW, respectively.

For an oscillator under fundamental injection locking, the phase noise within the lock range ω_L will be suppressed to that of the injection signal [1, 2]. It is thus deducible that for a subharmonic locking with a frequency ratio N, the phase noise inside the lock range ω_L would be constrained to $L_{inj}+20\log_{10}N$, where L_{inj} denotes the phase noise of the subrate injection signal CK_{inj}. Since usually the lock range of an LC-tank VCO is not only small but sensitive to PVT variations, the injection locking technique has to be combined into a PLL, i.e., forming a subharmonically injection-locked PLL. Generally, the lock range ω_L of the VCO is greater than the loop bandwidth (ω_{BW}), so a significant jitter reduction is expectable because the whole in-band noise is drawn down to $L_{inj}+20\log_{10}N$. As the offset frequency exceeds ω_L, the spectrum gradually deviates from the governance of L_{inj} and approaches the original phase noise of the PLL without injection locking (L_{PLL}). Beyond ω_{inj}, the noise here moves so fast that the injected signal has no chance to correct the phase. As a result, the phase noise would tightly follow L_{PLL} in this region. Figure 5.2.1(a) summarizes the analysis on the phase noise shaping, where the phase noise between ω_L and ω_{inj} is interpolated with a straight line. The rms jitter is thus readily available through the integration of it.

The above derivation can be fully verified by the previous CDR design in [3], which can perfectly function as a subharmonically injection-locked PLL. The output phase noise for the case $N=\omega_{out}/\omega_{inj}=8$ is shown in Fig. 5.2.2(a). It closely follows the $L_{inj}+20\log_{10}N$ line within the lock range and gradually returns back to L_{PLL} beyond ω_L as expected. Cases from $N=2$ to $N=64$ are examined to validate the accuracy of the model in Fig. 5.2.1(a). The average error is less than 5%.

The subharmonic-locking PLL reveals outstanding tolerance to PVT variations. Measurement suggests that for $N \le 8$, supply noise at any frequency below 100MHz (equipment limited) is fully rejected. In other words, with the help of injection locking, the PLL can be designed in more relaxed way and peripheral circuits such as supply regulators can be removed.

One issue hidden behind the beauty of the injection-locked PLLs is the possible conflict between the two locking forces; namely, the phase locking (from the reference PLL) and the injection locking (from the injection signal). In reality, the injection-locked PLL would automatically adjust the phase relationship to maintain the stability and accomplish the noise suppression. It can be proven that the maximum tolerable shift is given by $\pi+2\sin^{-1}(I_{inj,eff}/I_{osc})$ where I_{osc} and $I_{inj,eff}$ respectively denote the core and the effective injection currents of the VCO. By adjusting ΔT_1 in Fig. 5.2.1(b), the 210° safety region for the case $N=4$ and $I_{inj,eff}=I_{osc}/4$ is obtained. It can be shown that a fixed ΔT_1 is sufficient for the loop to stay stable over supply and temperature variations of ±10% V_{DD} and 85°C.

Two 20GHz PLLs are implemented to demonstrate the noise suppression technique. As shown in Fig. 5.2.3, the first circuit (chip A) is designed to provide a high divide ratio of 20 with minimum power consumption. To maintain an efficient subharmonic locking, a two-step locking of ×5 and ×4 sub-PLLs in cascade is implemented. Two pulse generators are responsible for creating injection signals whenever an input rising edge arrives. That is, CK_{out} is equivalently realigned to a clean edge once every 4 cycles. Two fixed delays ΔT_1 and ΔT_3 are placed in front of PLL_1 and PLL_2, respectively, to provide proper phases for injections. To minimize the power consumption, all dividers except the 20GHz one in PLL_2 are realized as true single-phase clocking (TSPC) topology. Note that the cascade structure can be extended to more stages to accommodate larger multiplication factors due to the low power and area penalty. For example, if the reference frequency is reduced to 250MHz and one more PLL stage is added in front, the power consumption would increase by 12%.

The pulse generator creates pulses with a width nominally equal to half the VCO clock period on occurrence of the rising edges of the reference. To save power, the power-hungry CML design in [3] is abandoned and the 20GHz pulse generator 2 is realized instead, as shown in Fig. 5.2.4(a). Combining CMOS and NMOS logics with reverse scaling, it produces 25ps injection pulses of approximately 600mV while consuming 1.15mW. The VCO design is shown in Fig. 5.2.4(b). Here, coupling pair M_3-M_4 receives the single-ended pulses at the gate of M_4, and injects a corresponding current into the LC tank. The device dimensions of M_1-M_2 and M_3-M_4 pairs as well as the bias circuit I_{b2}, M_5, and R_b define the injection strength. Static frequency dividers are used throughout the design. As presented in Fig. 5.2.4(c), the TSPC consumes at least 7× less power than CML at 10GHz. Thus, the 20GHz divider is realized with a class-AB CML flipflop, and the rest with TSPC flipflop. A 0.25mW CML-to-CMOS converter with 13GHz bandwidth is depicted in Fig. 5.2.4(d). The second circuit (chip B) is a modified version of that in [3]. It realizes 8× clock multiplication from 2.5 to 20GHz in one step, primarily attributed to the double-edge injection by means of an XOR gate.

The two 20GHz PLLs are fabricated in 90nm CMOS technology and tested on chip-on-board assemblies. Here, a low-noise signal generator SMA100A provides the reference input for both chips. In chip A, the 20 and 5GHz VCOs present tuning range of 940 and 700MHz, respectively, revealing a total operation of 940MHz. It consumes 38mW from a 1.3V supply, of which 12mW dissipates in PLL_1, 23mW in PLL_2, and 2.5mW in pulse generators. Figure 5.2.5(a) plots the phase noise of the 20GHz output with and without the subharmonic injection. The integrated rms jitter from 100Hz to 1GHz is 149fs. Chip B achieves an operation range of 0.5GHz while consuming 105mW from a 1.5V supply. The output phase noise is shown in Fig. 5.2.5(b), suggesting an integrated output jitter of 85fs. The phase noise at 1MHz offset of the two chips measures −113 and −123dBc/Hz, respectively. The recorded rms jitters as a function of temperature and supply voltage are plotted in Fig. 5.2.6(a). Without any manual tuning during the test, two circuits present robust locking and less than 33fs jitter deviation over 70°C and 200mV variations. Figure 5.2.6(b) compares the power consumption and jitter generation (integrated from 50kHz to 80MHz) of these two prototypes and other representative PLLs. Figure 5.2.7 shows the die micrographs, which measure $0.7\times0.65mm^2$ (chip A) and $0.65\times0.5mm^2$ (chip B) including pads, and a table summarizing the performance.

Acknowledgments:
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[2] B. Razavi, “A Study of Injection Locking and Pulling in Oscillators,” *IEEE J. Solid-State Circuits,* vol. 39, no. 9, pp. 1415-1424, Sep., 2004.
[3] Jri Lee and M. Liu, “A 20-Gb/s Burst-Mode Clock and Data Recovery Circuit Using Injection-Locking Technique,” *IEEE J. Solid-State Circuits,* vol. 43, no. 3, pp. 619-630, Mar., 2008.

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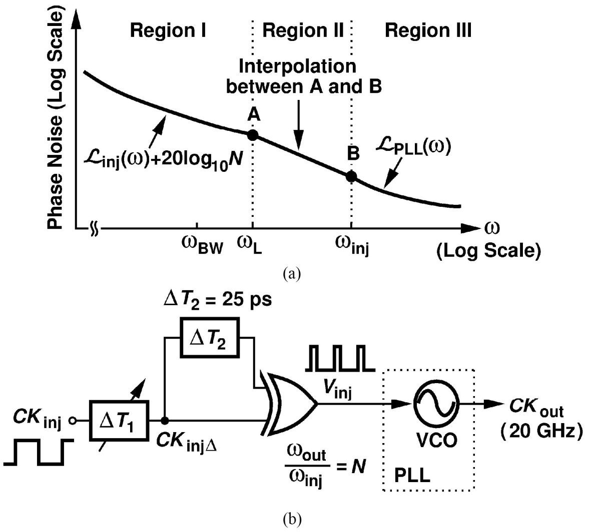


Figure 5.2.1: (a) Phase noise model of injection-locked PLLs, (b) redraw of the test circuit of [3].

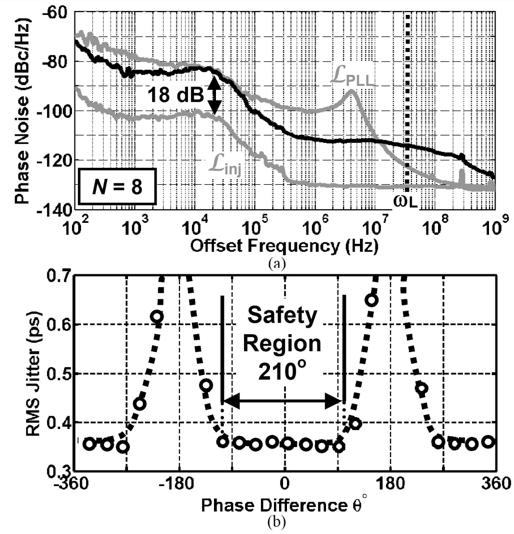


Figure 5.2.2: (a) Physical measurement of Fig. 5.2.1(b) for N=8, (b) measured jitter for N=4 and $I_{inj,eff}=I_{osc}/4$.

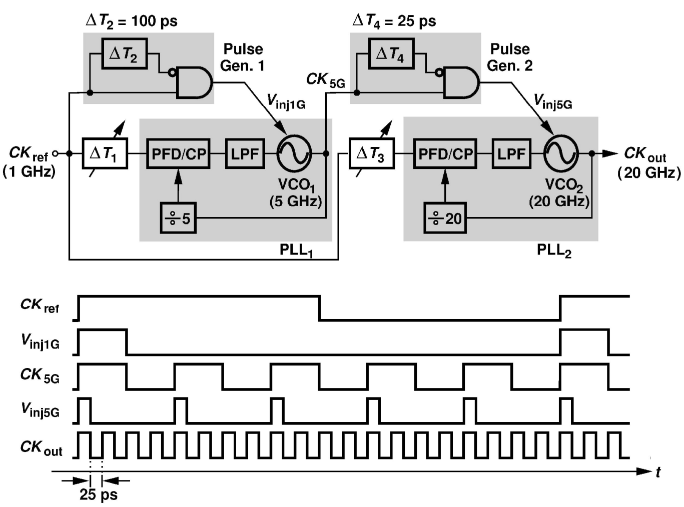


Figure 5.2.3: Chip A architecture and waveforms.

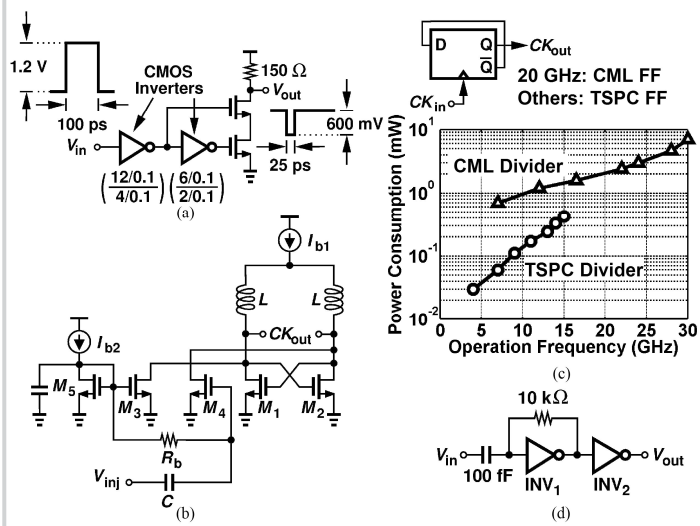


Figure 5.2.4: (a) Pulse generator for 20GHz clock, (b) 20GHz VCO, (c) power efficiency of static dividers, (d) CML-to-CMOS converter.

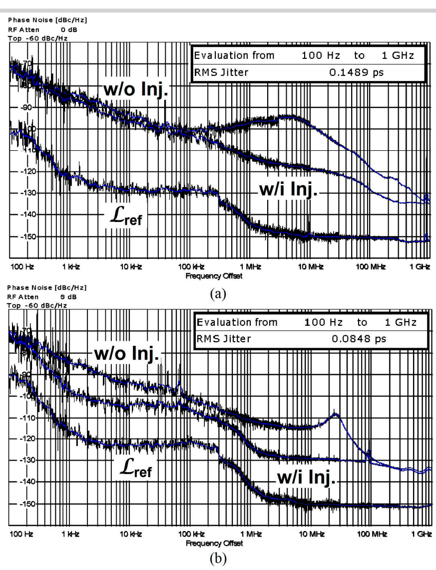


Figure 5.2.5: Measured phase noise of (a) chip A, (b) chip B.

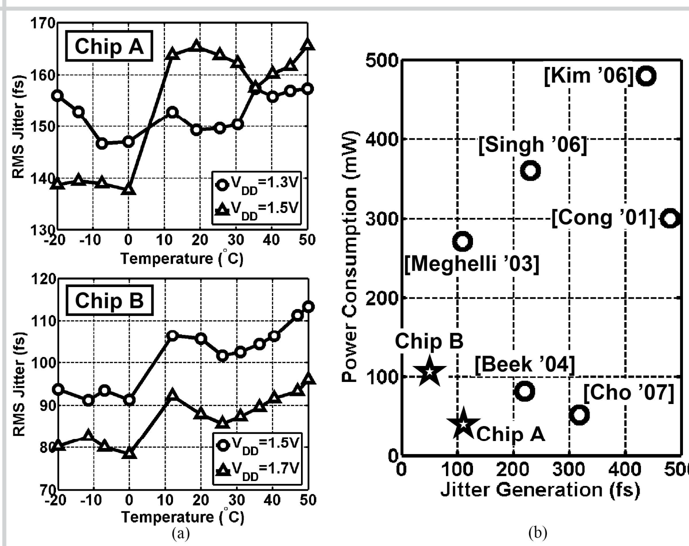
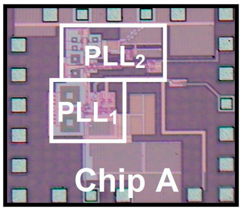


Figure 5.2.6: (a) Plot of rms jitter under supply and temperature variations, (b) performance comparison.

	[Kim '06]	[Meghelli '03]	Chip A	Chip B
Operation Freq.	20GHz	20GHz	20GHz	20GHz
Multiply Ratio	32	8	20	8
Phase Noise (@ 1–MHz Offset)	–101dBc/Hz	–108dBc/Hz	–113dBc/Hz	–123dBc/Hz
RMS Jitter				
100Hz~1GHz BW	650fs*	N/A	149fs	85fs
50kHz~80MHz BW	438fs**	110fs**	110fs	48fs
Supply Voltage	1.5V	–3.6V	1.3V	1.5V
Power Diss.	480mW	270mW	38mW	105mW
Lock Range	1800MHz	1800MHz	940MHz	500MHz
Loop Bandwidth	6.25MHz	3MHz	10MHz	8MHz
Chip Area	1.7mm^2	1.7 x 1.7mm^2	0.7 x 0.65mm^2	0.65 x 0.5mm^2
Technology	0.13-μm CMOS	SiGe BiCMOS	90-nm CMOS	90-nm CMOS

* Direct measurement in time domain. ** Calculated from the phase noise plots.



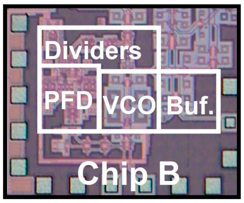


Figure 5.2.7: Chip micrograph and performance summary.