11.3 A 7-Band 3-8GHz Frequency Synthesizer with 1ns Band-Switching Time in 0.18μm CMOS Technology

Jri Lee, Da-Wei Chiu

National Taiwan University, Taipei, Taiwan

Frequency synthesizers for multi-band orthogonal frequency division multiplexing (MB-OFDM) systems need to provide a band-switching time on the order of nanoseconds [1], posing difficult challenges with respect to noise, sidebands, and power dissipation. Conventional phase-locked loop (PLL)-based synthesizers fail to provide such a fast switching due to their long settling time. The design and experimental verification of a fast hopping frequency synthesizer are presented in this paper. The frequency synthesizer generates clocks for 7 bands distributed from 3 to 8GHz with 1ns switching time.

The fast hopping characteristic can be achieved using a dual-loop architecture with single-sideband mixing. This architecture, however, requires accurate quadrature inputs and linear mixers. Moreover, as the number of bands increases, more intermediate frequency components need to be created, necessitating a large number of mixers and selectors. As a result, the unwanted sidebands of such components are "accumulated" through multi-stage mixing, substantially degrading the output signal. This added circuit complexity also results in a higher power consumption.

The above difficulties can be alleviated by using the topology shown in Fig. 11.3.1(a). A programmable tri-mode divider, capable of providing DC and quadrature signals of ω_1 with opposite I/Q sequences, is placed in front of one of the inputs of the SSB mixer. Such a configuration yields three programmable outputs, $\omega_2 \pm \omega_1$ and ω_2, with minimized hardware, reducing power consumption and undesired sidebands.

Based on the above observation, the architecture in Fig. 11.3.1(a) can be extended to accommodate the 7 bands of Group A and Group C in [1] with two selectors and one SSB mixer, as shown in Fig. 11.3.1(b). Here, the group PLL generates the center frequencies of 6.864 GHz (Band 5) and 3.432 GHz (Band 1), whereas the band PLL produces twofold the incremental frequencies, 2.112 GHz and 1.056 GHz, for frequency additions and subtractions. The subsequent tri-mode divider provides DC or quadrature signals with different I/Q sequences of f_B or $2f_B$ (f_B = 528 MHz), allowing the SSB mixer to create up to 10 synthesized frequencies. Since only one SSB mixer is used, the effect of nonidealities due to mismatches in the signal path and the mixer itself is considerably reduced.

The SSB mixer incorporates band-pass loads and double degeneration technique to suppress sidebands. As illustrated in Fig. 11.3.2(a), two identical SSB mixers with different inductive loads are used to achieve broadband operation. Sharing the same tail current to save power, these two SSB mixers are dedicated to Group A and Group C, respectively. Band selection is accomplished by adding capacitor arrays to change the tank resonance frequency [Fig. 11.3.2(b)]. The on-resistance of the band-selection switches in series with the capacitors is chosen to yield a capacitor Q of greater than 15. To improve linearity, the mixers employ source degeneration technique in both LO and RF ports [Fig. 11.3.2(b)]. Here, R_1-R_4 linearize the LO port switches M_1-M_8 with no voltage headroom consumption, splitting the RF port into 8 devices, M_9-M_{16}. These devices are also degenerated by R_5-R_8 in series with the on-resistance of the group selection switches M_{17}-M_{20}. Simulation shows that this topology achieves at least 6dB lower sidebands as compared with the structure in [2], which is redesigned in CMOS with the same power dissipation and operation frequency. Note that the loading inductor L_1 of the Group A mixer is approximately 4 times larger than that of the Group C mixer. Thus, for a given tank Q, the former exhibits a parallel resistance that is twice as much as that of the latter, and the output amplitude is expected to change by a factor of 2 during group switching.

The SSB mixer requires quadrature inputs so as to perform frequency additions and subtractions. In contrast to a phase shifter that operates only for narrow bands, a static frequency divider manifests itself in providing quadrature outputs across a wide frequency range. Realizing that the output phase sequence of a conventional divide-by-2 circuit is uniquely determined by the routing between the drains and gates of M_1-M_4 [Fig. 11.3.3(a)], the divider is modified by combining two opposite routing configurations. This leads to two possible output sequences, namely, clockwise (CW) and counterclockwise (CCW). Furthermore, the generation of DC signals can be also merged into the divider, which results in the tri-mode divider depicted in Fig. 11.3.3(b). The mode switching is accomplished by steering the tail current I_{SS1}, and the cross-coupled pairs are off while the circuit is producing DC signals.

Figure 11.3.4(a) shows the quadrature VCO, which employs two coupled LC oscillators along with MOS varactors. Modified from [3], this circuit uses common-source structures M_1-M_4 and M_5-M_8 to minimize the effect of device mismatches. Simulation shows that the proposed VCO displays a phase and amplitude error of 1.5% and 0.7%, respectively, in the presence of a 5% device mismatch; this is 2 to 3 times improvement compared to conventional quadrature topologies. The selector is depicted in Fig. 11.3.4(b), where two dummy pairs M_5-M_6 and M_7-M_8 are introduced to cancel out the undesired coupling to the first order while consuming no extra power. The divide-by-13 circuit in the group PLL block consists of a synchronous divide-by-3/4 circuit followed by two asynchronous divide-by-2 circuits. The OR-AND-flipflop in the divide-by-3/4 circuit uses complementary current-mode logic, avoiding the bias voltage necessary in the earlier realization [4].

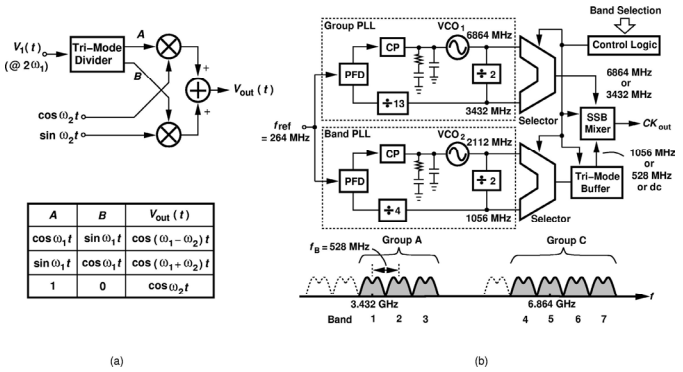
The frequency synthesizer has been fabricated in a 0.18μm CMOS technology. The chip micrograph is shown in Fig. 11.3.7. The die area is 1.3×1.1mm^2. The outputs are designed as 50Ω microstrip structures consisting of metal-6 atop metal-1. Phase and gain mismatches between internal signals are minimized through symmetry in layout. The circuit is tested on a chip-on-board assembly while running from a 2.2V supply. Note that in steady-state operation, none of the devices experiences more than 1.8V across it.

The VCOs in the group and band PLLs [VCO_1 and VCO_2 in Fig. 11.3.1(b)] achieve a tuning range of 900 and 470MHz, and a free-running phase noise of –110 and –116dBc/Hz at 1MHz offset, respectively. The worst sideband performance occurs at Band 4 (6.336GHz). Figure 11.3.6 depicts the spectrum of this band, suggesting a sideband rejection of 37dB. The band-switching behavior is shown in Fig. 11.3.5, where the bands are switched periodically and the synthesizer output is monitored. The longest settling time is approximately equal to 1ns, a value much less than the 9.5ns defined in [1].

Acknowledgments:
This work was supported in part by MediaTek, and National Science Council (NSC). The authors thank Chip Implementation Center (CIC) for chip fabrication, and Chorng-Kuang Wang and Shen-Iuan Liu for measurement support.

References:
[1] Anuj Batra et al., Multi-Band OFDM Physical Layer Proposal, doc. IEEE 802.15-03/267r5, July, 2003.
[2] Ting-Ping Liu, "A 2.7-V Dual-Frequency Single-Sideband Mixer," *Symp. VLSI Circuits,* pp. 124-127, June, 1998.
[3] Ting-Ping Liu, "A 6.5GHz Monolithic CMOS Voltage-Controlled Oscillator," *ISSCC Dig. of Tech. Papers,* pp. 404-405, Feb., 1999.
[4] C. Lam and B. Razavi, "A 2.6-GHz/5.2-GHz Frequency Synthesizer in 0.4μm CMOS Technology," *IEEE J. Solid-State Circuits,* vol. 35, no. 5, pp. 788-794, May, 2000.

 0-7803-8904-2/05/$20.00 ©2005 IEEE.



A	B	$V_{out}(t)$
$\cos\omega_1 t$	$\sin\omega_1 t$	$\cos(\omega_1-\omega_2)t$
$\sin\omega_1 t$	$\cos\omega_1 t$	$\cos(\omega_1+\omega_2)t$
1	0	$\cos\omega_2 t$

Figure 11.3.1: Proposed frequency synthesizer (a) conceptual illustration, (b) architecture.

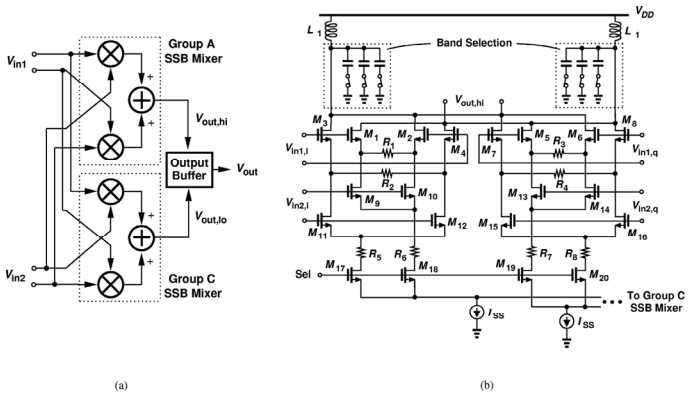


Figure 11.3.2: (a) SSB mixer architecture, (b) realization of Group A mixer.

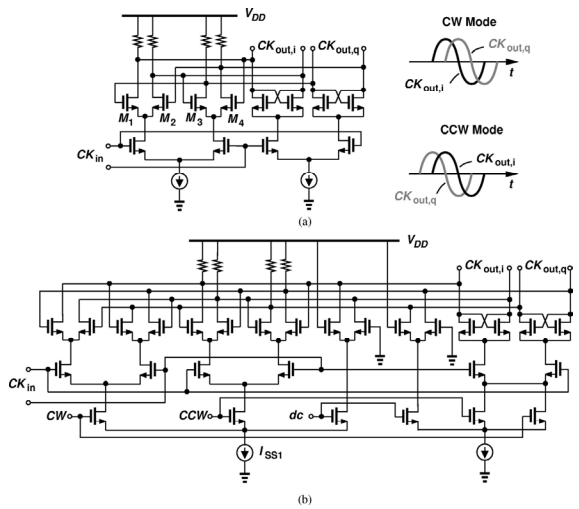


Figure 11.3.3: (a) Conventional static divide-by-2 circuit, (b) proposed tri-mode divider.

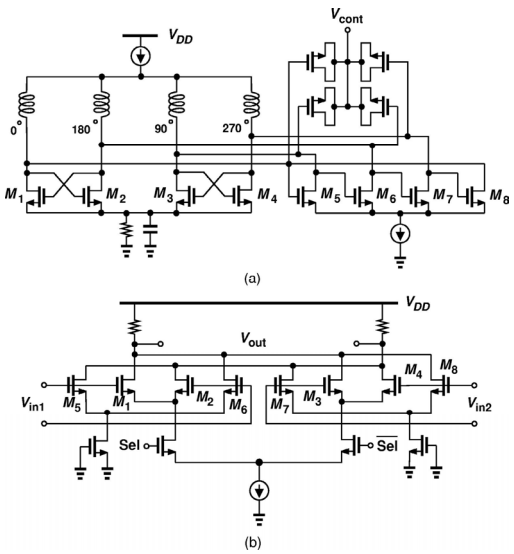


Figure 11.3.4: (a) Quadrature VCO, (b) selector.

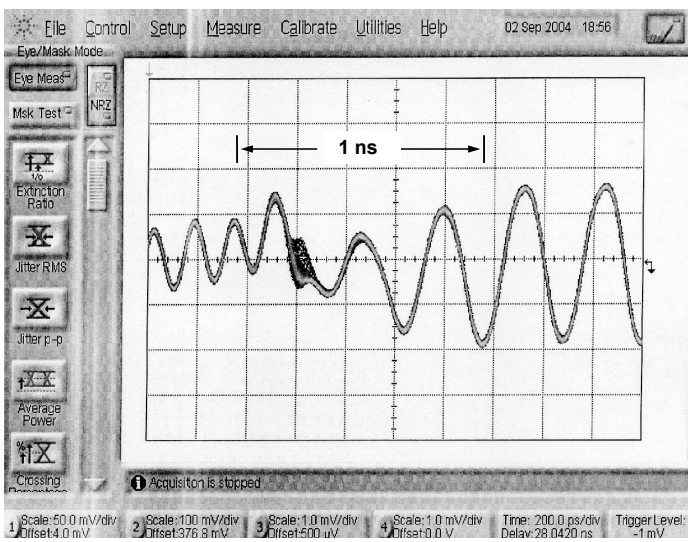


Figure 11.3.5: Band-switching behavior (from Band 4 to Band 1).

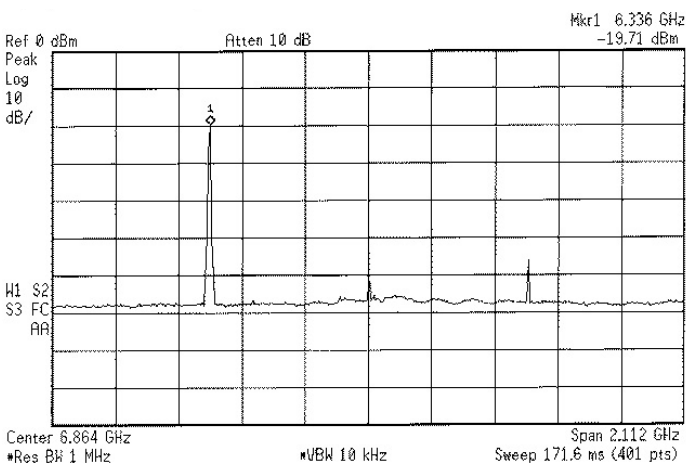


Figure 11.3.6: Output spectrum of Band 4.

Continued on Page 593

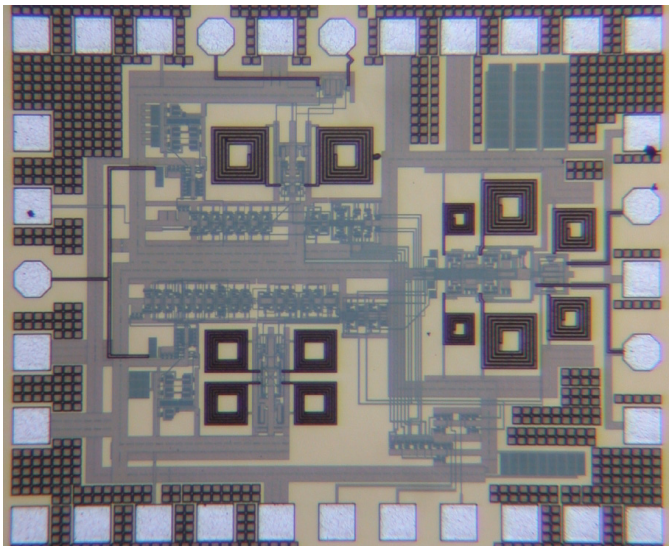


Figure 11.3.7: Chip micrograph.

 0-7803-8904-2/05/$20.00 ©2005 IEEE.