A 3-to-8-GHz Fast-Hopping Frequency Synthesizer in 0.18-μm CMOS Technology

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***Abstract*—A frequency synthesizer incorporating one single-sideband (SSB) mixer generates seven bands of clock distributed from 3 to 8 GHz with 1-ns switching time. An efficient frequency synthesizing technique producing balanced bands around one center frequency is employed, and the SSB mixer uses double degeneration topology to increase the linearity. Fabricated in 0.18-μm CMOS technology, this circuit achieves a sideband rejection of 37 dB while consuming 48 mW from a 2.2-V supply.**

***Index Terms*—Frequency synthesizer, phase-locked loop (PLL), single-sideband (SSB) mixer, ultra-wideband (UWB).**

I. Introduction

ULTRAWIDE-BAND (UWB) systems using multiband orthogonal frequency division multiplexing (MB-OFDM) technique require frequency synthesizers to provide multigigahertz clocks with a band switching time on the order of nanoseconds [1], posing difficult challenges with respect to noise, sidebands, and power dissipation. Conventional phase-locked loop (PLL)-based synthesizers are simply ill-suited due to the long settling times, which are typically tens of microseconds.

This paper presents the design and experimental verification of a fast-hopping frequency synthesizer that generates clocks for the seven bands in Mode 2 operation in [1] distributed from 3 to 8 GHz with a switching time of less than 1 ns. The proposed topology provides a simple yet efficient method of frequency synthesis that creates symmetric numbers of bands above and below a center frequency. Only one single-sideband (SSB) mixer is used in this prototype. Fabricated in 0.18-μm CMOS technology, this work achieves a phase noise of -103 dBc/Hz at 1-MHz offset and 37-dB sideband rejection while consuming 48 mW from a 2.2-V supply. This architecture could be further extended with minor changes to accomplish a full coverage of the 14 bands denned in a newer proposal [2].

Section II develops the foundation and architecture of the proposed synthesizer. Section III presents the transistor-level design of each building block, and Section IV summarizes the experimental results.

II. Architecture

The development of the UWB systems has invoked researches on fast-hopping frequency synthesizers, and numbers of methods have been reported to achieve a band switching time less than the 9.5-ns guard interval. The circuit in [3] incorporates modified Miller divider to selectively alter the regenerated output. The generators in [4] and [5] employ DLL-based multiplier and semi-dynamic divider to synthesize the desired frequencies. However, none of these ideas can be easily extended to cover more bands. The work in [6] uses quadrature clock source of twice the highest frequency ($\approx$16 GHz) and two stages of SSB mixing to generate the seven bands in Mode 2. The higher required operation frequency of the quadrature VCO necessitates a relatively advanced process. Meanwhile, the number of SSB mixers in such a direct frequency synthesizer should be minimized, otherwise more intermediate frequency components would be created, accumulating unwanted sidebands at the output. The proposed example circuit in [1] is unrealistic since it necessitates five SSB mixers in order to accommodate the seven bands in Mode 2. The circuit in [7] dedicates one PLL to each band. This topology is also difficult to be applied to more bands since the required area and power dissipation would soon become unacceptable.

To resolve the above difficulties, we propose a new topology that synthesize evenly distributed frequency components with minimum circuitry. The concept is illustrated as shown in Fig. 1. A programmable buffer is placed in front of one input of the SSB mixer. If this buffer provides quadrature signals of ω_1 with two opposite phase sequences, two possible frequencies, $\omega_1 \pm \omega_2$, can be synthesized. Similarly, an output frequency of ω_2 is created if the buffer provides a DC signal. As a result, such a configuration yields three programmable outputs equally spaced by ω_1, minimizing the hardware requirement, power consumption, and undesired sidebands. In practice, the tri-mode buffer is realized as a modified static frequency divider, owing to its nature of generating quadrature outputs. The tri-mode divider design is described in Section III-C.

This topology can be easily improved to cover more bands. As shown in Fig. 2, the proposed architecture can accommodate seven bands distributed from 3 to 8 GHz with only one SSB mixer. Here, the center PLL (PLL_1) generates the center frequencies of 6.864 GHz (Band 5) and 3.432 GHz (Band 1), whereas the incremental PLL (PLL_2) produces twofold the incremental frequencies, 2.112 and 1.056 GHz, for frequency addition and subtraction. The subsequent tri-mode divider provides DC or quadrature output signals with different phase sequences of f_B or $2f_B$ ($f_B = 528$ MHz), allowing the SSB mixer to create up to 10 synthesized band frequencies. That is, each center frequency has five bands spanned symmetrically around it. Since only one stage of SSB mixing is involved, the effect of nonidealities due to mismatches in the signal path and the mixer itself can be considerably reduced.

It is interesting to consider the compatibility of the proposed topology to other band plans. The UWB band plan proposed in [2] defines 14 evenly distributed bands from 3.1 to 10.6 GHz

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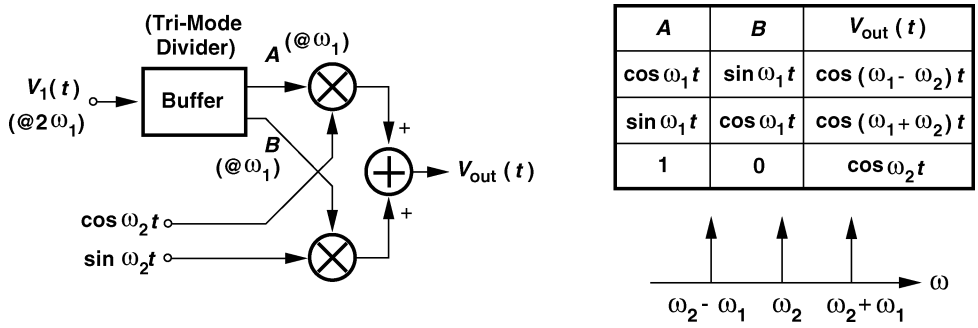

Fig. 1. Conceptual illustration of synthesizing three frequency bands.

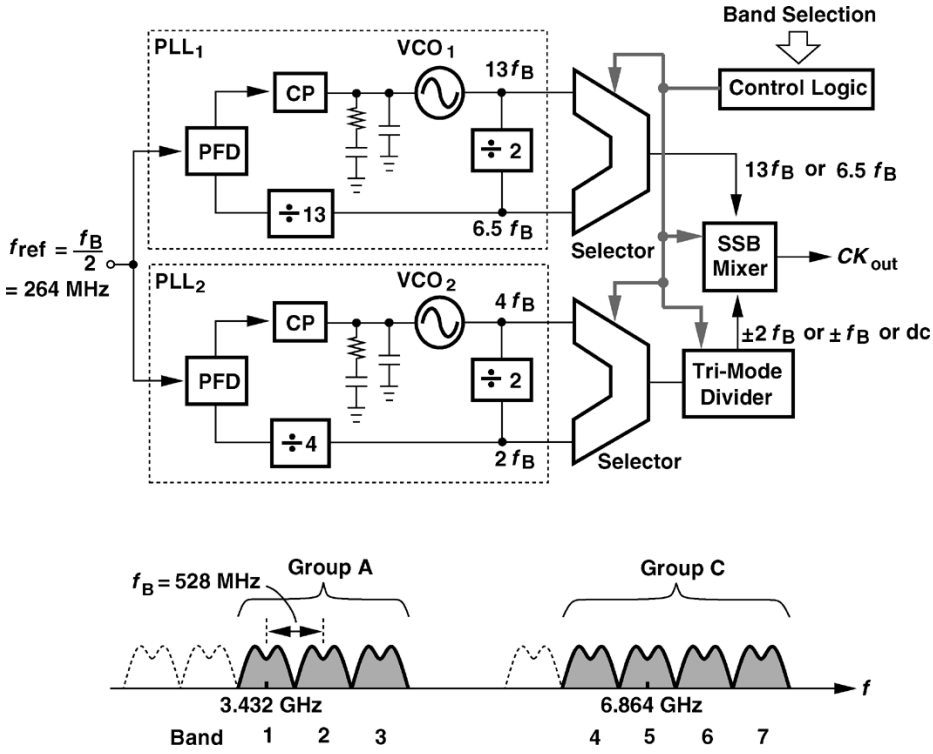

Fig. 2. Proposed synthesizer architecture.

without any gap in between. The architecture in Fig. 2 can be modified with minor changes (e.g., one additional SSB mixer) to accommodate all bands. Fig. 3 depicts an example. Here, SSB Mixer$_A$ along with a tri-mode divider creates three center frequencies, 7.5 f_B, 12.5 f_B, and 17.5 f_B,[1] whereas the same structure as that in Fig. 2 generates the incremental components (i.e., $\pm 2f_B$, $\pm f_B$, and 0). The two signals are combined by means of the SSB Mixer$_B$, producing up to 15 frequency components. The full coverage of the 14 bands is therefore achieved with the first band omitted. Note that none of the architectures in [3]–[7] can be easily extended to 14 bands without major changes.

III. Building Blocks

A. SSB Mixer

The performance of an SSB mixer is heavily influenced by the mismatches between the two input paths. To evaluate the sideband caused by mismatches, we consider an imperfect SSB mixer shown in Fig. 4. The two inputs present gain mismatches of ϵ_1 and ϵ_2, and phase imbalance of θ_1 and θ_2, respectively. Meanwhile, the gain mismatch between the two mixers is denoted as ϵ_k. The output is thus equal to

$$v_{\text{out}}(t) = kA_iA_2\cos\omega_1 t\cos\omega_2 t \tag{1}$$

$$+ k(1+\epsilon_k)A_i(1+\epsilon_1)A_2(1+\epsilon_2) \times \sin(\omega_1 t+\theta_1)\sin(\omega_2 t+\theta_2) \tag{2}$$

where A_1 and A_2 represent the input amplitudes and k the mixer gain. Denoting $C_1 = kA_1A_2$ and $C_2 = k(1+\epsilon_k)A_1(1+\epsilon_2)A_2(1+\epsilon_2)$, we arrive at

$$v_{\text{out}}(t) = C_1\frac{\cos(\omega_1+\omega_2)t+\cos(\omega_1-\omega_2)t}{2} \tag{3}$$

$$+C_2\frac{\cos[(\omega_1-\omega_2)t+\theta_1-\theta_2]+\cos[(\omega_1+\omega_2)t+\theta_1+\theta_2]}{2}. \tag{4}$$

[1]A few techniques can be used to implement the divide-by-2.5 function in PLL$_1$. For example, the semi-dynamic structure in [5].

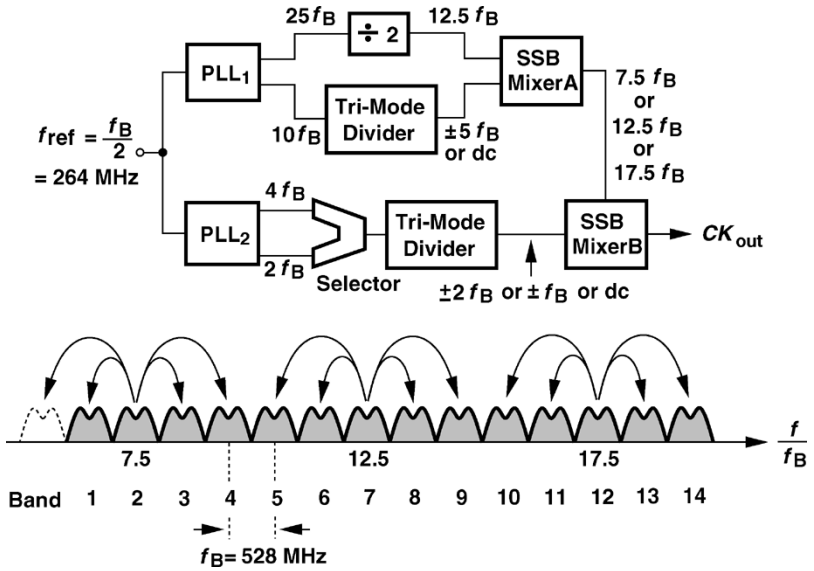

Fig. 3. Synthesizer modified to cover 14 bands.

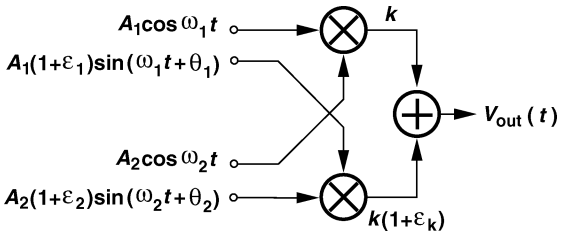

Fig. 4. SSB mixer with mismatches.

Thus, the image sideband at $\omega_1+\omega_2$ is given by

$$v_{im}(t)=\frac{C_1}{2}\cos(\omega_1+\omega_2)t - \frac{C_2}{2}\cos[(\omega_1+\omega_2)t+\theta_1+\theta_2] \quad (5)$$

$$=\sqrt{k_1^2+k_2^2}\cos[(\omega_1+\omega_2)t-\alpha] \quad (6)$$

where $k_1=[C_1-C_2\cos(\theta_1+\theta_2)]/2$, $k_2=C_2\sin(\theta_1+\theta_2)/2$, and $\alpha=\tan^{-1}(k_2/k_1)$. Similarly, the desired signal at $\omega_1-\omega_2$ can be expressed as

$$v_{sig}(t)=\frac{C_1}{2}\cos(\omega_1-\omega_2)t + \frac{C_2}{2}\cos[(\omega_1-\omega_2)t+\theta_1-\theta_2] \quad (7)$$

$$=\sqrt{k_3^2+k_4^2}\cos[(\omega_1-\omega_2)t+\beta] \quad (8)$$

where $k_3=[C_1+C_2\cos(\theta_1-\theta_2)]/2$, $k_4=C_2\sin(\theta_1-\theta_2)/2$, and $\beta=\tan^{-1}(k_4/k_3)$. The sideband rejection caused by mismatches is readily obtained as

$$\text{Sideband Rejection(dB)} = 10\log_{10}\frac{k_3^2+k_4^2}{k_1^2+k_2^2} \quad (9)$$

$$=10\log_{10}\frac{1+2\frac{C_2}{C_1}\cos(\theta_1-\theta_2)+(C_2^2/C_1^2)}{1-2\frac{C_2}{C_1}\cos(\theta_1+\theta_2)+(C_2^2/C_1^2)}. \quad (10)$$

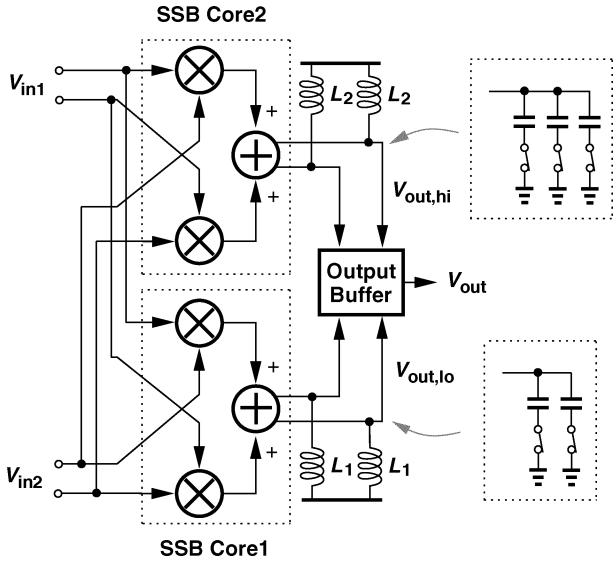

Fig. 5. Proposed wideband SSB mixer.

As expected, the image sideband of an SSB mixer is a function of phase and gain errors. For example, if $\theta_1=1^\circ$, $\theta_2=0^\circ$, and $C_2/C_1=0.1$ dB, an SSB mixer would present a image sideband of -39.6 dBc.

In addition to mismatches, nonlinearities in the SSB mixer itself also induce sidebands. While the mismatches create image sidebands, the nonlinearities produce spurs all over the spectrum due to cross-products of the input harmonics. Conventional SSB mixer designs usually employ source (emitter) degeneration technique in the RF port to increase the linearity [8]. However, the abrupt switching of the LO port still converts its harmonics to sidebands. Such unwanted sidebands degrade the output signal integrity. Meanwhile, the resistive loads in traditional designs present no filtering on sidebands [8], creating significant jitters and distortions in the output.

The architecture introduced here incorporates bandpass loads and double degeneration technique to suppress sidebands. As illustrated in Fig. 5, two identical SSB mixer cores with different

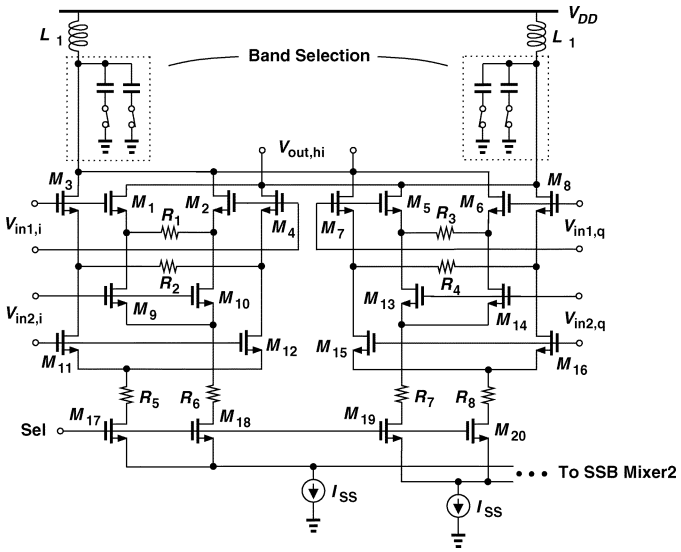

Fig. 6. Realization of SSB Core1 in Fig. 5.

inductive loads are used to achieve broadband operation. The SSB Core1 and SSB Core2 are dedicated to low and high group (Group A and C in Fig. 2), respectively, and only one core is active at a time. Band selection is accomplished by adding capacitor arrays to change the resonance frequency of the tanks. The on-resistance of the band selection switches in series with the capacitors is chosen to yield a capacitor Q of greater than 15.

The mixer cores employ source degeneration technique in both LO and RF ports (Fig. 6) to further improve the linearity. Here, R_1–R_4 linearize the LO port switches M_1–M_8 with no voltage headroom consumption, splitting the RF port into 8 devices, M_9–M_{16}. These devices also get degenerated by R_5–R_8 in series with the on-resistance of the group selection switches $M_{17}-M_{20}$. Fig. 7 shows the output spectra of SSB mixers with and without the RF and LO degeneration. The two circuits are simulated with the same operation frequency and power consumption. The highest spurs actually occurs at $f_{\rm LO}-3f_{\rm RF}$, resulting from the mixing of the LO signal and the third-order harmonic of the RF signal. The double degeneration technique suppresses this highest harmonic spur by 14 dB and the LO feedthrough by 10 dB. Note that no image sideband can be observed, since the SSB mixers here are of perfect symmetry. Monte Carlo simulation reveals that the device mismatch of the SSB mixer causes an image sideband of -45 dBc.

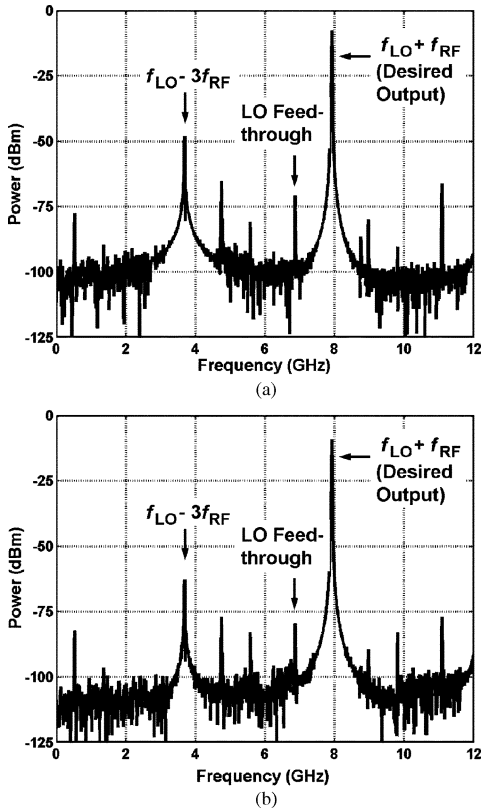

Fig. 7. Simulated spectra of SSB mixers (a) without and (b) with the LO and RF degenerations.

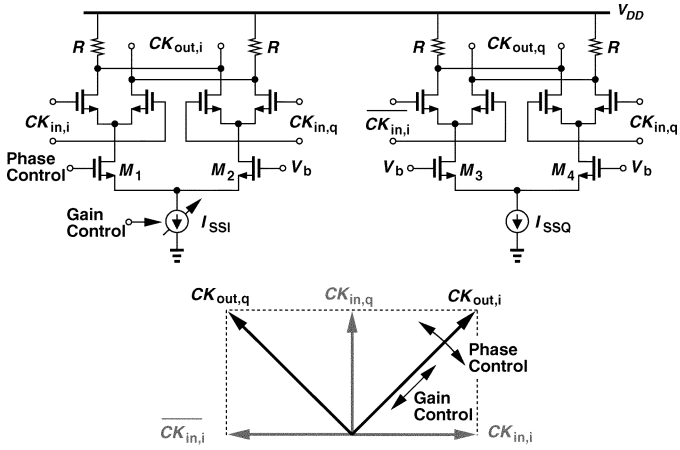

Fig. 8. Quadrature clock buffer with adjustable phase.

B. Clock Buffer

To generate the quadrature clocks, antiphase-coupled VCOs are incorporated in this design with proper choice of coupling factor so as to minimize the phase noise. However, this commonly used topology inevitably introduces finite phase and gain errors due to the device mismatches and routing asymmetries. Such imperfections result in sidebands in the output directly (Section III-A).

An interpolating buffer is employed here to counterbalance these errors. As shown in Fig. 8, two identical buffers driven by the in-phase (0°) and quadrature-phase (90°) clocks produce two clock outputs ($\rm CK_{out,}$$_i$ and $\rm CK_{out,}$$_q$), nominally equal to 45° and 135°, respectively. Here, the phase of $\rm CK_{out,}$$_i$ is adjustable, and the tuning is accomplished by steering the tail current $I_{\rm SSI}$ to alter the weighting factors of the two inputs. Since the phase of $\rm CK_{out,}$$_q$ remains fixed, the buffer presents a maximum phase tunable range of $\pm 45°$. Similarly, the gain error can be eliminated by adjusting the tail current $I_{\rm SSI}$ (nominally equal to $I_{\rm SSQ}$), arriving at quadrature outputs with balanced magnitudes. Note that in this prototype, both phase and gain errors are calibrated manually for simplicity. Calibration technique such as [9] is applicable in future designs to correct the phase and gain errors automatically at power up and allow continuous operation thereafter.

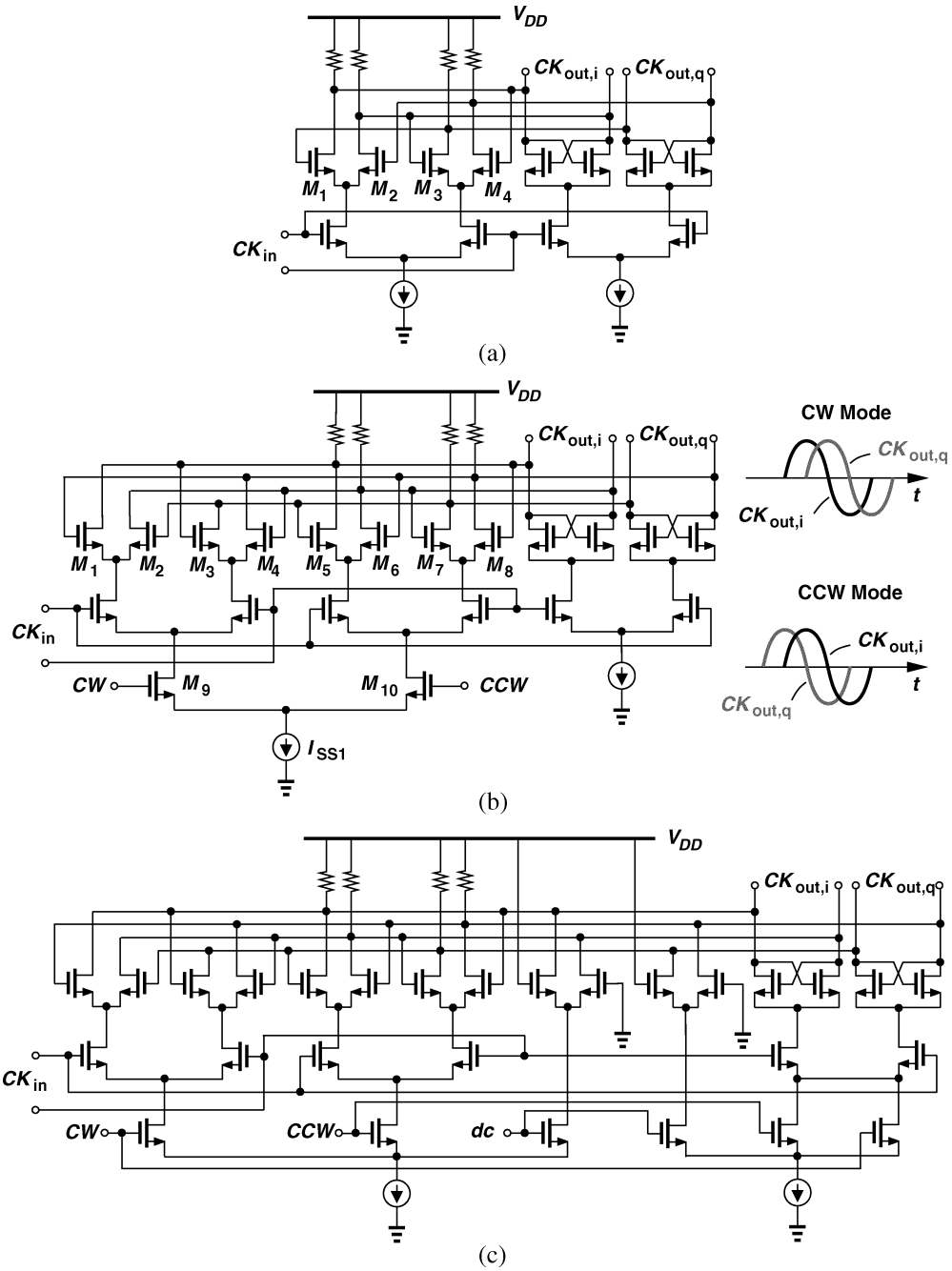

Fig. 9. Evolution of tri-mode buffer.

C. Tri-Mode Divider

The SSB mixer requires quadrature inputs so as to accomplish frequency addition and subtraction. In contrast to a phase shifter that operates only for narrow bands, a static frequency divider manifests itself in providing quadrature outputs across a wide frequency range.

Consider a conventional divide-by-2 circuit with a current-steering flip-flop (FF), as shown in Fig. 9(a). Recognizing that the output phase sequence is uniquely determined by the routing among the drains and gates of M_1–M_4, we modify the divider by combining two different routing configurations, as illustrated in Fig. 9(b). It leads to two opposite phase sequences, namely, clockwise (CW) and counterclockwise (CCW), and the sequence switching is accomplished by steering the tail current I_{SS1} through M_9 and M_{10}. The generation of DC signals can be also merged into the divider by introducing one more current-steering branch, arriving at a tri-mode divider circuit as depicted in Fig. 9(c). Note that the cross-coupled pairs are turned off to minimize perturbation while the circuit is producing DC signals. Such a configuration combines the three operation modes without extra power consumption.

D. Divide-by-13 Circuit

The divide-by-13 circuit in Group PLL consists of a synchronous $\div 3/4$ circuit followed by two asynchronous divide-by-2 circuits [Fig. 10(a)]. The current-mode logic (CML) flip-flops and NOR gate provide differential outputs, allowing a complementary operation in the OR-AND flip-flop [Fig. 10(b)].

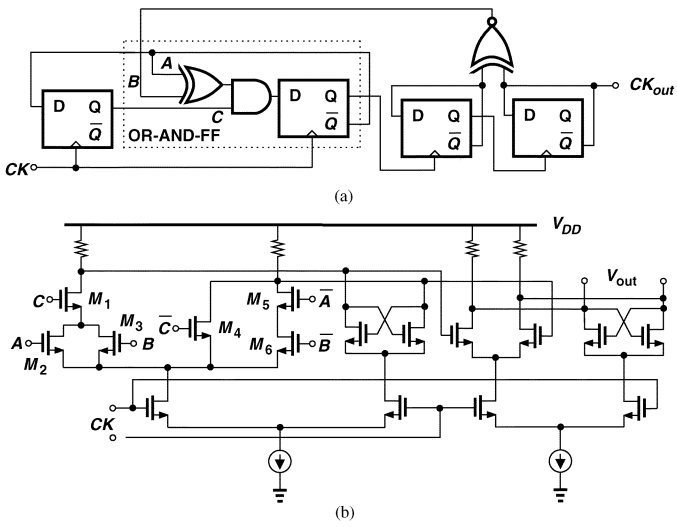

Fig. 10. (a) Divide-by-13 circuit, (b) realization of OR-AND-flip-flop.

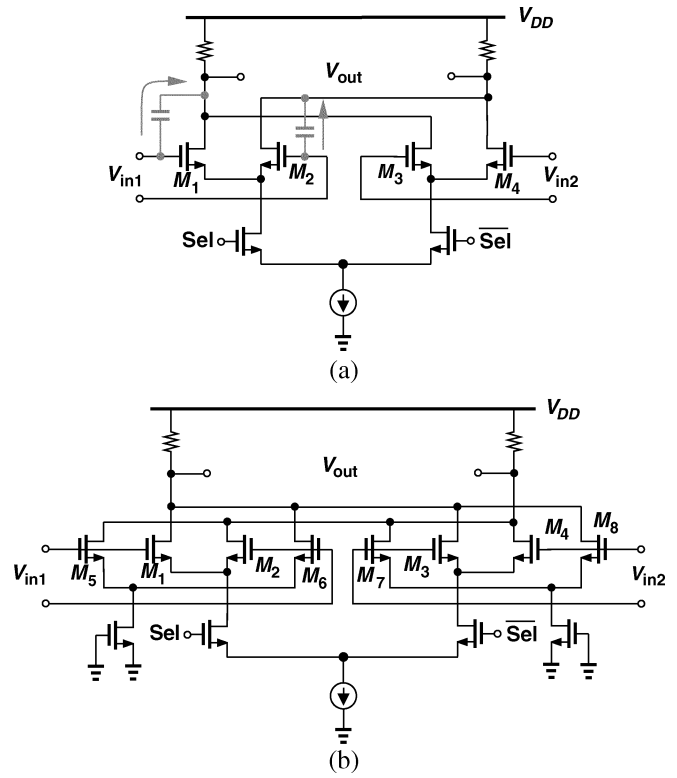

Fig. 11. (a) Conventional selector, (b) proposed selector with coupling cancellation technique.

Such a circuit avoids the bias voltage necessary in the earlier realization [10]. The circuit is designed to provide a sufficient speed with minimum power consumption, although it can operate with an input frequency as high as 10 GHz while burning more power.

E. Selector

A selector must provide fast switching and symmetry with respect to its two inputs. A conventional current-steering selector may suffer from undesired modulation, since the unselected signal in the disabled pair would still couple to the output

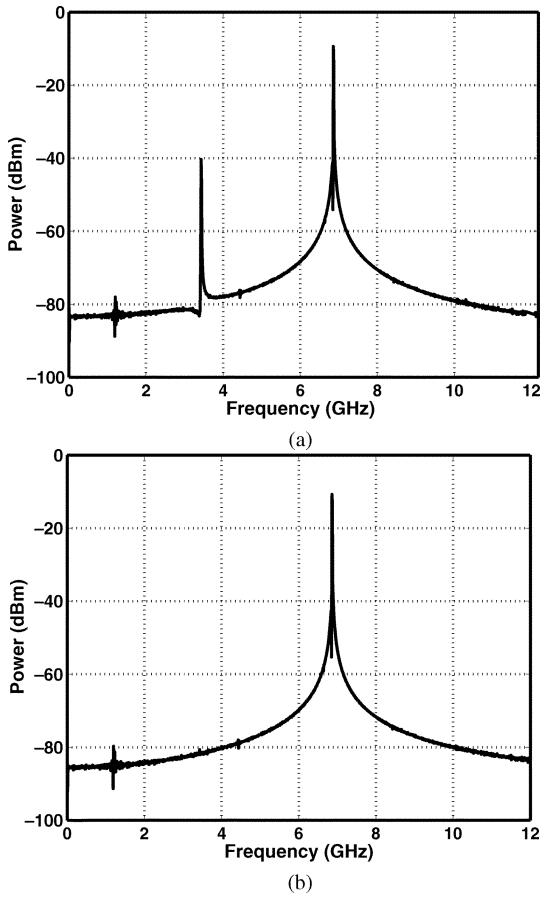

Fig. 12. Simulated spectrum of (a) conventional (b) proposed selector.

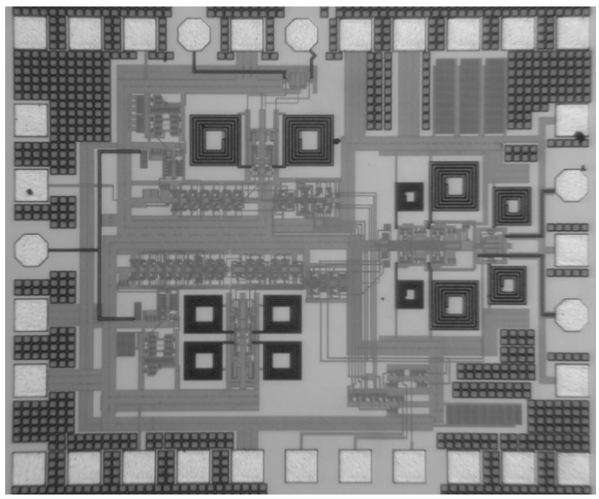

Fig. 13. Chip micrograph.

through the parasitic capacitance C_{GD} [Fig. 11(a)]. A modified version is shown in Fig. 11(b), where two dummy pairs, M_5–M_6 and M_7–M_8, are introduced to eliminate the unwanted coupling to the first order while consuming no extra power. Fig. 12 shows the simulated spectra of two selectors with and without coupling cancellation technique. The undesired coupling is suppressed by more than 40 dB.

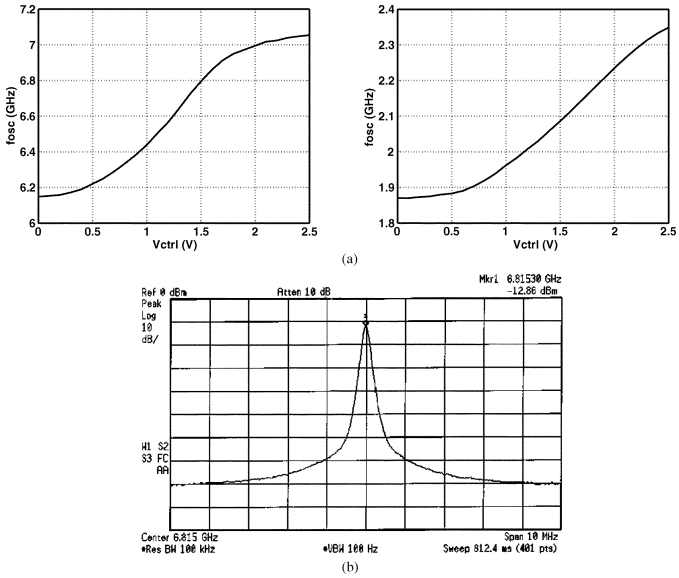

Fig. 14. (a) Tuning range of VCO_1 (left) and VCO_2 (right), (b) free-running spectrum of VCO_1.

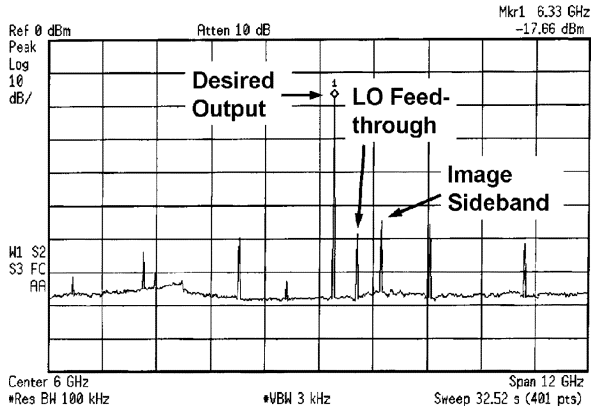

Fig. 15. Output spectrum of Band 4.

IV. Experimental Results

The frequency synthesizer has been fabricated in a 0.18-μm CMOS technology. Fig. 13 shows a photo of the die, which measures 1.3×1.1 mm^2. The outputs are designed as 50-Ω microstrip structures consisting of metal-6 atop metal-1 to absorb pad and routing capacitance. Phase and gain mismatches between internal signals are minimized through symmetry in layout. The circuit has been tested on a chip-on-board assembly while consuming 48 mW from a 2.2-V supply. Note that in steady-state operation, none of the devices experiences more than 1.8 V across it.

To avoid harmonic pulling, the two VCOs are placed apart from each other as much as possible, and guard rings are used between and around them to achieve better isolation. To further investigate the pulling, we examine the spectrum of VCO_1 with VCO_2 turned on and off. No pulling phenomenon is observed. In the spectrum of VCO_1, spurs corresponding to the couplings of VCO_2's fundamental ($\sim$2.112 GHz) and third-order harmonic ($\sim$6.336 GHz) frequencies are measured -64 and -74 dBc, respectively, which are either too weak or too far to cause pulling.

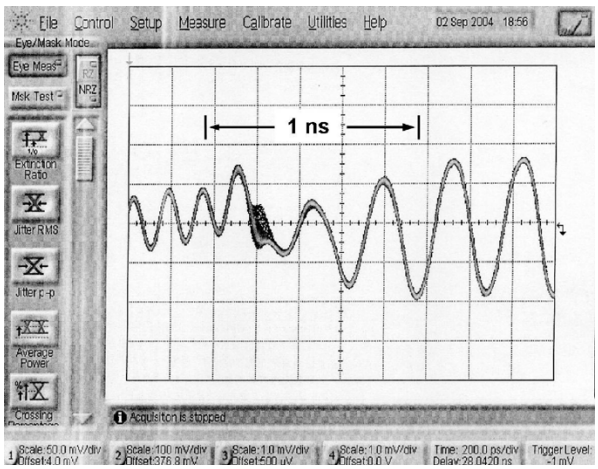

Fig. 16. Band-switching behavior (from Band 4 to Band 1).

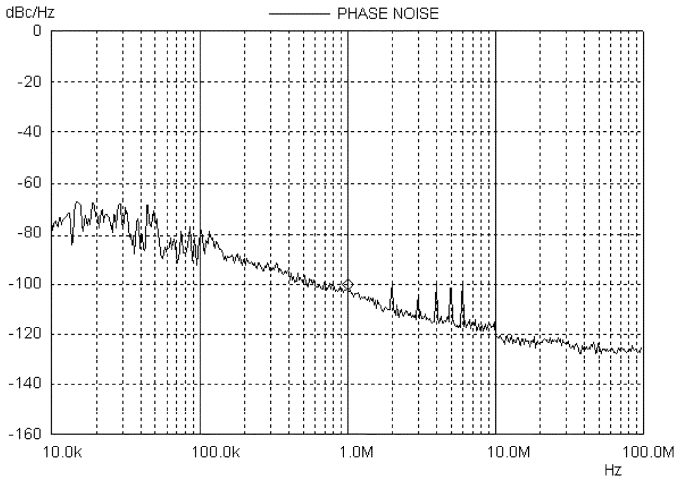

Fig. 17. Output phase noise of Band 3.

Fig. 14(a) shows the tuning characteristics of VCO_1 and VCO_2, suggesting a tuning range of 900 MHz and 470 MHz, respectively. VCO_1 and VCO_2 achieve free-running phase noise of -110 and -116 dBc/Hz at 1-MHz offset, and the spectrum of VCO_1 is plotted in Fig. 14(b). The worst sideband rejection occurs at Band 4 (6.336 GHz), and the spectrum of this band is depicted in Fig. 15. The highest sideband locates at its image (7.392 GHz), which is equal to -37 dBc. The harmonic sidebands are somewhat lower than expected. It is probably because the inductor Q of the SSB mixer's bandpass loading is underestimated in simulation, and a more efficient filtering is performed. The spurs around 2.4 GHz and 5.2 GHz are at least 48 dB lower than the carrier, allowing coexistance between UWB and the ISM users. The band-switching behavior is shown in Fig. 16. Here, the bands are switched periodically and the synthesizer output is monitored. The longest settling time is approximately equal to 1 ns, a value much less than the 9.5-ns guard interval denned in [1]. Note that in Fig. 5, the loading inductor L_1 is approximately 4 times larger than L_2. Thus, for a given Q, the former exhibits a parallel resistance that is twice as much as that of the latter, and the output amplitude changes by a factor of 2 during group switching. Fig. 17 shows the phase noise of Band 3, which measures -103 dBc/Hz at

TABLE I
PERFORMANCE SUMMARY

	[6]	[11]	This Work
Frequency	3.432 ~ 7.92 GHz	3.432 ~ 4.488 GHz	3.432 ~ 7.92 GHz
No. of Bands	7	3	7
Spurs			
In-Band	N/A	≤ –35 dBc	≤ –37 dBc
Out-of-Band	N/A	≤ –45 dBc	≤ –48 dBc
Phase Noise (@1-MHz Offset)	–110 dBc/Hz	–104 dBc/Hz	–103 dBc/Hz
Settling Time	3 ns	1 ns	1 ns
Power Diss.	46 mW	27 mW	48 mW
Supply Voltage	2.7 V	2.7 V	2.2 V
Chip Area	2.0 mm x 2.0 mm	1.0 mm x 1.1 mm	1.3 mm x 1.1 mm
Technology	0.18–um SiGe	0.25–um SiGe	0.18–um CMOS

1-MHz offset. Table I summarizes the measured performance of this work and compares with some other UWB synthesizers recently published in the literature.

V. CONCLUSION

A fast-hopping frequency synthesizer for UWB application produces seven clock frequencies for Mode 2 operation. Achieving switching time of 1 ns and unwanted sidebands of less than -37 dBc, the circuit provides a solution to generate a full coverage of the 14 bands with minor modification, holding great promise for future USB systems.

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