

A 94GHz Duobinary Keying Wireless Transceiver in 65nm CMOS

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Abstract

This work introduces a 94GHz duobinary keying wireless transceiver for point-to-point communications. It presents bandwidth efficiency twice as much as an OOK system and requires no carrier recovery and baseband circuitry to reduce power consumption. Designed and fabricated in 65nm CMOS, the transceiver achieves a 2.0-Gb/s data link with BER $< 10^{-9}$ while consuming a total power of 265mW.

I. Introduction

This paper introduces a novel modulation method based on duobinary signaling, which is especially suitable for broadband point-to-point communications. Duobinary signal presents bandwidth efficiency twice as much as NRZ data, and provides at least 2 to 3 dB better SNR than PAM4 signal [1]. If duobinary is applied to a wireless system with amplitude modulation, it bears twice data rate as compared with an OOK system for a given bandwidth. It is also superior to the 4-ary ASK counterpart in terms of sensitivity. We realize this prototype as a 94GHz wireless data link [2].

II. Transceiver Architecture

Figure 1 illustrates such an idea. The input data is first processed by a duobinary encoder, which controls the transmitter front-end to deliver a W-band carrier with 3 different magnitudes: 0 (off), 1 (half power), and 2 (full power). Similar to a normal duobinary transceiver, the probability of appearing "1" is 50%, whereas that of the other two cases ("0" and "2") are 25% each. The spectrum for a 94GHz carrier under duobinary keying is shown as well, indicating twice bandwidth efficiency as compared with OOK signal under the same condition. The receiver front-end detects the envelope, and passes the amplitude information to the subsequent duobinary decoder. The binary (NRZ) data output is therefore obtained. Unlike PSK or QAM, the duobinary modulation/demodulation can be realized non-coherently, i.e., it needs no carrier recovery circuit, and even the baseband could be omitted. As a result, we can significantly simplify the hardware design and lower the power consumption. Furthermore, it can be shown that the symbol error rate of this scheme is given by

$$\text{SER} = \frac{1}{4} \exp\left(-\frac{\log_2 3}{6} \frac{E_b}{N_0}\right) + \frac{5}{4} Q\left(\sqrt{\frac{\log_2 3}{3} \frac{E_b}{N_0}}\right),$$

where E_b denotes the average bit energy and N_0 is the noise power spectral density under AWGN channel [3]. Although the 4QAM achieves lower SER in theory, the complicate coherent demodulator design with possible phase error

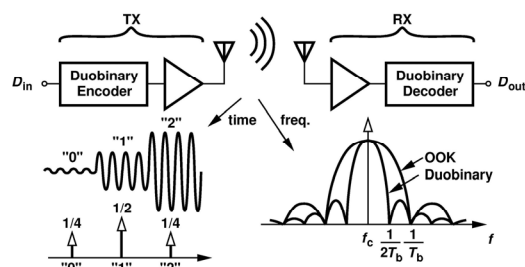


Fig. 1: Duobinary amplitude shift keying.

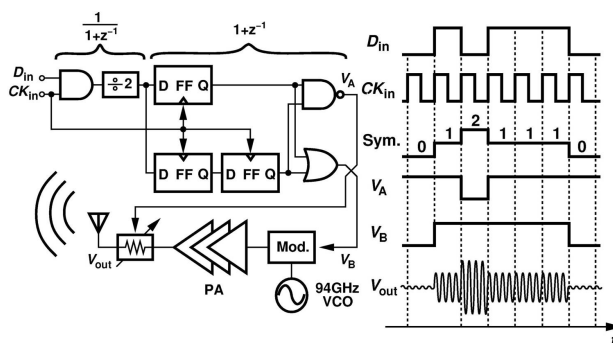


Fig. 2: Transmitter architecture.

degrades the performance significantly. The 4-ary ASK suffers from high error rate and nonlinearity issue, making it improper in practical circuit design.

III. Building Blocks

The transmitter design is shown in Fig. 2. To avoid accumulated data error in transmission, we put both the $1/(1+z^{-1})$ and $1+z^{-1}$ functions in the TX [1]. Two outputs V_A and V_B are generated to control the magnitude of the 94GHz carrier. Owing to the simple architecture, we don't even need a frequency synthesizer here, but instead a free-running VCO. It provides a 94GHz clock, and the modulator determines whether the output is on ("1" or "2"), or off ("0"). An output "0" is quenched by the modulator and nothing is delivered. For a nontrivial output, the PA amplifies the carrier in full scale first, and then the final attenuator activates if the output is a "1". With independent control of the attenuator, it allows the PA to operate in saturation mode and pushes the communication distance to the most extent. A timing diagram introducing the waveforms is shown in Fig. 2.

The modulator and PA/attenuator design is shown in Fig. 3. The 94GHz clock drives the bottom pair M_1 - M_2 , injecting RF current into the switching quad M_3 - M_6 . The on/off signal V_B governs the switching stage M_3 - M_6 . If the output is on ("1" or "2"), differential RF signal goes into the transformer and converts itself into single-ended mode to drive PA. In other words, the transformer here acts as an mm-Wave balun. With proper matching and biasing, the PA delivers RF output to the attenuator. Incorporating 3 identical stages in cascade, the attenuator shorts a portion of RF current to ground by means of switches M_8 and M_9 . The ac-coupled signal path along with switches leaves frequency response almost unchanged for different gain levels. Moreover, when V_A is high, the

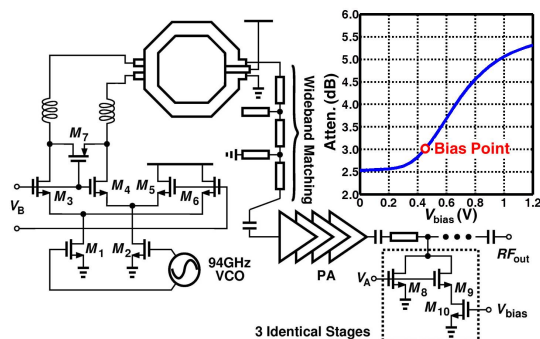


Fig. 3: Realization of modulator, transformer, and attenuator.

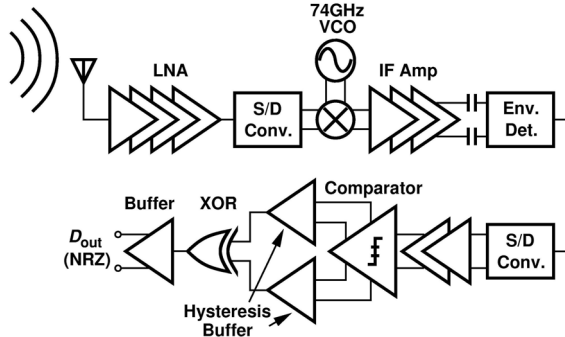


Fig. 4: Receiver architecture.

attenuation can be further fine-tuned by switch M_0 and bias current M_{10} , arriving at a precise 3dB loss over PVT variations. A feed-forward loop performing automatic loss control can be applied here to adjust the attenuation dynamically [4]. Simulation shows that less than 0.3dB variation is achieved for $\pm 10\%$ supply and -20 to 85°C temperature variations. Four staggered common-source amplifier stages are employed as the PA, where conjugate matching is maintained between stages to achieve sufficient power gain. The transformer presents a conversion gain of greater than -1.3dB for the band of 70 to 100GHz, and PA presents a power gain of greater than 18dB for the band of 82 to 98GHz.

The RX must capture the envelope of the 94GHz carrier and convert it back to NRZ data as output. Fig. 4 illustrates the architecture. After LNA, the RF signal is first down-converted into 20GHz or so for easier envelope detection. The envelope detector is realized as that in [5] with even higher gain (0.8dB improvement) due to more advanced CMOS process, and the network corner frequency has been changed to meet the system's requirement. The subsequent single-ended to differential (S/D) converter together with buffers corrects possible waveform distortion caused by envelope detector's nonlinearity. Similar to that in [1], the duobinary decoder involves no coherent sampling. A reference-free comparator with offset control loop optimizes the output data jitter. It compares the input with two threshold levels, generating two outputs which are then XORed to produce the final output D_{out} . If necessary, the remaining data jitter could be further removed by an independent CDR behind the RX.

IV. Experiment Results

The transceiver chipsets have been designed and fabricated in 65nm CMOS technology. The TX consumes 112mW and the RX 153mW, respectively, both from a 1.2V supply. Fig. 5 shows the TX's output waveform and spectrum under 1 and 2 Gb/s duobinary modulation with bit length of $2^{31}-1$, revealing a well-shaped sinc function centered at the carrier frequency ($f_c=92.2\text{GHz}$). Fig. 6(a) illustrates the RX recovered data in response to a 1 and 2Gb/s data (also PRBS of length $2^{31}-1$). The BER as a function of data rate is also investigated. Fig. 6(b) depicts the results for different pattern. $\text{BER} < 10^{-9}$ can be obtained for input data of 1.5Gb/s, and significant error begins to occur as the path loss is greater than 45dB. Lower data rate or shorter sequence prolongs the $\text{BER} < 10^{-9}$ region, as expected. Fig. 7 shows the die micrographs, where the TX occupies 0.55mm^2 and the RX 1.1mm^2 , including pads. A table summarizing the performance of this work and that of other state of the arts is shown in Fig. 7 as well.

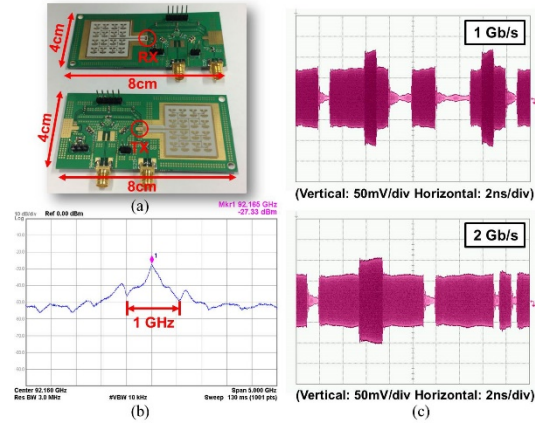


Fig. 5: (a) System assembly, (b) TX output spectrum, (c) TX output waveforms.

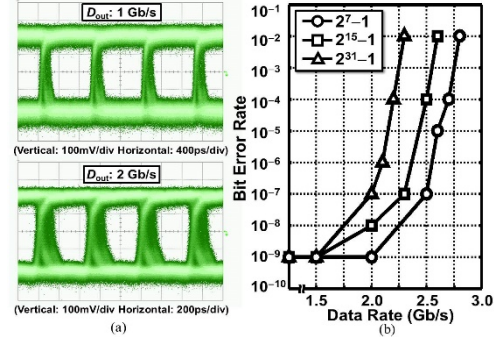


Fig. 6: (a) Recovered data at 1 Gb/s and 2 Gb/s, (b) BER test.

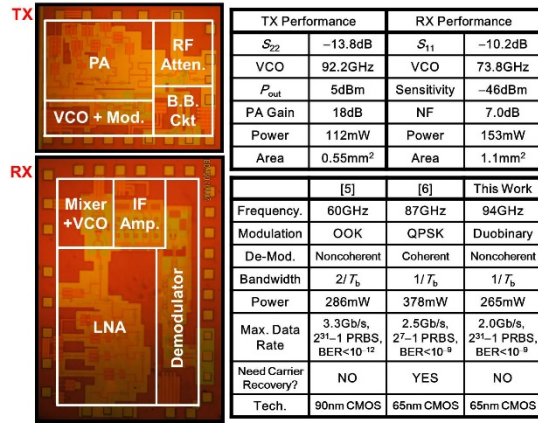


Fig. 7: Die micrograph and performance summary.

Acknowledgment

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