56Gb/s PAM4 and NRZ SerDes Transceivers in 40nm CMOS

Jri Lee, Ping-Chuan Chiang, Chih-Chi Weng
National Taiwan University, Taipei, Taiwan

Abstract

This paper presents 56Gb/s PAM4 and NRZ SerDes transceivers (TRXs), designed and fabricated in advance CMOS technology. Incorporating broadband techniques, noise suppression skills, and clock extraction circuits, this work demonstrates feasibility of 56Gb/s SerDes and compares tradeoffs between the two data format.

I. PAM4 TRX

PAM4 TX is depicted in Fig. 1(a), which has been modified significantly from our previous work [1]. Here, two half-rate serializers with built-in PRBS engines are introduced to provide 16:1 multiplexing and self-testing. PLLs with subharmonically -injection locking technique are used to synchronize the data. Three-tap interleaved FFEs along with nominally 2:1 weighting combiners drive the output port with impedance matching. In optical applications, typical electroabsorption-modulated laser (EML) would present nonlinear transfer function, which degrades the RX's SNR and sensitivity. To obtain 4 uniformly-distributed emission at the RX side, the TX's output must be pre-distorted, adjusting the two middle levels. It could be done by introducing a current-steering combiner, deviating the current ratio between I_{MSB} and I_{LSB} away from 2:1. For a given temperature, the two iDACs governed by FPGA provide corresponding tail currents to the two data paths of the combiner, generating necessary pre-distortion. The level- adjustable range is set to be ±100%, way beyond any possible EML distortion. Figure 1(b) shows two measured cases.

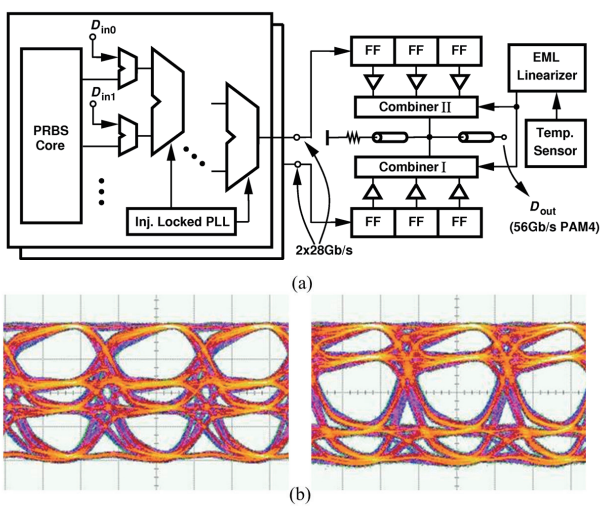


Fig. 1. (a) 56Gb/s PAM4 TX architecture, (b) squeezing and stretching the two middle levels.

Figure 2 illustrates the PAM4 receiver design. It consists of a pre-amplifier/equalizer, a 3-level digitizer with DFE, a PAM4 decoder, and a CDR dedicated to PAM4 data. The input PAM4 signal gets amplified and equalized in a single-stage linear amplifier/equalizer, and then digitized (by three slicers with different offsets) into thermometer code of V_A, V_B, and V_C. The decoder (or equivalently, a 2-bit DAC) converts it to two parallel binary outputs. To ensure sufficient bandwidth through the data path, DFE with 1~3 taps can be applied here. The final data outputs at 28Gb/s (MSB and LSB) are retimed by the 28GHz clock to further clean up jitter and/or distortion. The pure linear CDR design in [2] manifests itself in the capability of handling multi-level signals. Here, V_B (formed by limiting the PAM4 input with balanced threshold) is taken as the input to CDR. Owing to the great granularity and purely linear operation of such a CDR, it smoothly filters out the perturbation of the transition points by its loop bandwidth and leaves the clock edge right in the center of the PAM4 data eye. The PAM4 decoder plays a critical role in the RX design. Stacking logic such as that in [3] fails to work at 56Gb/s simply due to the significant capacitance at internal nodes, insufficient voltage headroom, and limited bandwidth. To remedy this, a flattened structure is proposed in Fig. 3(a). Here, V_A, V_B, and V_C drive three identical differential pairs with different polarities. One extra branch flows half amount of tail current to balance the output dc level, and peaking components are added to extend the bandwidth. The pre-amplifier/equalizer design is illustrated in Fig. 3(b). The switching quad M_1-M_4 together with the loading resistor $R_{1,2}$ and tail currents $I_{1,2}$ reveals three outputs with different thresholds. Variable resistors and capacitors are inserted into the common-source nodes of the quad to provide high-frequency boosting.

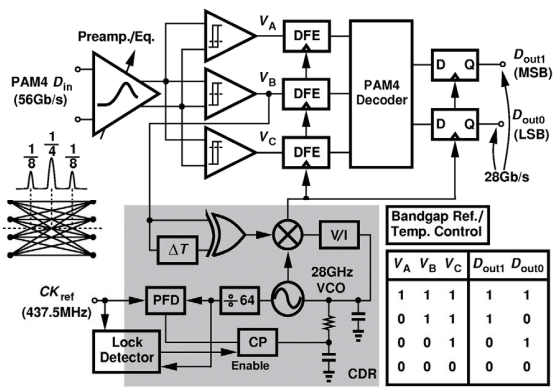


Fig. 2. 56Gb/s PAM4 RX architecture.

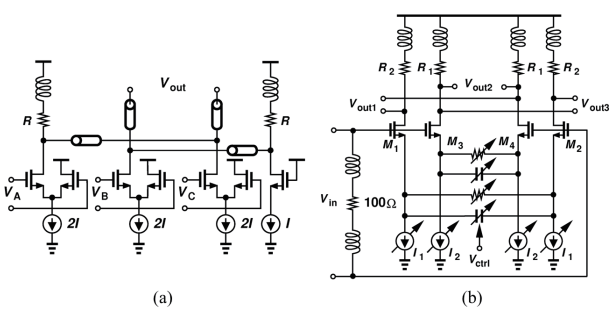


Fig. 3. (a) PAM4 RX LSB decoder, (b) pre-amplifier/equalizer.

II. NRZ TRX

NRZ TX basically follows the design in [1] but with bandwidth and power optimization. The NRZ RX design is illustrated in Fig. 4. Here, we present a full-rate purely-linear NRZ CDR/DEMUX operating at 56Gb/s. After pre-amplification and equalization, the input data goes through a static divided-by-2 circuit to slow down the high-speed data by a factor of 2. The data transitions are still preserved but split into two interleaved paths. By doing so we have earned at least twice as much time to create a pulse, considerably relaxing the timing requirement. The XOR gates are incorporated to distill the transition information from these two new data sequences and mix them up with full-rate clock. To achieve high-speed operation, the half-bit delay generator in [2] is no longer adopted. Instead, we employ vernier approach, i.e., the

half-bit delay is created by the arrival time difference $2(\Delta T_1 - \Delta T_2)$. No data transition is missing here, as a three-input mixer serves as the phase detector. The input data is further deserialized by a 1:8 DMUX, driven by sub-rate clocks coming from the divider chain. Auxiliary loop for frequency acquisition is included to ensure proper operation. To the authors best knowledge, it is the first full-rate linear CDR operating at 50+Gb/s ever reported in the literature.

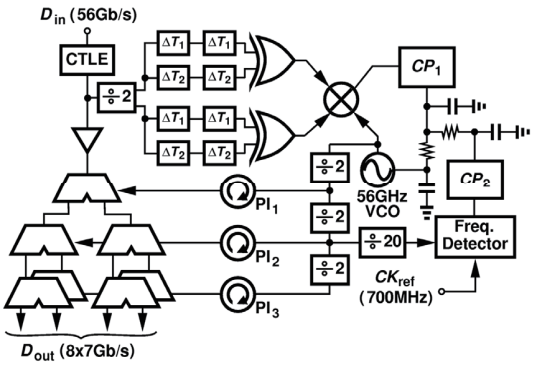


Fig. 4. 56Gb/s NRZ RX architecture.

III. Experimental Results

All chips have been fabricated in 40nm CMOS technology. The PAM4 TX/RX consume 290/420mW of power and NRZ TX/RX 450/220mW, respectively, all from a 1.2V supply. The PAM4 TX output at 56Gb/s is shown in Fig. 5(a), suggesting 4-level total swing of 200mV with vertical rms noise of 3.4mV. In other words, the PAM4 output eye SNR is given by 19.8dB. The PAM4 TX operates nicely from very low data rate to 62Gb/s. Using this PAM4 TX to provide input, we realize an end-to-end link and conduct testing on the PAM4 RX. Figure 5(b) illustrates the phase noise of the recovered clock, which presents rms jitter of 532fs as integrated from 100Hz to 1GHz. CDR itself achieves operation range from 54.1 to 56.8Gb/s. Figure 5(c) shows the recovered output data at 28Gb/s, which presents jitter of less than 520fs,rms and 3.6ps,pp. BER has also been recorded as a function of input level. At 25°C with threshold of BER = 10^{-12}, the sensitivity of PAM4 RX is given by 23mV (spacing between levels) as shown in Fig. 5(d).

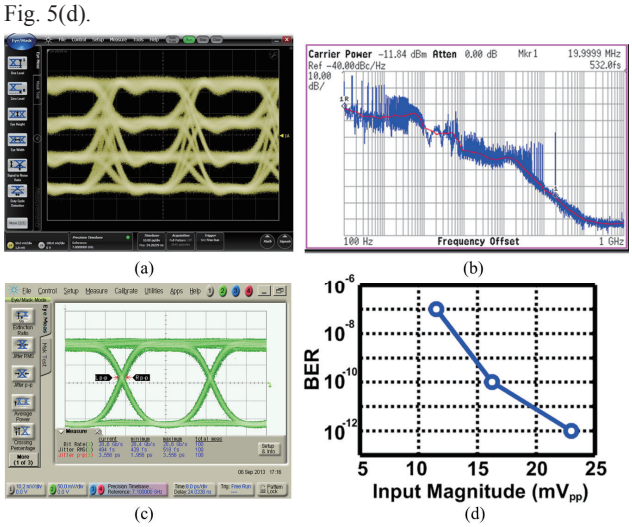


Fig. 5. (a) PAM4 TX outputs (vertical scale: 50mV/div, horizontal scale: 20ps/div), (b) recovered clock at RX, (c) recovered data at RX, (d) RX sensitivity.

Figure 6(a) demonstrates the spectrum of recovered clock at 56GHz. After de-embedding the high loss of the testing equipment (~50dB, harmonic mixer + cable), the original output power is estimated to be 0dBm. Figure 6(b) reveals the 56GHz clock captured by an oscilloscope with 70GHz sampling bandwidth. Again, the limited bandwidth of the scope accounts for the jittery waveform. The demultiplexed data output (@7Gb/s) is depicted in Fig. 6(c), where the rms and peak-to-peak jitter measures 1.40ps and 8.89ps, respectively. BER is less than 10^{-12}. The NRZ CDR shows an operation range from 55.5 to 56.5Gb/s. Figure 6(d) depicts the output BER as a function of input magnitude, implying a sensitivity of 47mV_{pp}. Due to the lack of proper testing equipments at such a high data rate, jitter tolerance cannot be measured at this moment. Figure 7 reveals the die photographs and performance summary.

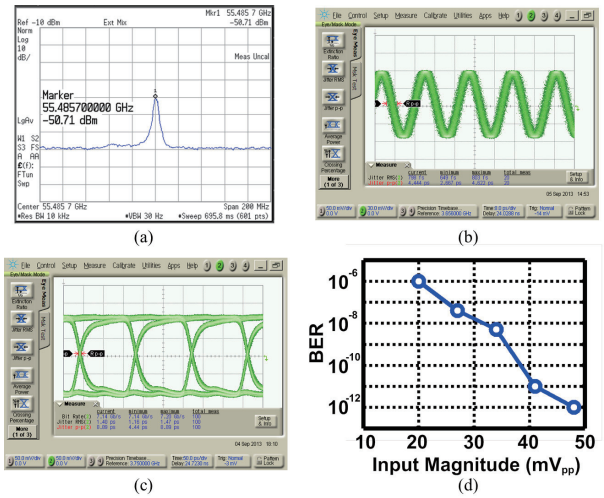
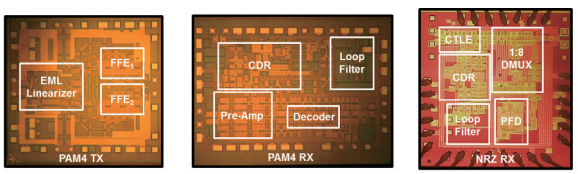


Fig. 6. NRZ RX measurements: (a) recovered clock spectrum at 56GHz (b) clock waveform, (c) demultiplexed output data (7Gb/s), (d) RX sensitivity.



PAM4 TX		PAM4 RX	
Function	Combiner + FFE+ Built-in PLL	Function	CDR + CTLE + 1:2 DMUX
Data Rate	62Gb/s	Operation Range	54.1Gb/s~56.8Gb/s
TX Clock Phase Noise	-99dBc/Hz @ 1MHz	Receiver Clock Jitter	532fs,rms(100Hz~1GHz); 2.0ps,pp @ 28GHz
TX Clock RMS Jitter	508fs (100Hz~1GHz)	Receiver Data Jitter	520fs,rms; 3.6ps,pp @ 28GHz
D_{OUT} Full Mag.	250mV_{pp}	Sensitivity	23mV_{pp} @ BER=10^{-12}
Min. Eye Opening	50mV_{pp}	Power Consumption	420mW
Horizontal Eye Opening	>0.6 UI @ 60Gb/s	Chip Area	1.6 x 1.0mm^2
20-80% Rise/Fall Time	6.8ps @ 56Gb/s	Technology	40nm Digital CMOS
Power Consumption	290mW		
Chip Area	1.2 x 0.95mm^2		
Technology	65nm Digital CMOS		

NRZ TX		NRZ RX	
Function	4:1 MUX + 60GHz PLL + Built-in PRBS	Function	CTLE + CDR + 1:8 DMUX
Data Rate	60 Gb/s	Operation Range	55.5 Gb/s~56.5 Gb/s
TX Clock Phase Noise	-100dBc/Hz @ 1MHz	Receiver Clock Jitter	800fs,rms; 4.4ps,pp @ 56GHz
TX Clock RMS Jitter	461fs (1kHz~20MHz)	Receiver Data Jitter	1.4ps,rms; 8.89ps,pp @ 7Gb/s
Data Input Range (S.E.)	50~300mV_{pp}	Sensitivity	47mV_{pp} @ BER=10^{-12}
Clock Input Range (S.E.)	100~300mV_{pp}	Power Consumption	220mW
Data swing(S.E.)	250mV_{pp} (60Gb/s); 250mV_{pp} (30Gb/s)	Chip Area	1.0 x 1.1mm^2
Power Consumption	450mW (MUX: 81mW)	Technology	65nm Digital CMOS
Chip Area	2.1 x 1mm^2		
Technology	65nm Digital CMOS		

Fig. 7. Chip micrographs and performance summary.

Acknowledgement

This work is sponsored in part by Atilia Technology Inc. The authors thank TSMC university shuttle program for chip fabrication.

References

[1] P. Chiang, *et al.*, *ISSCC* 2014.

[2] Jri Lee, *et al.*, *ISSCC* 2009.

[3] Jri Lee, *et al.*, *JSSC* 2008.