Brief Papers

Analysis and Modeling of Bang-Bang Clock and Data Recovery Circuits

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***Abstract*—A large-signal piecewise-linear model is proposed for bang-bang phase detectors that predicts characteristics of clock and data recovery circuits such as jitter transfer, jitter tolerance, and jitter generation. The results are validated by 1-Gb/s and 10-Gb/s CMOS prototypes using an Alexander phase detector and an LC oscillator.**

***Index Terms*—Bang-bang loops, binary PDs, CDR circuits, jitter, metastability, nonlinear phase detector.**

I. Introduction

CLOCK AND DATA RECOVERY (CDR) circuits incorporating bang-bang (binary) phase detectors (BBPDs) have recently found wide usage in high-speed applications. In contrast to their linear counterparts, BBPDs typically provide so much gain as to avoid the use of charge pumps, thus obviating the need for amplification of very short pulses. Moreover, tristate realizations such as the Alexander topology [1] leave the oscillator control undisturbed in the absence of data transitions, suppressing pattern-dependent jitter. Nevertheless, the heavily nonlinear nature of BBPDs makes the analysis and design of bang-bang CDR circuits difficult.

This paper proposes an approach to modeling bang-bang CDR loops that permits the analytical formulation of jitter characteristics. Two full-rate CMOS CDR circuits operating at 1 Gb/s and 10 Gb/s serve as experimental vehicles to validate the theoretical predictions.

The next section of the paper develops the basic model to be used in the analysis of the loop. Section III applies the model to jitter characteristics. Section IV presents the experimental results.

II. Bang-Bang PD Model

The ideally binary characteristic of BBPDs in practice exhibits a finite slope across a narrow range of the input phase difference. Thus, small phase errors lead to linear operation whereas large phase errors introduce "slewing" in the loop. While [2] considers only the ideal binary model, the distinction between the linear and saturated regions proves critical. In this section, we examine two phenomena that "smooth" out the binary characteristic.

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A. Effect of Metastability

When the zero-crossing points of the recovered clock fall in the vicinity of data transitions, the flipflops comprising the PD may experience metastability, thereby generating an output lower than the full level for some time. In other words, the average output produced by the phase detector remains below the saturated level for small phase differences.

To quantify the effect of metastability, we first consider a single latch consisting of a preamplifier and a regenerative pair (Fig. 1), assuming a gain of $A_{\rm pre}$ for the former and a regeneration time constant of $\tau_{\rm reg}$ for the latter.[1] We also assume a slope of $2k$ for the input differential data and a sufficiently large bandwidth at X and Y so that $V_X - V_Y$ tracks $D_{\rm in}$ with the same slope.

Fig. 2 illustrates three distinct cases that determine certain points on the PD characteristic. If the phase difference between CK and $D_{\rm in}$, ΔT, is large enough, the output reaches the saturated level, $V_F = I_{SS}R_c$, in the sampling model [Fig. 2(a)], yielding an average approximately equal to V_F. For the case $2k\Delta T A_{\rm pre} < V_F$, the circuit regeneratively amplifies the sampled level [Fig. 2(b)], providing $\overline{V_{\rm PD}} < V_F$. Finally, if ΔT is sufficiently small, the regeneration in half a clock period does not amplify $2k\Delta T A_{\rm pre}$ to V_F [Fig. 2(c)], leading to an average output substantially less than V_F. Since the current delivered to the loop filter is proportional to the area under $V_X - V_Y$ and since the waveform in this case begins with an initial condition equal to $2k\Delta T A_{\rm pre}$, we can write

$$\overline{V_{\rm PD,meta}}(\Delta T) \approx \frac{1}{T_b}\int_0^{T_b/2} 2k\Delta T A_{\rm pre}\exp\frac{t}{\tau_{\rm reg}}\,dt \quad (1)$$

$$\approx 2k\Delta T A_{\rm pre}\frac{\tau_{\rm reg}}{T_b}\exp\frac{T_b}{2\tau_{\rm reg}}. \quad (2)$$

Thus, the average output is indeed linearly proportional to ΔT. The linear regime holds so long as the final value at $t = T_b/2$ remains less than V_F,[2] and the maximum phase difference in this regime is given by

$$2k\Delta T_{\rm lin}A_{\rm pre}\exp\frac{T_b}{2\tau_{\rm reg}} = V_F \quad (3)$$

and hence

$$\Delta T_{\rm lin} = \frac{V_F}{2kA_{\rm pre}\exp\dfrac{T_b}{2\tau_{\rm reg}}}. \quad (4)$$

[1]For the sake of brevity, the regenerative gain is included in $\tau_{\rm reg}$, allowing an expression of the form $\exp(t/\tau_{\rm reg})$ for the positive feedback growth of the signal.

[2]Since the regeneration time is in fact equal to $T_b/2 - \Delta T$, the PD characteristic displays a slight nonlinearity in this regime.

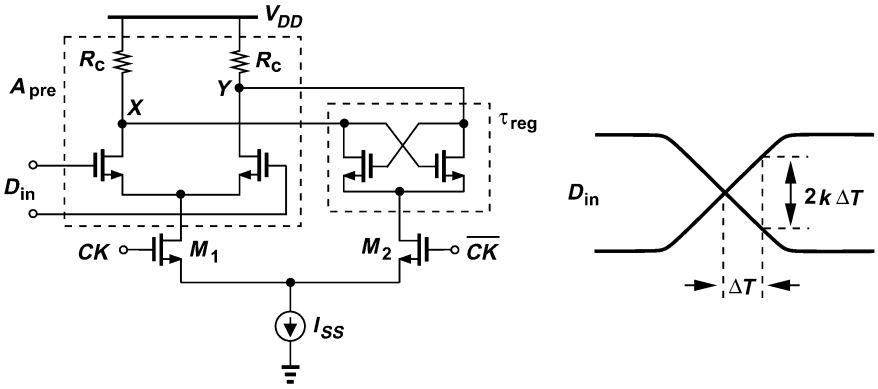

Fig. 1. Current-steering latch and its input data waveform.

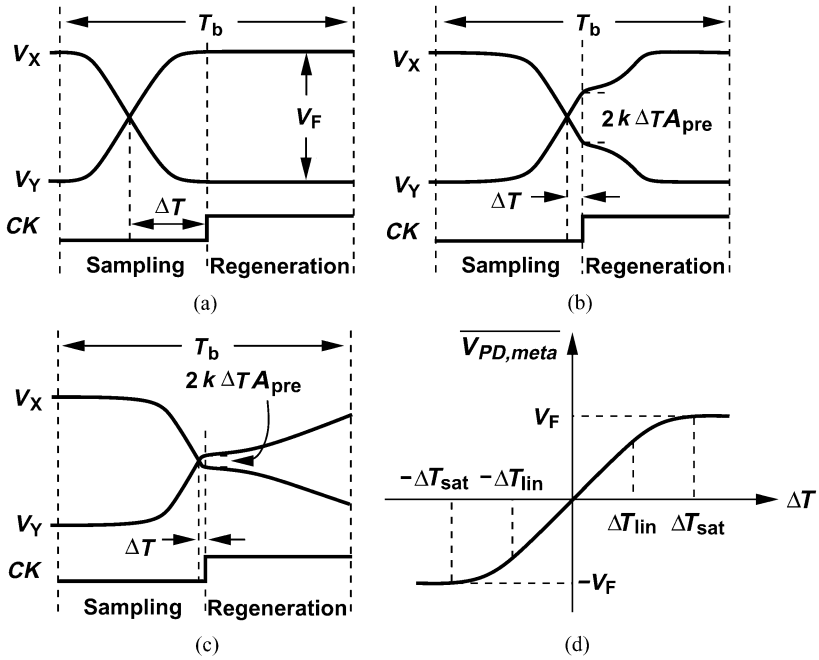

Fig. 2. (a) Average PD output for complete differential pair switching. (b) Average PD output for partial differential pair switching but full regeneration. (c) Average PD output for incomplete regeneration. (d) Typical bang-bang characteristic.

For phase differences greater than $\Delta T_{\rm lin}$, the slope of the characteristic begins to drop, approaching zero if the preamplified level reaches V_F:

$$\Delta T_{\rm sat} = \frac{V_F}{2kA_{\rm pre}}. \tag{5}$$

Fig. 2(d) summarizes these concepts.

In practice, PDs employ a number of flipflops, possibly with different fanouts, making the analysis more difficult. Nevertheless, transistor-level simulations of the circuit can yield the characteristic as the phase difference between $D_{\rm in}$ and CK is varied in small steps. Fig. 3 shows the Alexander PD (followed by a voltage-to-current converter) and the simulated characteristic in 0.18-μm CMOS technology for a data rate of 10 Gb/s and a clock frequency of 10 GHz. The latches in the PD are based on the topology depicted in Fig. 1.

B. Effect of Jitter

The binary PD characteristic is also smoothed out by the jitter inherent in the input data and the oscillator output. Even with abrupt data and clock transitions, the random phase difference resulting from jitter leads to an average output lower than the saturated levels. As illustrated in Fig. 4(a), for a phase difference of ΔT, it is possible that the tail of the jitter distribution shifts the clock edge to the left by more than ΔT, forcing the PD to sample a level of $-V_0$ rather than $+V_0$. To obtain the average output under this condition, we sum the positive and negative samples with a weighting given by the probability of their occurrences:

$$\overline{V_{\rm PD}}(\Delta T) = -V_0 \int_{-\infty}^{-\Delta T} p(x)\,dx + V_0 \int_{-\Delta T}^{+\infty} p(x)\,dx \tag{6}$$

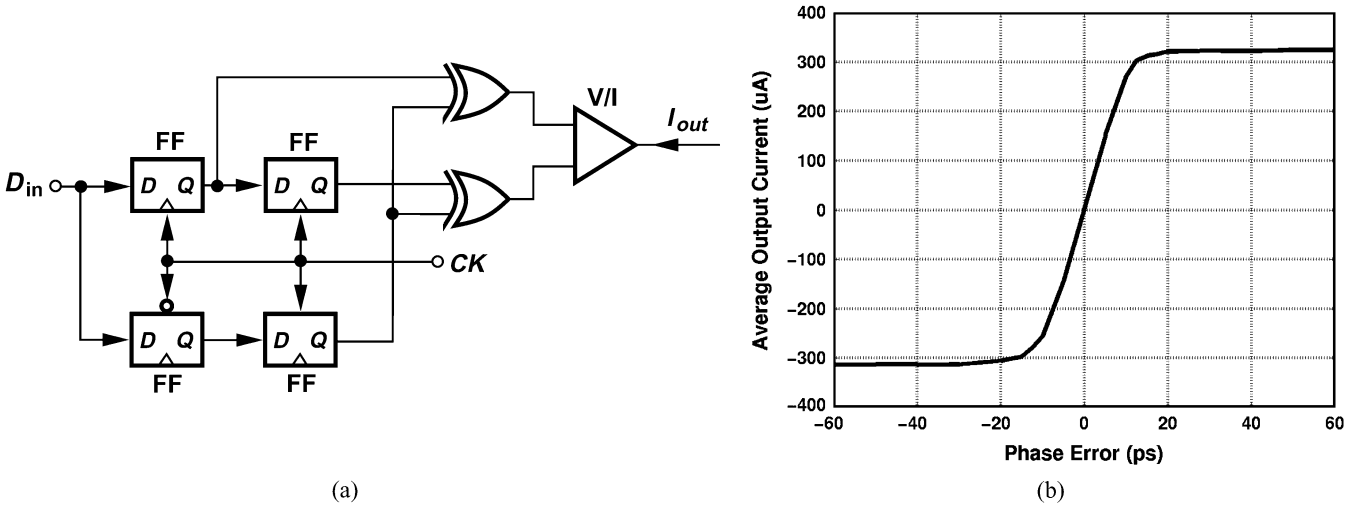

Fig. 3. (a) Alexander PD. (b) Simulated characteristic at transistor level.

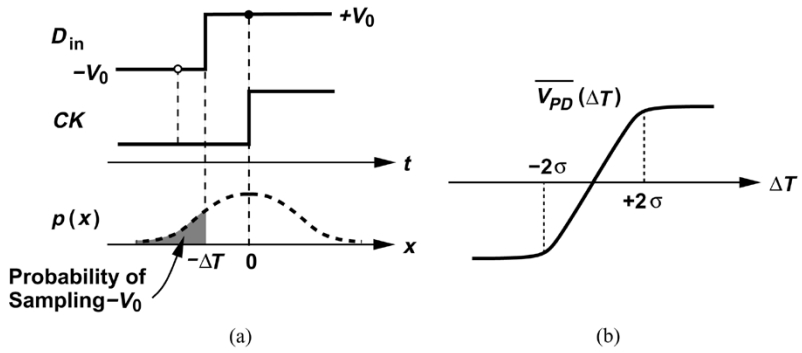

Fig. 4. Smoothing of PD characteristic due to jitter.

where $p(x)$ denotes the probability density function (PDF) of jitter. Since the PDF is typically even-symmetric, this result can be rewritten as

$$\overline{V_{\rm PD}}(\Delta T) = -V_0 \int_{+\Delta T}^{+\infty} p(x)\,dx + V_0 \int_{-\infty}^{+\Delta T} p(x)\,dx \quad (7)$$

which is equivalent to the convolution of the bang-bang characteristic and the PDF of jitter. Illustrated in Fig. 4(b), $\overline{V_{\rm PD}}$ exhibits a relatively linear range for $|\Delta T| < 2\sigma$ if the PDF is Gaussian with a standard deviation of σ.

C. Overall Characteristic

To combine the above effects, we begin with a characteristic smoothed by metastability, $\overline{V_{\rm meta}}$, and determine the impact of jitter. As shown in Fig. 5(a), the probability that the jitter lies between x and $x + dx$ is equal to $p(x)\,dx$. In other words, the PD generates an output equal to $\overline{V_{\rm meta}}(\Delta T_1 + x)$ rather than $\overline{V_{\rm meta}}(\Delta T_1)$ with a probability of $p(x)\,dx$. Thus, the average output corresponding to a nominal phase difference of ΔT_1 is equal to

$$\overline{V_{\rm tot}}(\Delta T_1) = \int_{-\infty}^{+\infty} \overline{V_{\rm meta}}(\Delta T_1 + x)p(x)\,dx. \quad (8)$$

Since $p(x) = p(-x)$, this expression can be written as

$$\overline{V_{\rm tot}}(\Delta T_1) = \int_{-\infty}^{+\infty} \overline{V_{\rm meta}}(\Delta T_1 - u)p(u)\,du \quad (9)$$

which is equal to the convolution of $\overline{V_{\rm meta}}(\Delta T)$ and $p(x)$. As illustrated in Fig. 5(b) for small jitter, the convolution effect further widens the metastability-smoothed characteristic, pushing the "corners" of $\overline{V_{\rm meta}}$ by approximately 2σ.

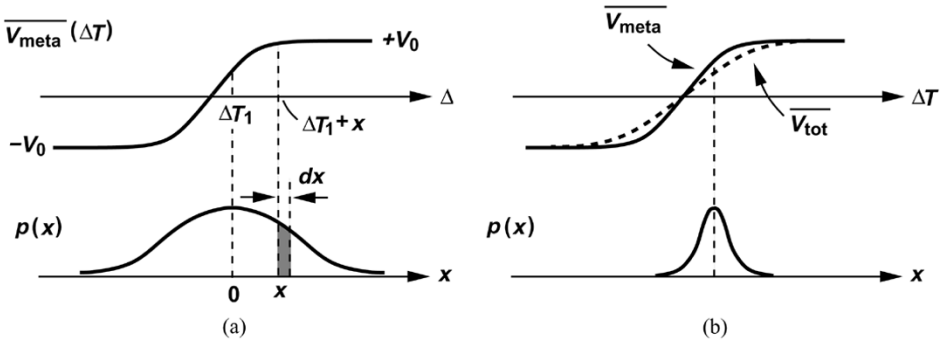

Fig. 5. (a) Derivation of overall characteristic. (b) Result for small jitter.

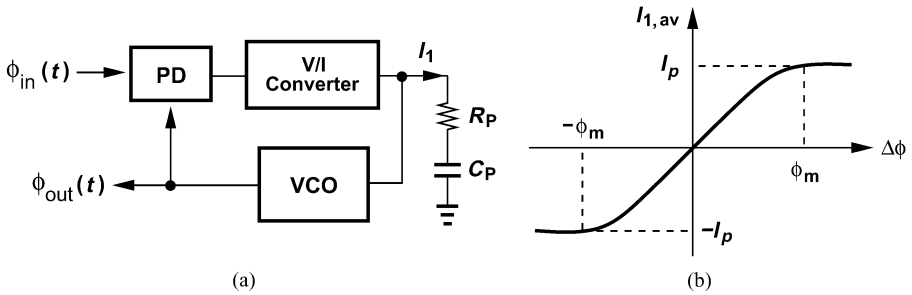

Fig. 6. (a) Bang-bang CDR model and (b) the corresponding characteristic.

Fig. 6 depicts the resulting model. The PD is followed by a low-speed V/I converter[3] and the linear range of the PD characteristic is denoted by $\pm\phi_m$.

III. Jitter Analysis

A. Jitter Transfer

Jitter transfer represents the response of a CDR loop to input jitter, $\phi_{\rm in}(t) = \phi_{{\rm in},p}\cos\omega_\phi t$. If $\phi_{{\rm in},p} < \phi_m$, then the PD operates in the linear region, yielding a standard second-order system. On the other hand, as $\phi_{{\rm in},p}$ exceeds ϕ_m, the phase difference between the input and output may also rise above ϕ_m, leading to nonlinear operation. At low jitter frequencies, $\phi_{\rm out}(t)$ still tracks $\phi_{\rm in}(t)$ closely, $|\Delta\phi| < |\phi_m|$, and $|\phi_{\rm out}/\phi_{\rm in}| \approx 1$. As ω_ϕ increases, so does $\Delta\phi$, demanding that the V/I converter pump a larger current into the loop filter. However, since the available current beyond the linear PD region is constant, large and fast variation of $\phi_{\rm in}$ results in "slewing."

To study this phenomenon, let us assume $\phi_{{\rm in},p} \gg \phi_m$ as an extreme case so that $\Delta\phi$ changes polarity in every half cycle of ω_ϕ, requiring that I_1 alternately jump between $+I_p$ and $-I_p$ (Fig. 7). Since the loop filter capacitor is typically large, the oscillator control voltage tracks I_1R_p, leading to binary modulation of the VCO frequency and hence triangular variation of the output phase. The peak value of $\phi_{\rm out}$ occurs after integration of the control voltage for a duration of $T_\phi/4$, where $T_\phi = 2\pi/\omega_\phi$; that is,

$$\phi_{{\rm out},p} = \frac{K_{\rm VCO}I_pR_pT_\phi}{4} \tag{10}$$

[3]We distinguish between V/I converters and charge pumps because the former can sense the *average* levels at the XOR gate outputs whereas the latter must be driven with high-speed pulses.

and

$$\left|\frac{\phi_{{\rm out},p}}{\phi_{{\rm in},p}}\right| = \frac{\pi K_{\rm VCO}I_pR_p}{2\phi_{{\rm in},p}\omega_\phi}. \tag{11}$$

Expressing the dependence of the jitter transfer upon the jitter amplitude, $\phi_{{\rm in},p}$, this equation also reveals a 20-dB/dec roll-off in terms of ω_ϕ. Of course, as ω_ϕ decreases, slewing eventually vanishes, (11) is no longer valid, and the jitter transfer approaches unity. As depicted in Fig. 8(a), extrapolation of linear and slewing regimes yields an approximate value for the -3-dB bandwidth of the jitter transfer:

$$\omega_{-3\ {\rm dB}} = \frac{\pi K_{\rm VCO}I_pR_p}{2\phi_{{\rm in},p}}. \tag{12}$$

It is therefore possible to approximate the entire jitter transfer as

$$\frac{\phi_{{\rm out},p}}{\phi_{{\rm in},p}}(s) = \frac{1}{1+\dfrac{s}{\omega_{-3\ {\rm dB}}}}. \tag{13}$$

Fig. 8(b) plots the jitter transfer for different input jitter amplitudes. The transfer approaches that of a linear loop as $\phi_{{\rm in},p}$ decreases toward ϕ_m.

It is interesting to note that the jitter transfer of slew-limited CDR loops exhibits negligible peaking. Due to the high gain in the linear regime, the loop operates with a relatively large damping factor in the vicinity of $\omega_{-3\ {\rm dB}}$. In the slewing regime, as evident from the $\phi_{\rm in}$ and $\phi_{\rm out}$ waveforms in Fig. 7, $\phi_{{\rm out},p}$ can only *fall* monotonically as ω_ϕ increases because the slew rate is constant.

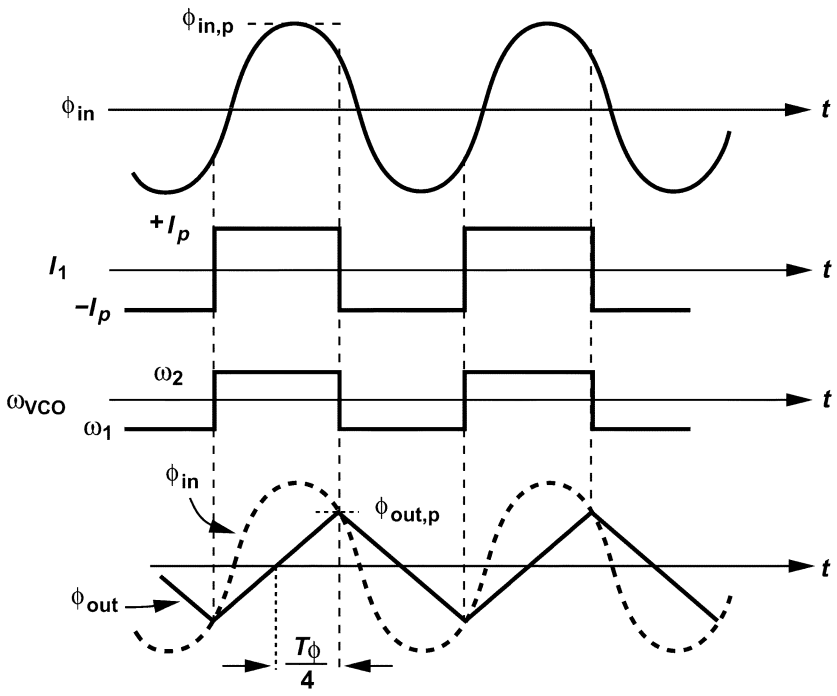

Fig. 7. Slewing in a CDR loop.

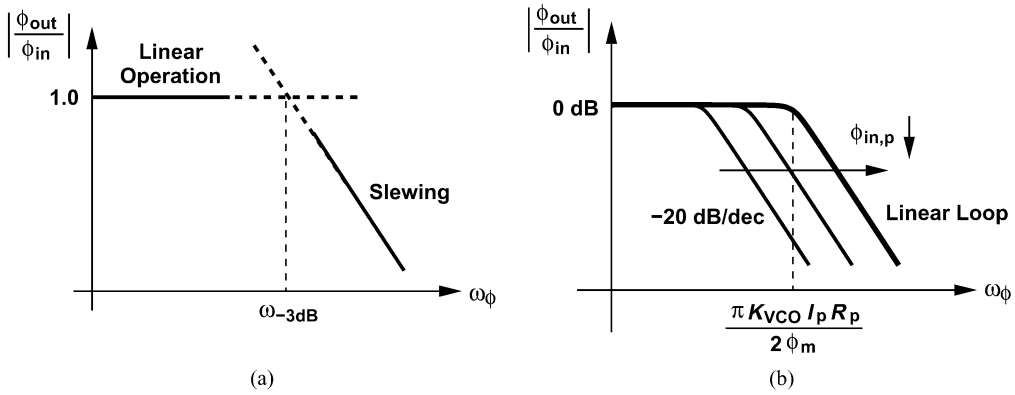

Fig. 8. (a) Calculation of −3-dB. (b) Jitter transfer function of a bang-bang CDR.

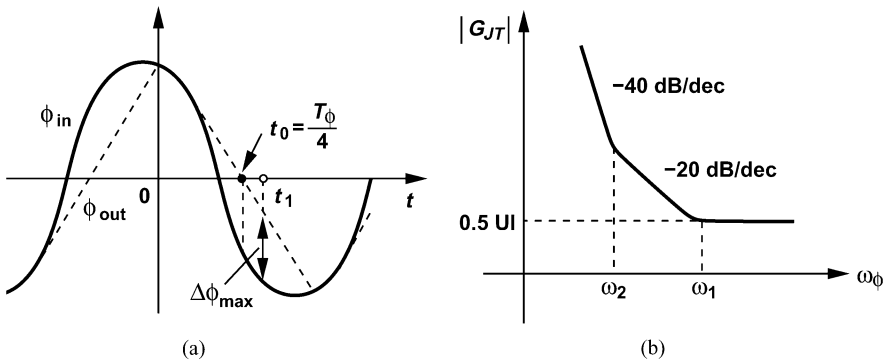

Fig. 9. (a) Slewing in jitter tolerance test. (b) Jitter tolerance of a bang-bang CDR circuit.

B. Jitter Tolerance

Jitter tolerance is defined as the maximum input jitter that a CDR loop can tolerate without increasing the bit error rate at a given jitter frequency. As the phase error, $\phi_{\rm in} - \phi_{\rm out}$, approaches π [= half unit interval (UI)], BER rises rapidly.

It is important to recognize that a bang-bang loop *must* slew if it incurs errors. With no slewing, the phase difference between the input and output falls below $\phi_m (\ll \pi)$, and the data is sampled correctly. Fig. 9(a) shows an example where $\phi_{\rm out}$ slews and $\phi_{{\rm in},p}$ is chosen such that $\Delta\phi_{\max} = \pi$. Thus, a relationship

is sought that expresses $\phi_{\text{in},p}$ in terms of ω_ϕ while the maximum phase error is equal to 0.5 UI.

Fig. 9(a) reveals that $\Delta\phi_{\max}$ occurs at some point t_1, but $\Delta\phi$ at t_0 is close to $\Delta\phi_{\max}$ and much simpler to calculate. If ϕ_{out} slews for most of the period, t_0 is approximately equal to $T_\phi/4$. Assuming $\phi_{\text{in}} = \phi_{\text{in},p}\cos(\omega_\phi t + \delta)$,[4] we arrive at

$$K_{\text{VCO}} I_p R_p \frac{T_\phi}{4} = \phi_{\text{in},p}\cos\delta \tag{14}$$

and

$$\delta = \tan^{-1}\frac{\sqrt{4\omega_\phi^2\phi_{\text{in},p}^2 - \pi^2 K_{\text{VCO}}^2 I_p^2 R_p^2}}{\pi K_{\text{VCO}} I_p R_p}. \tag{15}$$

It follows that

$$\Delta\phi_{\max} \approx \Delta\phi(t_0) = \left|\phi_{\text{in},p}\cos\left(\frac{\pi}{2}+\delta\right)\right| \tag{16}$$

$$= \frac{\sqrt{4\omega_\phi^2\phi_{\text{in},p}^2 - \pi^2 K_{\text{VCO}}^2 I_p^2 R_p^2}}{2\omega_\phi}. \tag{17}$$

Equating $\Delta\phi_{\max}$ to π yields the maximum tolerable input jitter $\phi_{\text{in},p} = G_{\text{JT}}$:

$$|G_{\text{JT}}| = \pi\sqrt{1 + \frac{K_{\text{VCO}}^2 I_p^2 R_p^2}{4\omega_\phi^2}}. \tag{18}$$

As expected, $|G_{\text{JT}}|$ falls at a rate of 20 dB/dec for low ω_ϕ, approaching π at high ω_ϕ. A corner frequency, ω_1, can be defined by equating (18) to $\sqrt{2}\pi$:

$$\omega_1 = \frac{K_{\text{VCO}} I_p R_p}{2}. \tag{19}$$

The above analysis has followed the same assumptions as those in Fig. 7, namely, the change in the control voltage is due to $I_1 R_p$ and the voltage across C_p remains constant. At jitter frequencies below $(R_p C_p)^{-1}$, however, this condition is violated, leading to "nonlinear slewing" at the output. In fact, for a sufficiently low ω_ϕ, the (linear) voltage change across C_p far exceeds $I_1 R_p$, yielding a *parabolic* shape for ϕ_{out} (Fig. 10). Thus

$$\phi_{\text{out}}(t) = -\int K_{\text{VCO}}\frac{I_p}{C_p} t\,dt + \phi_{\text{out},p}, \quad 0 < t < \frac{T_\phi}{2} \tag{20}$$

$$= -\frac{1}{2}\frac{K_{\text{VCO}} I_p}{C_p} t^2 + \phi_{\text{out},p}. \tag{21}$$

Since ϕ_{out} reaches $-\phi_{\text{out},p}$ at $t = T_\phi/2$, we have

$$\phi_{\text{out}}\left(\frac{T_\phi}{2}\right) = -\phi_{\text{out},p} = -\frac{1}{2}\frac{K_{\text{VCO}} I_p}{C_p}\frac{T_\phi^2}{4} + \phi_{\text{out},p} \tag{22}$$

[4]The angle δ is chosen such that the *output* peak occurs at $t = 0$, simplifying the algebra.

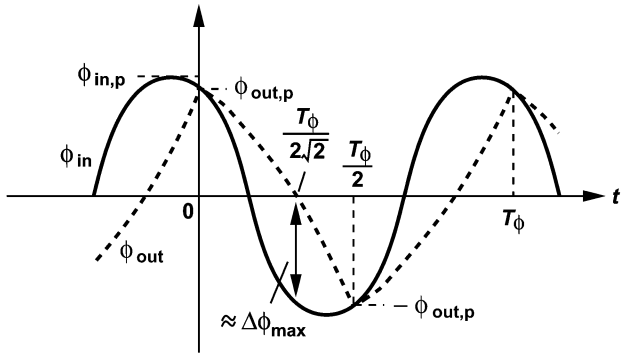

Fig. 10. Nonlinear slewing in jitter tolerance test.

and hence

$$\phi_{\text{out},p} = \phi_{\text{in},p}\cos\delta = \frac{K_{\text{VCO}} I_p \pi^2}{4 C_p \omega_\phi^2}. \tag{23}$$

Note that the zero-crossing point of ϕ_{out} occurs at $t = T_\phi/(2\sqrt{2})$. Adopting the same technique used for the linear-slewing case, we approximate $\Delta\phi_{\max}$ with $|\phi_{\text{in}}(T_\phi/2\sqrt{2})|$ and obtain

$$\Delta\phi_{\max} \approx \left|\phi_{\text{in},p}\cos\left(\omega_\phi\frac{T_\phi}{2\sqrt{2}} + \delta\right)\right| \tag{24}$$

$$= -\phi_{\text{in},p}\cos\frac{\pi}{\sqrt{2}}\cos\delta + \phi_{\text{in},p}\sin\frac{\pi}{\sqrt{2}}\sin\delta \tag{25}$$

$$= 0.61\frac{K_{\text{VCO}} I_p \pi^2}{4 C_p \omega_\phi^2} + 0.8\frac{\sqrt{16 C_p^2\omega_\phi^4\phi_{\text{in},p}^2 - K_{\text{VCO}}^2 I_p^2 \pi^4}}{4 C_p \omega_\phi^2}. \tag{26}$$

Again, equating $\Delta\phi_{\max}$ to π yields the jitter tolerance, $G_{\text{JT}} = \phi_{\text{in},p}$:

$$|G_{\text{JT}}| = \sqrt{\frac{\left(\pi - 0.61\frac{K_{\text{VCO}} I_p \pi^2}{4 C_p \omega_\phi^2}\right)^2}{0.64} + \frac{K_{\text{VCO}}^2 I_p^2 \pi^4}{16 C_p^2 \omega_\phi^4}}. \tag{27}$$

At very low jitter frequencies, we have

$$0.61\frac{K_{\text{VCO}} I_p \pi^2}{4 C_p \omega_\phi^2} \gg \pi \tag{28}$$

and $|G_{\text{JT}}|$ is equal to

$$|G_{\text{JT}}| = 1.26\frac{K_{\text{VCO}} I_p \pi^2}{4 C_p \omega_\phi^2}. \tag{29}$$

Consequently, $|G_{\text{JT}}|$ falls at a rate of approximately 40 dB/dec in this regime [Fig. 9(b)]. The corner frequency between the two regimes can be calculated by extrapolating (18) and (29) and

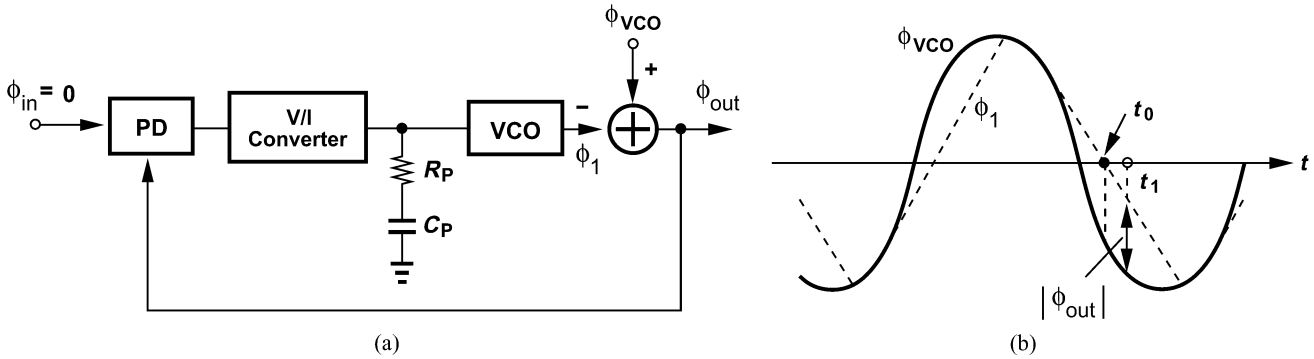

Fig. 11. (a) CDR with additive VCO phase noise. (b) Effect of slewing due to VCO jitter.

assuming that their intersection frequency is several times lower than ω_1:

$$\omega_2 = 0.63\frac{\pi}{R_pC_p}. \tag{30}$$

To justify the assumption $\omega_1 \gg \omega_2$, we write from (19) and (30):

$$\frac{K_{\rm VCO}I_pR_p}{2\pi} \gg \frac{0.63}{R_pC_p}. \tag{31}$$

The right-hand side represents the (small-signal) -3-dB bandwidth of the loop (for a relatively large damping factor) while the left-hand side is equal to the closed-loop zero frequency multiplied by 0.63. Since the loop bandwidth is typically much greater than the zero frequency [3], the above assumption is valid.

C. Jitter Generation due to VCO Phase Noise

The jitter generated by a CDR loop arises from a number of sources, including the VCO phase noise, ripple on the control line, supply and substrate noise, etc. In this section, we study the contribution of VCO phase noise to the output jitter. For low-frequency or small VCO jitter, the PD operates linearly, yielding a second-order high-pass transfer function for the VCO phase noise. If the damping factor is large

$$\frac{\phi_{\rm out}}{\phi_{\rm in}}(s) \approx \frac{s}{s+2\zeta\omega_n} \tag{32}$$

where $\zeta = (R_p/2)\sqrt{I_pC_pK_{\rm VCO}/\phi_m}$ and $\omega_n = \sqrt{I_pK_{\rm VCO}/(C_p\phi_m)}$. The corner frequency of the high-pass transfer is thus equal to

$$\omega_{-3\ {\rm dB,lin}} = \frac{K_{\rm VCO}I_pR_p}{\phi_m}. \tag{33}$$

Moderate jitter frequencies having a peak amplitude greater than ϕ_m introduce slewing. As depicted in Fig. 11(a), such a jitter component is represented by $\phi_{\rm VCO}(t) = \phi_{{\rm VCO},p}\cos\omega_\phi t$,

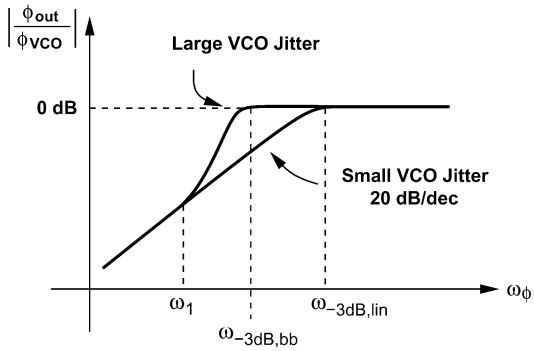

Fig. 12. Transfer function of VCO phase noise.

and ϕ_1 tracks $\phi_{\rm VCO}$ so as to minimize $\phi_{\rm out}$. In the case of extreme slewing, $\phi_{\rm VCO}$ and ϕ_1 appear as shown in Fig. 11(b), allowing an approximation similar to that for jitter tolerance:

$$|\phi_{{\rm out},p}| = \sqrt{\phi_{{\rm VCO},p}^2 - \frac{\pi^2K_{\rm VCO}^2I_p^2R_p^2}{4\omega_\phi^2}} \tag{34}$$

and hence

$$\left|\frac{\phi_{{\rm out},p}}{\phi_{{\rm VCO},p}}\right| = \sqrt{1 - \frac{\pi^2K_{\rm VCO}^2I_p^2R_p^2}{4\omega_\phi^2\phi_{{\rm VCO},p}^2}}. \tag{35}$$

These results hold for $\omega_\phi > \pi K_{\rm VCO}I_pR_p/(2\phi_{{\rm VCO},p})$. The derivative of (35) indicates that $|\phi_{{\rm out},p}/\phi_{{\rm VCO},p}|$ rises at a rate higher than 20 dB/dec under slewing conditions (Fig. 12). To estimate the frequency at which the linear and nonlinear regimes begin to depart from each other, we substitute $|\phi_{{\rm out},p}| = \phi_m$ in the linear model:

$$\left|\frac{\phi_m}{\phi_{{\rm VCO},p}}\right| = \frac{\omega_1}{\sqrt{\omega_1^2 + 4\zeta^2\omega_n^2}} \tag{36}$$

obtaining

$$\omega_1 = \frac{K_{\rm VCO}I_pR_p}{\sqrt{\phi_{{\rm VCO},p}^2 - \phi_m^2}}. \tag{37}$$

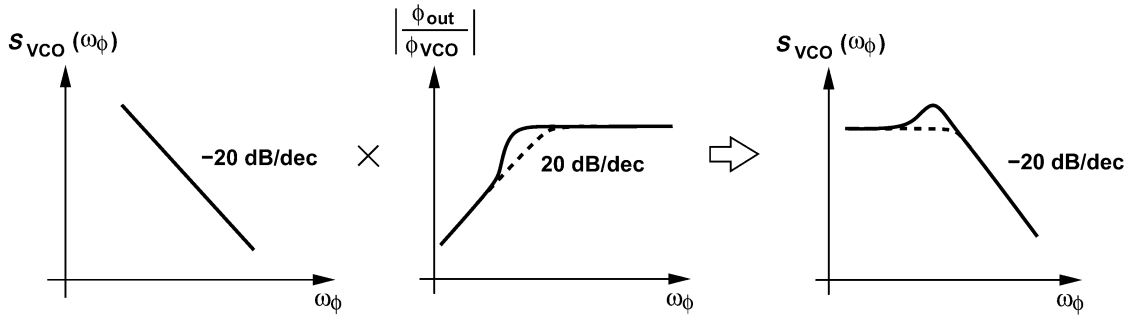

Fig. 13. VCO phase noise shaping.

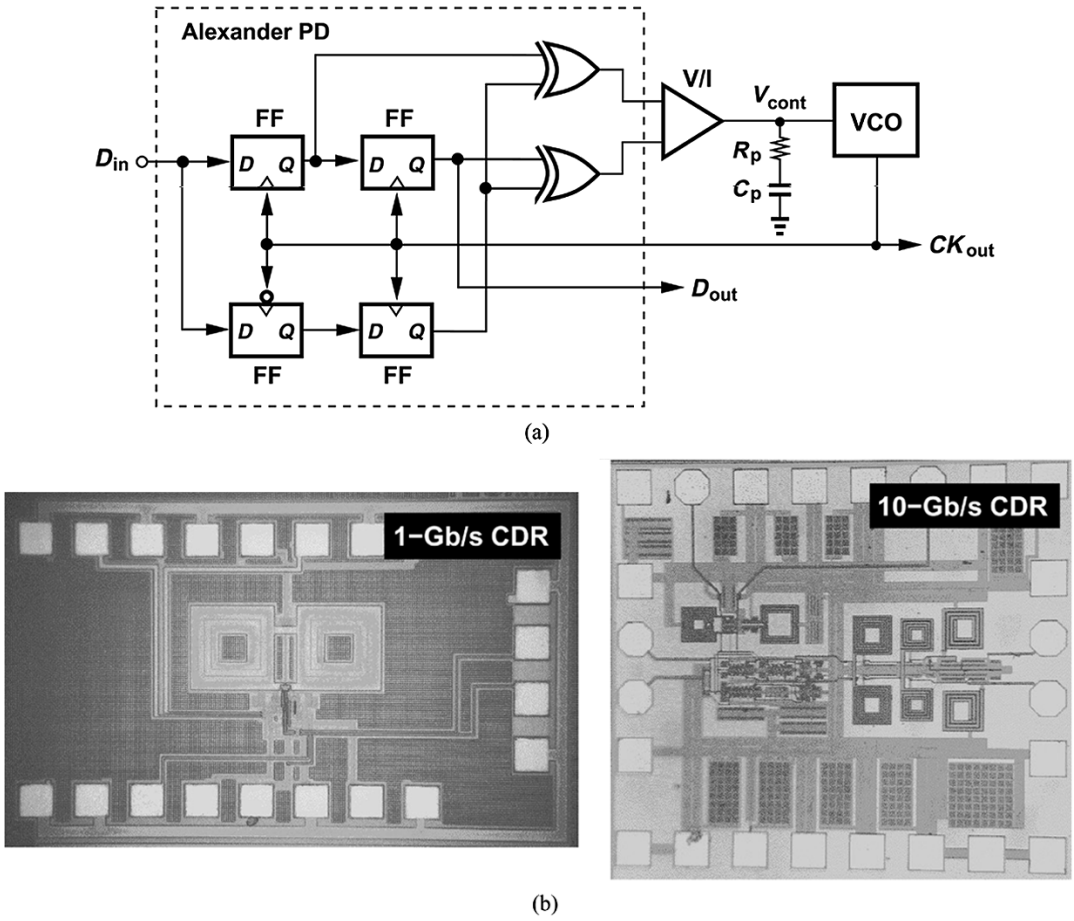

Fig. 14. (a) CDR architecture and (b) die photographs.

The corner frequency, $\omega_{-3\ \mathrm{dB},bb}$, is computed by equating (35) to $1/\sqrt{2}$:

$$\omega_{-3\ \mathrm{dB},bb} = \frac{\pi K_{\mathrm{VCO}} I_p R_p}{\sqrt{2}\phi_{\mathrm{VCO},p}}. \tag{38}$$

The sharp rise of $|\phi_{\mathrm{out}}/\phi_{\mathrm{VCO}}|$ under the slewing condition suggests that the spectrum of the recovered clock may exhibit a peak near the band edge (Fig. 13). In other words, *if* the VCO jitter is large, then a peak may appear in the spectrum, an effect not predicted by linear models.

IV. Experimental Results

Two CDR circuits operating at 1 Gb/s and 10 Gb/s[5] have been designed and fabricated in 0.35-μm and 0.18-μm CMOS technologies, respectively, to validate the analysis and modeling techniques presented in this paper. Fig. 14(a) shows the CDR architecture and Fig. 14(b) the die photographs. The VCO employs a cross-coupled pair with spiral inductors and MOS varactors.

[5]The center frequency of the VCO in the 10-Gb/s prototype is around 11 GHz. Thus, most measurements are performed around 10.5–11 Gb/s.

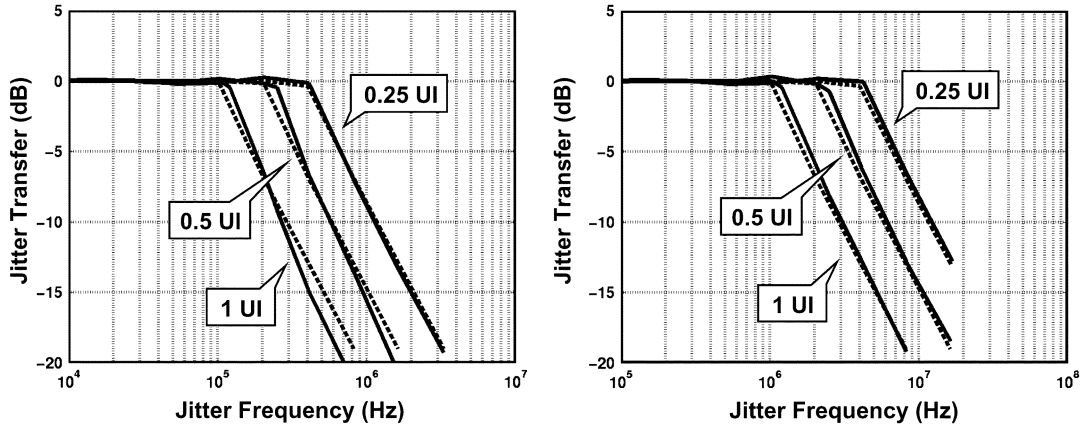

Fig. 15. Measured (solid lines) and predicted (dashed lines) jitter transfer of (a) 1-Gb/s prototype and (b) 10-Gb/s prototype for different input jitter amplitudes.

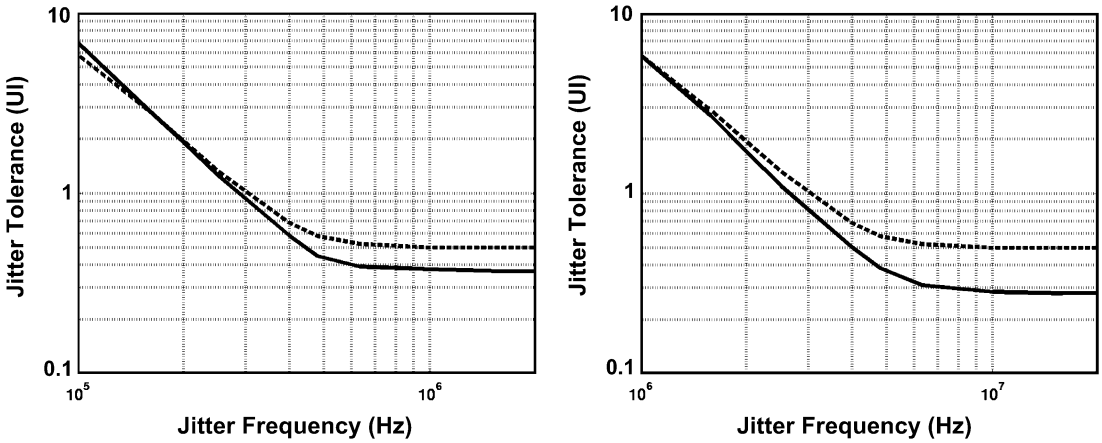

Fig. 16. Measured (solid lines) and predicted (dashed lines) jitter tolerance of (a) 1-Gb/s prototype and (b) 10-Gb/s prototype.

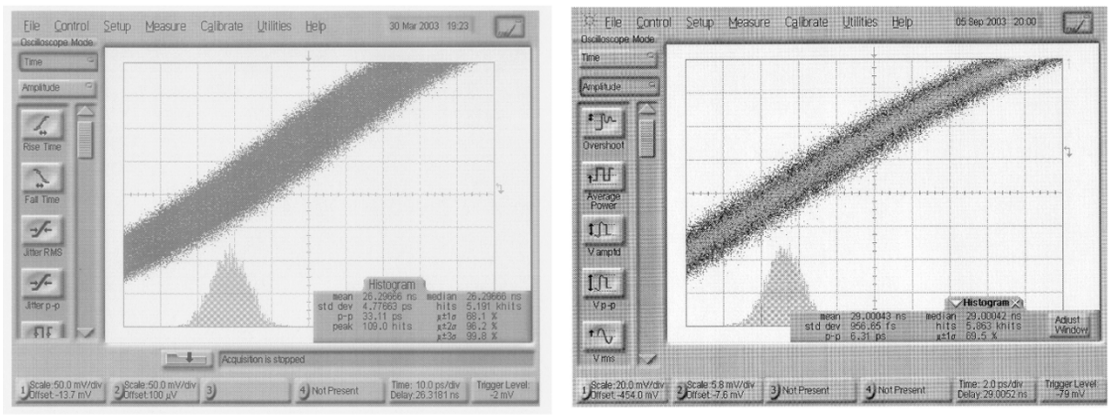

Fig. 17. Recovered clock histograms for (a) 1-Gb/s (horizontal scale: 10 ps/div, vertical scale: 50 mV/div) and (b) 10-Gb/s (horizontal scale: 2 ps/div, vertical scale: 5.8 mV/div) CDR circuits.

Figs. 15 and 16 plot the theoretical and measured jitter transfer and tolerance of both CDR circuits, respectively. The high-frequency deviation of jitter tolerance is attributed to intersymbol interference in the recovered data as well as the effect of additive noise and finite data transition times.

Fig. 17 depicts the jitter of the recovered clocks, suggesting rms values of 4.77 ps and 0.95 ps, and peak-to-peak values of 33 and 6.3 ps, respectively. Fig. 18 shows the output spectrum of the 10-Gb/s loop, suggesting a phase noise of −118 dBc/Hz at 1-MHz offset. These jitter measurements use a pseudo-random

TABLE I
THEORETICAL AND MEASURED RESULTS

	1−Gb/s CDR		10−Gb/s CDR	
	Theory	Measurement	Theory	Measurement
Jitter Transfer Corner Freq.	405 kHz	420 kHz	4.2 MHz	4.45 MHz
Peaking	0 dB	0.25 dB	0 dB	0.28 dB
Jitter Tolerance Corner Freq.	490 kHz	460 kHz	5.45 MHz	4.90 MHz
Recovered Clock Jitter	4.21 ps,rms	4.77 ps,rms	0.81 ps,rms	0.95 ps,rms

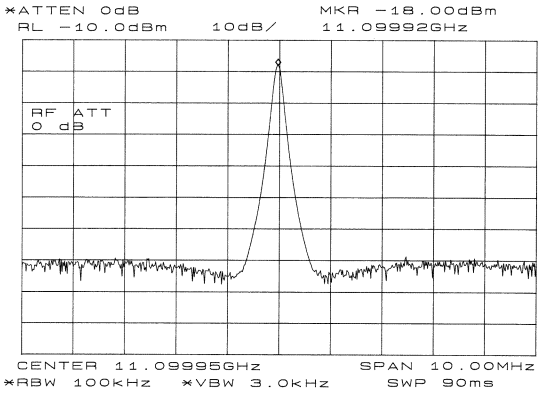

Fig. 18. Recovered clock spectrum of the 10-Gb/s prototype.

sequence length of $2^{31} - 1$. Table I summarizes the theoretical and measured results. The theoretical values of jitter generation are obtained from the linear model in [4]. As expected, the measured rms jitters are slightly higher than these predictions due to the peaking in the recovered clock spectrum.

V. CONCLUSION

A piecewise-linear model of bang-bang phase detectors is proposed that can be used in conjunction with large-signal behavior of the loop to predict the jitter characteristics and other parameters. Experimental results measured on 1-Gb/s and 10-Gb/s CDR prototypes indicate that the model provides reasonable accuracy while carrying an intuitive view of the behavior.

REFERENCES

[1] J. D. H. Alexander, "Clock recovery from random binary data," *Electronics Letters*, vol. 11, pp. 541–542, Oct. 1975.
[2] R. C. Walker, "Designing bang-bang PLL's for clock and data recovery in serial data transmission systems," in *Phase-Locking in High-Performance Systems*, B. Razavi, Ed: IEEE Press, 2003, pp. 34–45.
[3] B. Razavi, *Design of Integrated Circuits for Optical Communications*. New York, NY: McGraw-Hill, 2002.
[4] J. McNeill, "Jitter in ring oscillators," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 870–879, June 1997.