High-Speed Circuit Designs for Transmitters in Broadband Data Links

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***Abstract*—Various high-speed techniques including internal peaking, differentially stacked inductor, and dual-loop PLL for wireline communications are proposed, analyzed, and verified by means of three independent circuits. A multiplexer incorporates multiple peaking techniques and gate control switching to achieve an operation speed of 20 Gb/s while consuming 22 mW from a 1.8-V supply. A voltage-controlled oscillator employing differentially stacked inductor accomplishes a phase noise of −90 dBc/Hz at 1-MHz offset with a minimum power of 1 mW. A clock multiplication unit utilizes dual-loop architecture as well as a third-order loop filter, arriving at an output jitter of 0.2 ps, rms (0.87 ps, rms de-embedding 0.84 ps, rms from the instruments) and 4.5 ps, pp while consuming 40 mW from a 1.8-V supply.**

***Index Terms*—Clock multiplication unit (CMU), multiplexer (MUX), phase-locked loop (PLL), transmitter, voltage-controlled oscillator (VCO).**

I. Introduction

THE continuous growth of broadband data communications has driven optical systems to operate at tens of gigabits per second [1], [2]. A transmitter poses difficult challenges in many aspects since it must deliver a full-rate data with reasonable swings. Fig. 1 illustrates a typical realization of a wireline transmitter, composing multiple ranks of multiplexers (MUXes) and clock multiplication unit (CMU) providing the clocks. The last-stage MUX and the voltage-controlled oscillator (VCO) play critical roles simply due to the high-speed requirement. Until now, most of these blocks are implemented with bipolar, GaAs, or InP technologies [3], [4]. Recently, some realizations with advanced CMOS technologies begin to appear in the literature [5], [6], but they either overstress the devices with high supply voltages or consume significant power. Meanwhile, the CMU circuit also has an important influence on the overall performance of a transmitter, since its jitter would transport to the data output directly. To relax the speed and precision requirements, modern designs sometimes omit the final retimer flipflop and use a half-rate CMU [7]. Even so, realizing such a phase-locked loop (PLL) in CMOS is not trivial at all since it involves high-speed (e.g., frequency divider) and low-noise (e.g., jitter suppression) designs simultaneously. To the author's best knowledge, no PLL operating at 20 GHz or beyond has ever been demonstrated in 0.18-μm CMOS.

This paper explores the speed limitation of CMOS technology, revealing its potential of taking over territories so far claimed by compound devices. It presents the design, analysis, and experimental verification of three key blocks: a 20-Gb/s 2-to-1 MUX, a 40-GHz VCO, and a 20-GHz CMU circuit. All of them are realized in standard 0.18-μm CMOS Technology. The MUX incorporates multiple resonance techniques, achieving an rms jitter of 1.57 ps and a power consumption of 22 mW. The VCO arrives at a phase-noise of −90 dBc/Hz at 1-MHz offset by using a differentially stacked inductor. The CMU circuit utilizes dual loops to minimize the jitter while maintaining a wide acquisition range, resulting in an output jitter of 0.2 ps, rms (0.87 ps, rms de-embedding 0.84 ps, rms from the instruments) while consuming 40 mW from a 1.8-V supply.

Sections II, III, and IV describe the design and analysis of the MUX, VCO, and CMU circuits, respectively. Section V presents the experimental results, and Section VI summarizes these works with a conclusion.

II. 20-Gb/s MUX

A. Internal Peaking Technique

For a differential pair, it is well known that the inductive peaking technique can be used to improve the bandwidth of the output port, and ideally a maximum bandwidth extension of 82% is achievable [8]. However, a conventional current-steering selector would still suffer from speed limitation due to the capacitance of internal nodes. As illustrated in Fig. 2(a), when the clock turns on, the parasitic capacitance C at node A must be discharged so as to lower V_A until either M_1 or M_2 is on. The −3-dB bandwidth ω_1 is thus given by $(r_{O3}C)^{-1}$, where r_{O3} denotes the output resistance of M_3. The relatively large capacitance C considerably degrades the the performance at high speed.

To raise the bandwidth associated with the internal nodes, a series inductor L is inserted between the clock and data stages as shown in Fig. 2(b) [4], [6], splitting C into two components [9]. Assuming the M_1–M_2 pair and M_3 contribute approximately equivalent capacitance $(C/2)$, we choose L to resonate with $C/2$ at $2\omega_1$ to minimize peaking: at $\omega = 2\omega_1$, the L-$C/2$ network acts as a short, absorbing all of I_{in} and causing $|V_A/I_{\text{in}}| = [2\omega_1(C/2)]^{-1} = r_{O3}$; at $\omega = 2\sqrt{2}\omega_1$, the π network of $C/2$-L-$C/2$ resonates, forcing all of I_{in} to flow through r_{O3} and making $|V_A/I_{\text{in}}| = r_{O3}$. (The two capacitors in the π network carry equal and opposite currents.) Quantitative analysis reveals that

$$\left|\frac{V_A}{I_{\text{in}}}\right|(j\omega) = \frac{4r_{O3}}{\sqrt{\left[4-\left(\frac{\omega}{\omega_1}\right)^2\right]^2+\left[4\left(\frac{\omega}{\omega_1}\right)-\frac{1}{2}\left(\frac{\omega}{\omega_1}\right)^3\right]^2}} \quad (1)$$

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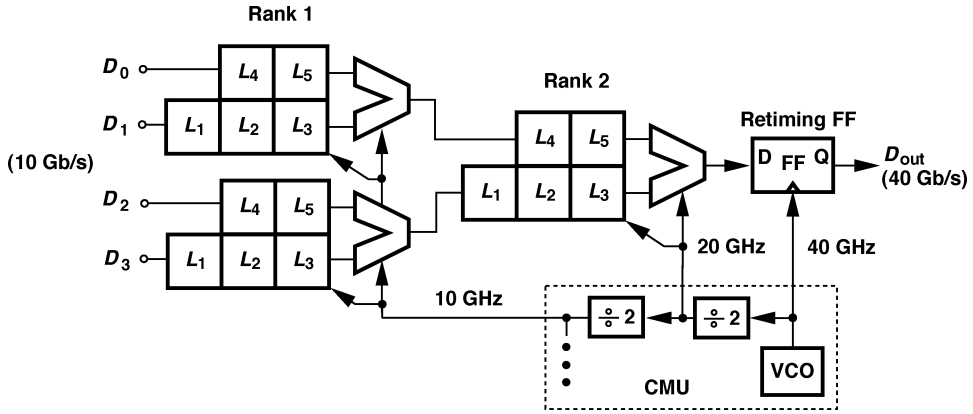


Fig. 1. Conventional realization of a 40-Gb/s transmitter with 4:1 MUX.

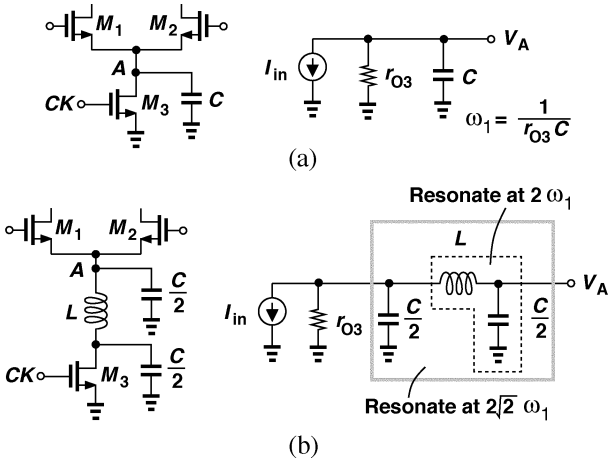


Fig. 2. Internal node behavior (a) without and (b) with series inductor.

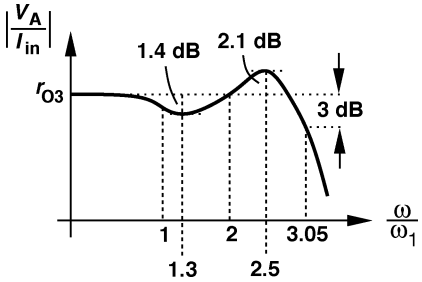


Fig. 3. Transfer function of the circuit in Fig. 2(b).

and the transfer function is plotted in Fig. 3. The peak (2.1 dB) and valley (-1.4 dB) occur at $2.5\omega_1$ and $1.3\omega_1$, respectively. The -3-dB bandwidth is approximately equal to $3.05\omega_1$. In other words, this technique extends the bandwidth associated with the internal node A by a factor of 3.

In practice, the inductor L introduces parasitic capacitance and loss, limiting the bandwidth improvement to a lesser extent. The large-signal behavior of a MUX restricts the bandwidth enhancement as well. The capacitance C may not be split evenly either. For example, if M_3 contributes $C/3$ and the M_1–M_2 pair $2C/3$ to node A, we could choose the L-$2C/3$ network to resonate at $1.5\omega_1$, arriving at a 2.3-times bandwidth improvement of the internal node with passband ripple of less than 0.2 dB.

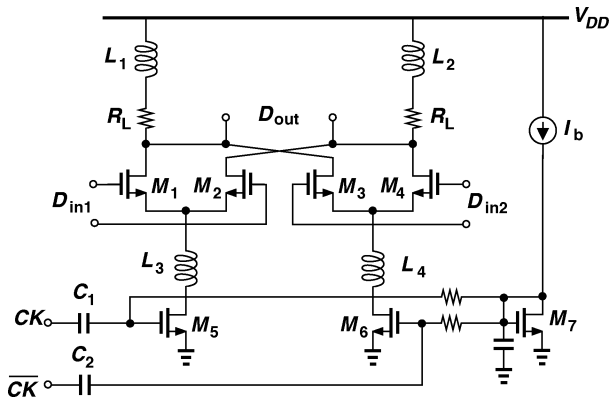


Fig. 4. Proposed selector.

Nonetheless, careful design and simulations are required in such a high-speed block.

B. 2-to-1 MUX Design

The proposed selector is depicted in Fig. 4, where the tail current source is eliminated to relax the voltage headroom requirement. Current switching in M_5–M_6 is accomplished by gate control or so-called "Class-AB" operation. Since the tail current source is removed, M_5–M_6 can be much narrower, presenting a smaller capacitance to the clock buffer. Such Class-AB current sources create a large peak current and provide greater voltage swings at the output. The coupling capacitors C_1 and C_2 are realized as fringe structure [10] using metal-2 through metal-5 layers. Electromagnetic simulation indicates a bottom-plate capacitance of only 5% on each side. Table I summarizes the design values for the selector of Fig. 4. The sizes of M_5–M_6 are chosen to accommodate the required peak current, which along with the resistor R_L determines the output swing. Transistors M_1–M_4 are made as small as possible (as long as they can afford complete steering of the peak currents) to minimize the parasitic capacitance. Inductors $(L_1$–$L_4)$ are implemented as single-ended structures since the symmetric ones are prone to difficult routings. The process and temperature variations of the load resistor R_L would deviate the circuit from the optimal performance. Simulation shows that an eye closure of 1 dB is observed in this design for a $\pm 18\%$ variation of R_L.

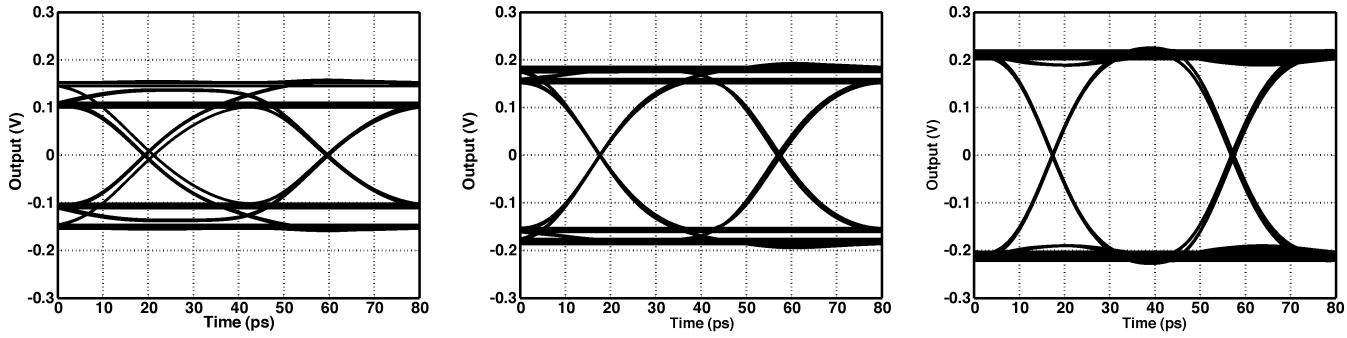


Fig. 5. Output data for: (a) conventional current-steering selector; (b) current-steering selector with inductive peaking; (c) proposed selector.

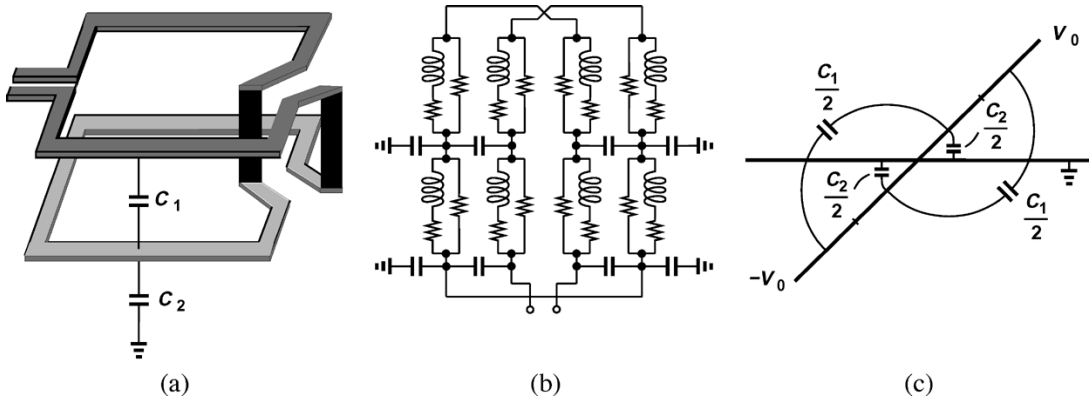


Fig. 6. (a) Proposed differentially stacked inductor; (b) its model; (c) the voltage profile.

TABLE I
DESIGN PARAMETERS OF THE PROPOSED SELECTOR

Parameter	Value
$(W/L)_{1-4}$	12 um/0.18 um
$(W/L)_{5-6}$	18 um/0.18 um
I_{bias} for M_{5-6}	2 mA
R_L	100 Ω
L_{1-2}	0.6 nH
L_{3-4}	1.2 nH
C_{1-2}	180 fF

Fig. 5 plots the simulated output data of three different selectors operating at 25 Gb/s with the same power consumption. Each circuit is optimized with slight loading adjustment to reach a most opening eye. It is clear that the proposed selector introduces much less intersymbol interference (ISI) with largest swing.

III. 40-GHz VCO

A. Differentially Stacked Inductors

The performance of an LC oscillator heavily depends on the quality of the inductors. Among the various inductor topologies, a stacked inductor provides a high f_{SR} by reducing the equivalent capacitance [11], but the asymmetric structure limits its application in differential circuits. On the other hand, a differential (balanced) inductor achieves a higher Q by reducing the effect of substrate loss [12] and is well-suited for a differential stimulus. However, the interwinding capacitance somewhat lowers the f_{SR}.

To resolve the foregoing dilemma, a topology combining both structures is proposed as shown in Fig. 6(a). Here, two layers of spirals are stacked differentially to preserve symmetry, allowing differential excitation. The strong mutual coupling between the top and bottom layers forms a total inductance of nearly 4 times that of a single-layer single-turn inductor. Such a structure can be modeled by distributed elements as depicted in Fig. 6(b). Here, the inductance, layer-to-layer capacitance C_1, layer-to-substrate capacitance C_2, and loss are decomposed evenly into eight segments. Assuming perfect coupling between the two layers, we obtain the differentially stimulated voltage profile [Fig. 6(c)], where C_1 experiences a constant voltage V_0 across it and C_2 a linear voltage variation from $-V_0/2$ to $V_0/2$. To calculate the equivalent capacitance, we equate the total electric energy stored in the structure for a peak differential voltage of $2V_0$ to $C_{\rm eq}(2V_0)^2/2$ and obtain

$$E_{\rm elec} = \frac{1}{2}C_1V_0^2 + 2\int_0^{\frac{C_2}{2}} \frac{1}{2}\left(\frac{x}{(C_2/2)}\frac{V_0}{2}\right)^2 dx = \frac{1}{2}C_{\rm eq}(2V_0)^2 \tag{2}$$

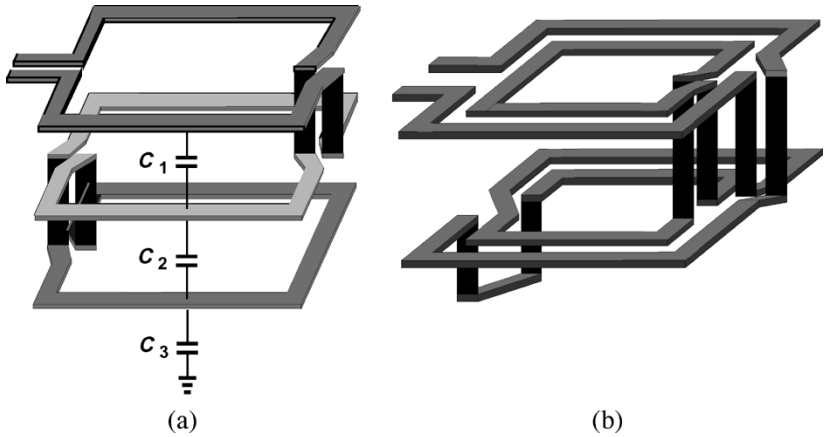


Fig. 7. Differentially stacked inductors with multiple layers and turns. (a) Three layers. (b) Multiple turns and layers.

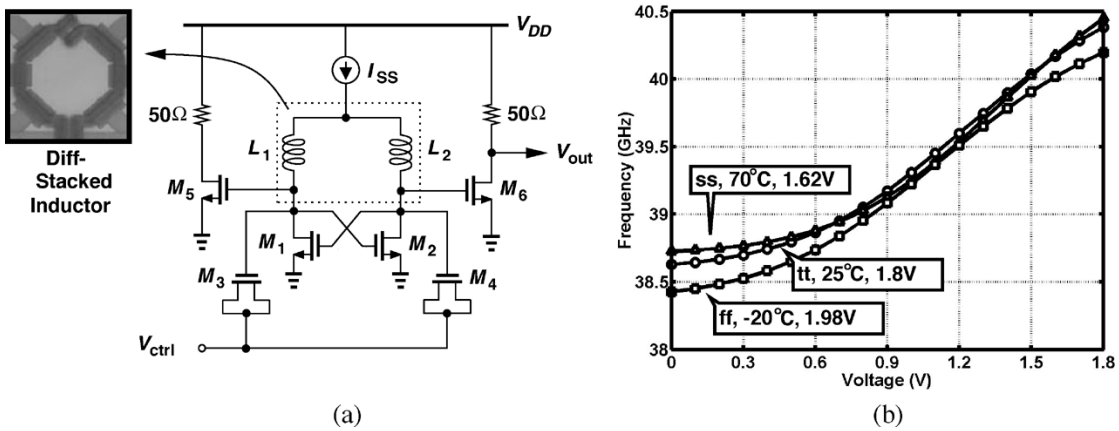


Fig. 8. (a) VCO design and its parameters. (b) Tuning curves under process, temperature, and supply variations.

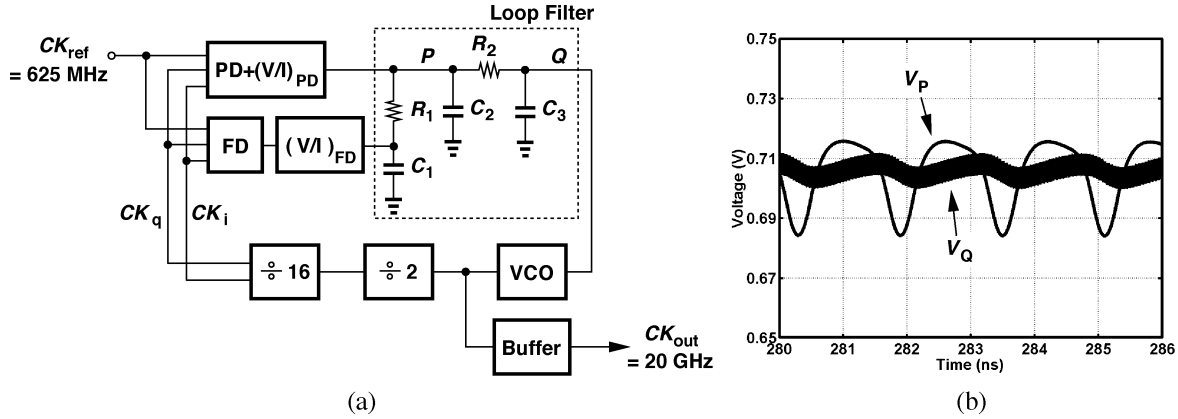


Fig. 9. (a) CMU architecture. (b) Simulated waveforms of V_P and V_Q.

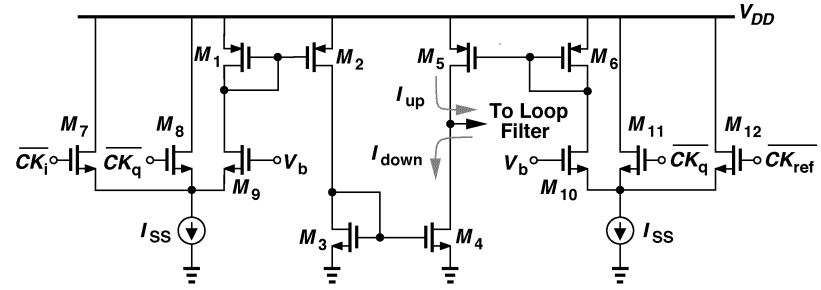
yielding the equivalent capacitance as

$$C_{\text{eq}} = \frac{C_1}{4} + \frac{C_2}{48}. \tag{3}$$

Equation (3) reveals that C_1 impacts the self-resonance frequency 12 times as much as C_2. Note that the total inductance remains relatively constant for different distances between the two layers, because the lateral dimensions of the inductor are much greater than the vertical one [11]. Thus, it is desirable to place the two layers of spirals far from each other, consistent with the result of simple stacked inductors in [11].

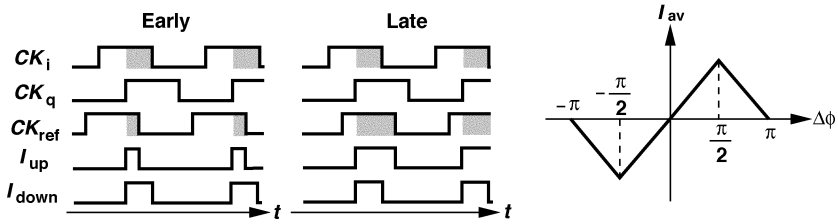
The differentially stacked topology can be further extended to multiple-layer stacks as well. For a single-turn differential inductor with n stacked spirals, the equivalent capacitance is given by

$$C_{\text{eq,multi}} = \sum_{k=1}^{n-1} \left(\frac{n-k}{n}\right)^2 C_k + \frac{C_n}{12n^2}. \tag{4}$$



Parameter	Value
$(W/L)_{1\text{-}2}$ & $(W/L)_{5\text{-}6}$	72 um/0.6 um
$(W/L)_{3\text{-}4}$	30 um/0.6 um
$(W/L)_{7\text{-}12}$	10 um/0.18 um

(a)



(b)

(c)

Fig. 10. (a) Phase detector and *V*-to-*I* converter; (b) timing diagram; (c) its characteristic.

TABLE II
VCO AND INDUCTOR PARAMETERS

VCO Parameters	
$(W/L)_{1-2}$	1.2 um/0.8 um
$(W/L)_{3-4}$	2 um/0.5 um
$(W/L)_{5-6}$	6 um/0.18 um
L_{1-2}	0.2 nH
I_{SS}	$\geq$ 0.8 mA
Inductor Parameters	
Outer Diameter	69 um
Line Width	5 um
Upper Layer	Metal6
Lower Layer	Metal2 + Metal3

TABLE III
CMU DESIGN PARAMETERS

Parameter	Value
$K_{PD+(V/I)}$	0.4/2π mA/rad
K_{VCO}	2π×0.8 Grad/s/V
R_1	2.4 kΩ
C_1	65 pF
C_2	1.4 pF
R_2	1.52 kΩ
C_3	0.5 pF
Phase Margin	68°
Loop Bandwidth	5.3 MHz

Fig. 7(a) illustrates an example of three layers. Similarly, it is possible to implement a structure with multiple turns and layers [Fig. 7(b)]. Due to the complexity, these structures require electromagnetic simulators to build accurate models.

B. VCO Design

As illustrated in Fig. 8, the VCO incorporates a cross-coupled pair with the proposed inductor and MOS varactors. To further increase Q, the inductor is implemented as octagonal shape, and the bottom layer is realized as parallel shunt spirals, i.e., metal-2 and metal-3 connected through vias. To reduce the coupling to the substrate, a ground shield made of polysilicon sticks with minimum gap width is placed under the spirals in the direction perpendicular to the current flow [13]. The design values of the VCO and the inductor are listed in Table II. In this prototype, 50-Ω termination resistors are used in both the real and dummy buffers. Such an imbalanced loading may cause asymmetric capacitance seen at the two terminals of the VCO tank according to the Miller effect. Fortunately, this issue only contributes negligible difference because 1) the gain of the buffers is low (-18 dB), and 2) the gate-drain capacitances are quite small (2.2 fF). Nevertheless, a 25-Ω loading resistor could be used in the dummy buffer to achieve a better balance if necessary.

To stabilize the supply, control voltage, and other DC lines, large bypass capacitors ($\approx$16 pF in total) is placed on chip in this prototype. Fig. 8(b) shows the tuning characteristics under process, temperature, and supply variations. The maximum deviation of center frequency is about $\pm$0.15%. Regulators could be used in future design to minimize the supply sensitivity.

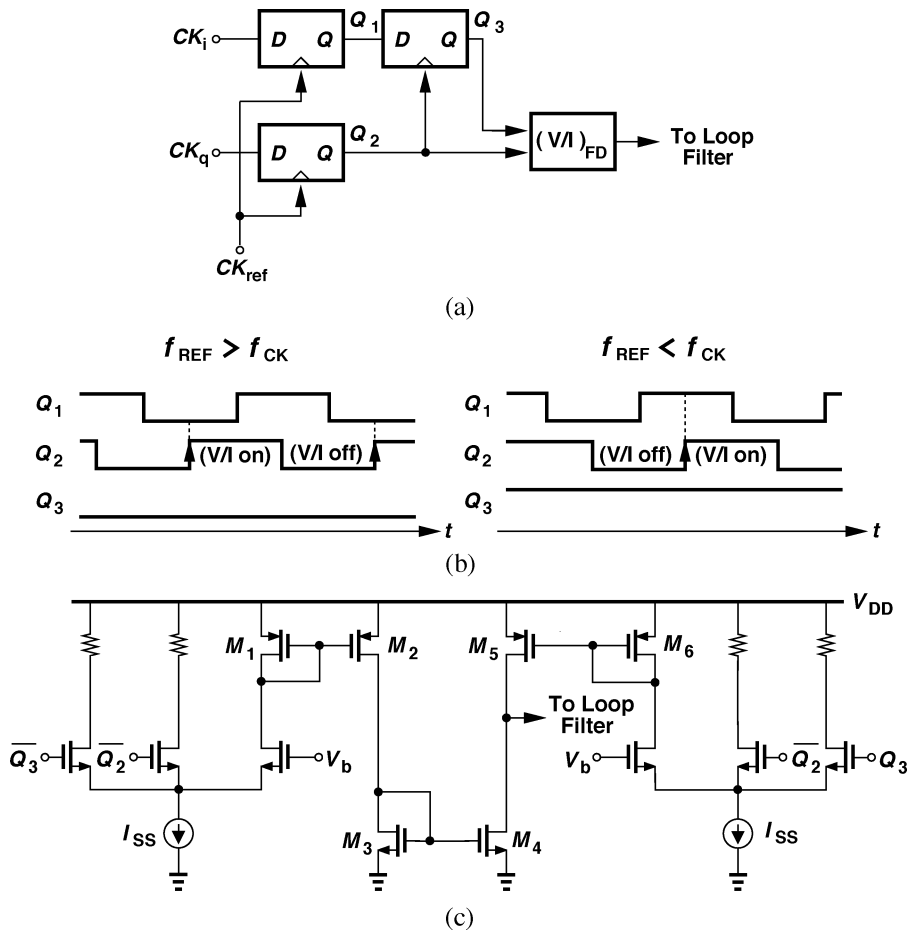


Fig. 11. (a) Frequency detector; (b) its operation; (c) realization of $(V/I)_{\mathrm{FD}}$.

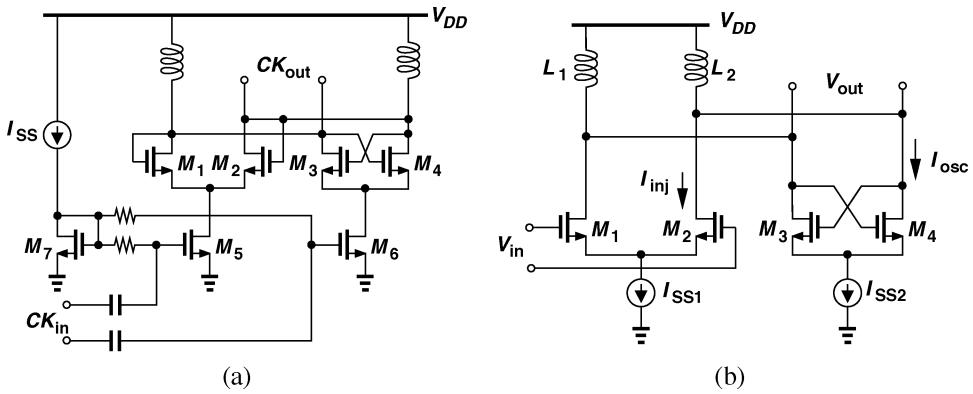


Fig. 12. (a) First ÷2 circuit. (b) Clock buffer.

IV. 20-GHz CMU

A. Architecture

A conventional phase-locked loop (PLL) with type IV phase/frequency detector (PFD) provides simplicity and infinite capture range. However, the finite pulsewidth required to drive the charge pump restricts the PFD from being operated at high speed.

Fig. 9(a) depicts the proposed CMU architecture. Here, the phase and frequency detection are decomposed to minimize jitter while maintaining a wide acquisition range. The frequency detector (FD) drives the VCO frequency toward the desired value, and the phase detector (PD) locks the loop afterwards. A third-order loop filter is employed to suppress the ripple on the control line, and all the passive components are realized on chip. The VCO is followed by a chain of frequency dividers with a total modulus of 32. Note that to minimize the noise and power, the PD and its V/I converter are merged together and the FD automatically disables itself when the loop is locked. Table III summarizes the design parameters, where the loop bandwidth is equal to 5.3 MHz and the third-order loop filter suppresses the control line ripple by 10 dB [14]. Fig. 9(b)

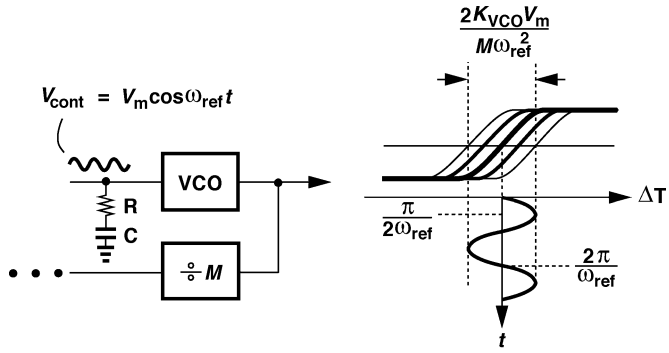


Fig. 13. Jitter due to control-line ripple.

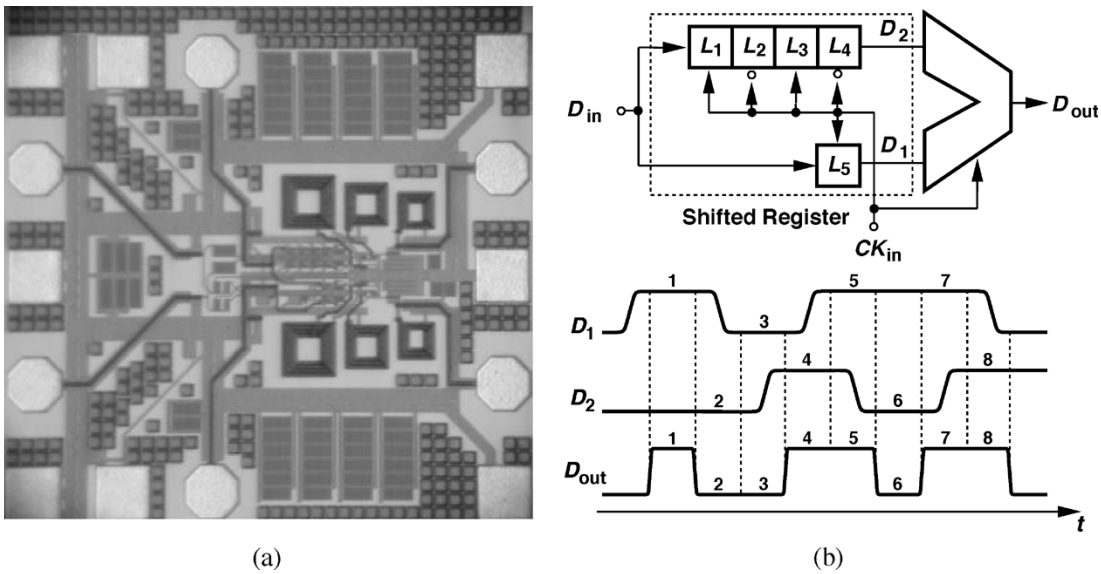


Fig. 14. (a) Chip photo of MUX. (b) Generation of input data.

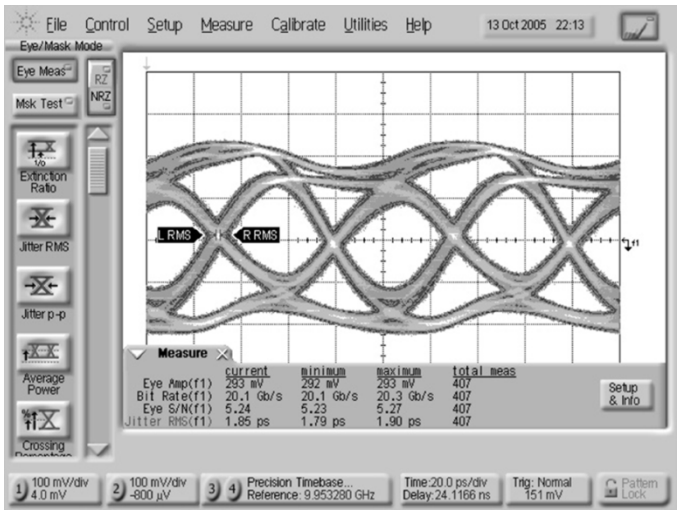


Fig. 15. Output waveform of the MUX operating at 20 Gb/s.

depicts the voltage waveforms of nodes P and Q in Fig. 9(a) under locked condition. Simulation shows that the peak-to-peak jitter (due to control-line ripple) in this design is approximately 320 fs, whereas that of an identical PLL with second-order loop filter is as large as 1.1 ps.

B. Building Blocks

PD and V/I Converter: The PD and V/I converter co-design is shown in Fig. 10(a). The quadrature clocks CK_i and CK_q, provided by the last stage of dividers, create quarter-period reference pulses, while CK_q and the input reference $CK_{\rm ref}$

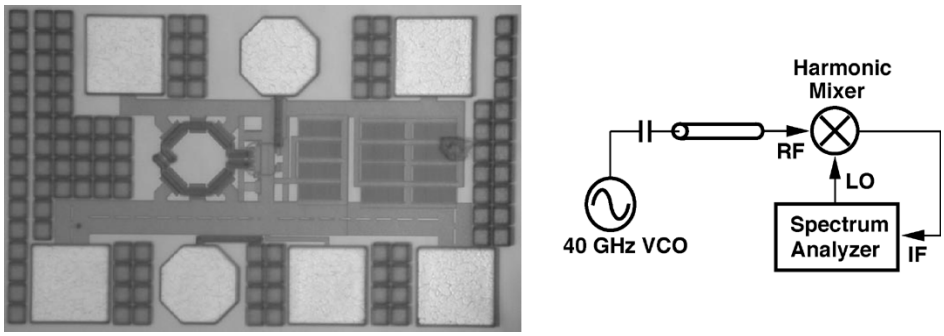


Fig. 16. Chip micrograph of VCO and the testing setup.

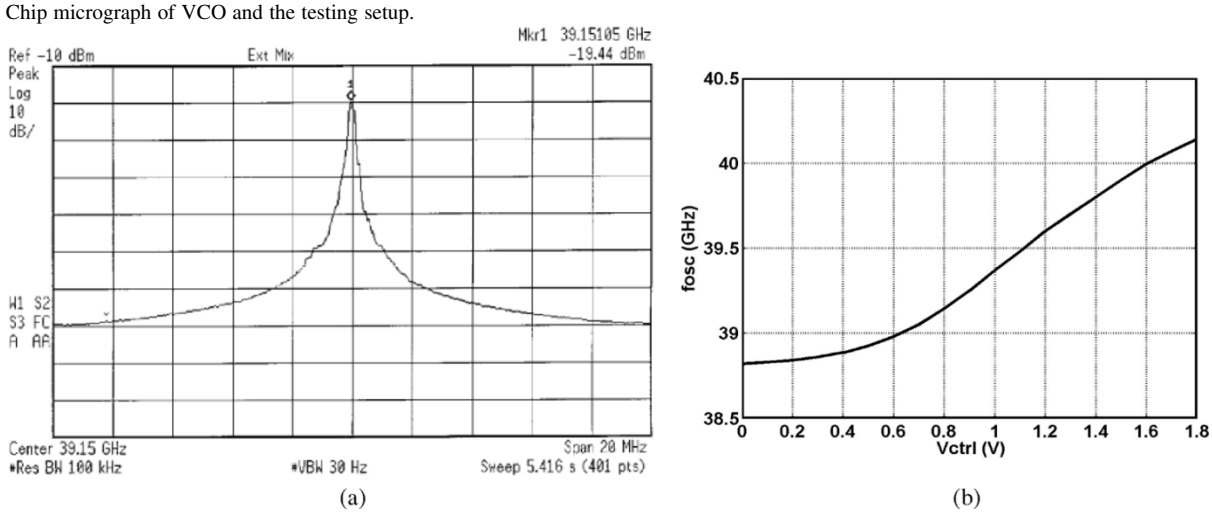


Fig. 17. (a) Spectrum. (b) Tuning curve of the 40-GHz VCO.

generate pulses whose widths are proportional to the phase error [Fig. 10(b)]. As a result, a linear characteristic of Fig. 10(c) is obtained, and $CK_{\rm ref}$ eventually aligns with CK_i upon lock.

It can be shown that skews between $I_{\rm up}$ and $I_{\rm down}$ paths (M_5–M_6 and M_1–M_4, respectively) disturbs the VCO control line periodically, and the channel-length modulation of M_1–M_6 causes control-line ripple as well. In this design, the dimension of M_1–M_6 is chosen as a compromise between these two effects such that the jitter is minimized. Transistor sizes are listed in Fig. 10(a). Note that the input signals ($\overline{CK_i}$, $\overline{CK_q}$, and $\overline{CK_{\rm ref}}$) have swings of 0.6 V (from 1.2 to 1.8 V), and V_b is set to 1.5 V.

Frequency Detector: As shown in Fig. 11(a), the frequency detector (FD) produces the polarity of beat frequency, and inject a current to the loop filter accordingly. Here, CK_i and CK_q are sampled by the reference clock, generating two periodic signals Q_1 and Q_2 if the two frequencies are not equal [15]. Using Q_2 to sample Q_1, we obtain the signal Q_3 that indicates the polarity [Fig. 11(b)].

To minimize the disturbance on VCO, the frequency acquisition should be turned off upon lock. Observing that Q_2 would stay low under locked condition, we apply Q_2 to the V/I converter $[V/I_{\rm FD}]$ as well and have it disabled when the loop is locked. In other words, the V/I converter activates for 50% of the time during tracking, and automatically switches off when the frequency acquisition is accomplished [16]. The V/I converter associated with the FD is depicted in Fig. 11(c). Note that it bears a pumping current 4 times larger than that of the PD to ensure the FD loop dominates during frequency acquisition.

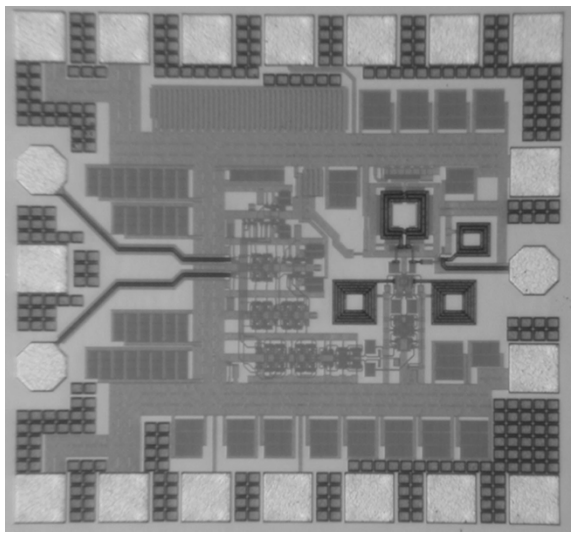
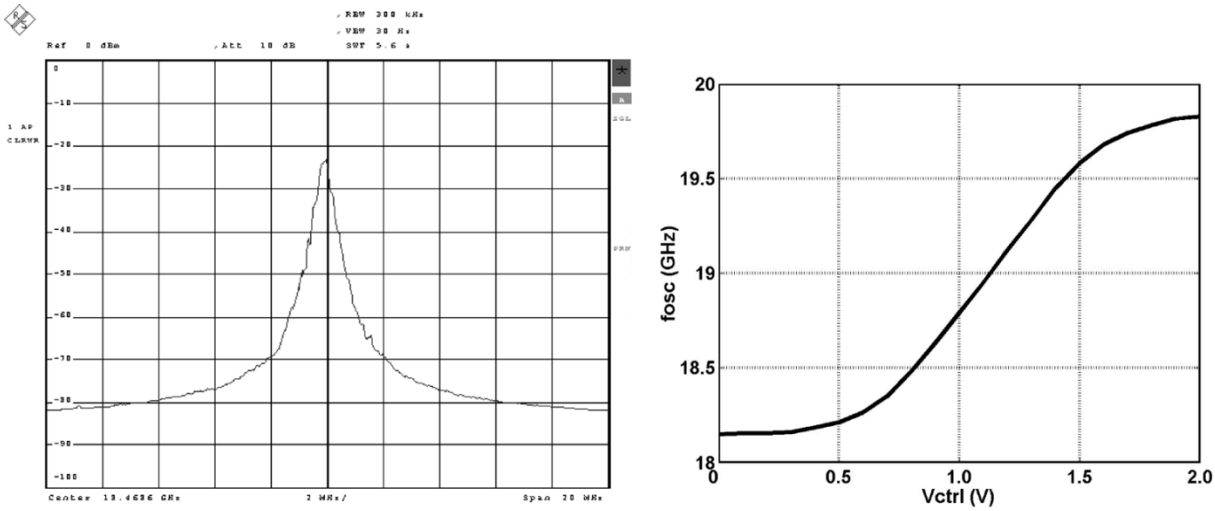


Fig. 18. Die photo of CMU.

VCO/Divider/Buffer: The 20-GHz VCO is realized as an LC oscillator with a differentially stacked inductor described in Section III. The first divider stage is implemented as a Miller divider with inductive loads [17], as depicted in Fig. 12(a). Simulation shows that this topology achieves an operation range of 7 GHz, well exceeding the VCO tuning range.

In most cases, the high-speed clock must drive a large loading, including selectors and their retiming latches. Here,



(a) (b)

Fig. 19. (a) Free-running spectrum (center: 18.47 GHz, span: 20 MHz, RBW: 300 kHz). (b) Tuning range of the VCO in the CMU circuit.

an inductively loaded buffer as shown in Fig. 12(b) is proposed to ensure a large swing. The inductor L_1 and L_2 resonates at 20 GHz, whereas the cross-coupled pair M_3–M_4 cancels part of the loss and further increases the swing. It is interesting that this circuit can be also recognized as an injection-locked oscillator. It can be shown that if $I_{SS1} = 3I_{SS2}$ and $Q \approx 6$, a locking range of 25% is achieved [18]. This range is approximately 3 times larger than the VCO tuning range, suggesting a safe locking under any circumstance.

C. Considerations

Reference Feedthrough: The sources that generates control line ripple include current mismatch and pulse skew of the *V*-to-*I* converter. Synchronized with the input reference clock, the ripple on the control line modulates the VCO frequency, resulting in clock jitter directly.

Consider a periodic ripple, $V_m \cos \omega_{\rm ref} t$, imposed on a control voltage of a locked loop [Fig. 13(a)]. The excessive phase caused by the ripple is given by

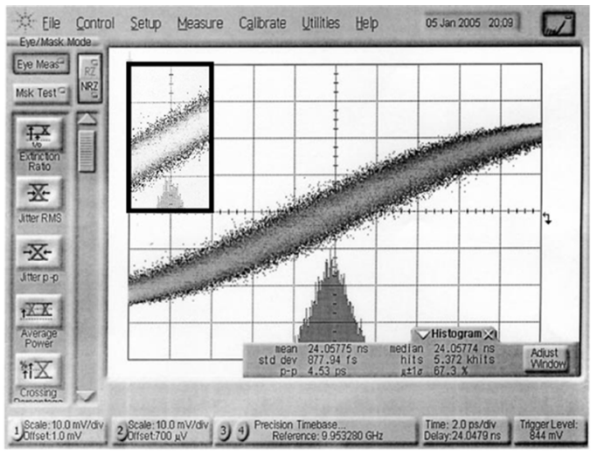
$$\Delta\phi(t) = \int_0^t K_{\rm VCO} V_m \cos \omega_{\rm ref} \tau d\tau c \frac{K_{\rm VCO} V_m}{\omega_{\rm ref}} \sin \omega_{\rm ref} t. \quad (5)$$

Noting that (absolute) jitter is defined as the deviation of the zero-crossing point of the output clock, we arrive at

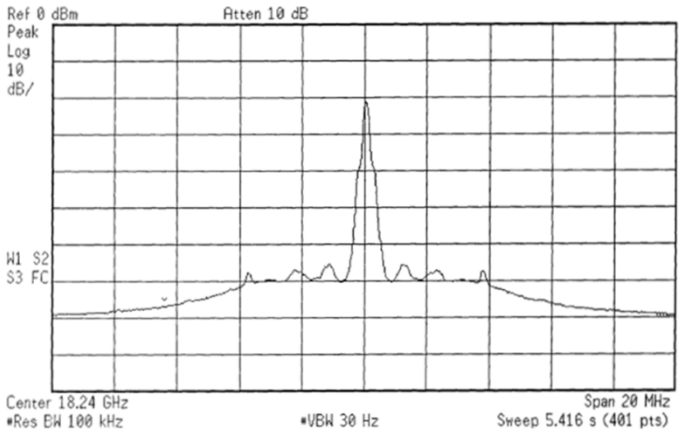
$$\Delta T(t) = \frac{\Delta\phi(t)}{M\omega_{\rm ref}} = \frac{K_{\rm VCO} V_m}{M\omega_{\rm ref}^2} \sin \omega_{\rm ref} t \quad (6)$$

where M denotes the divide ratio. As illustrated in Fig. 13(b), the zero-crossing point "waggles" around the *average* point with a frequency of $\omega_{\rm ref}/2\pi$. For large divide ratio M, the rms jitter can be obtained as

$$(\Delta T)_{\rm rms}^2 = \frac{\omega_{\rm ref}}{2\pi} \int_0^{\frac{2\pi}{\omega_{\rm ref}}} \frac{K_{\rm VCO}^2 V_m^2}{M^2 \omega_{\rm ref}^4} \sin^2 \omega_{\rm ref} t dt. \quad (7)$$



(a)



(b)

Fig. 20. (a) Clock jitter measurement (horizontal scale: 2 ps/div, vertical scale: 10 mV/div). (b) Output spectrum under locked condition.

It follows that

$$(\Delta T)_{\rm rms} = \frac{K_{\rm VCO} V_m}{\sqrt{2} M \omega_{\rm ref}^2}. \quad (8)$$

TABLE IV
PERFORMANCE SUMMARY OF (A) MUX, (B) VCO, AND (C) CMU

Parameter	[20]	This Work
Max. Output Data Rate	25 Gb/s	20 Gb/s
Function	2 : 1	2 : 1
Supply Voltage	1.5 V	1.8 V
Power Diss.	44 mW	22 mW
Technology	0.12−um CMOS	0.18−um CMOS

(a)

Parameter	[21]	[22]	This Work
Frequency	43 GHz	51 GHz	40 GHz
Tunning Range	4.2%	1.2%	3.5%
Phase Noise (@ 1−MHz offset)	−90 dBc/Hz	−85 dBc/Hz	−90 dBc/Hz
Supply Voltage	≥ 1 V	≥ 1 V	≥ 1 V
Power Diss.	7 mW	1 mW	1 mW
Chip Area	N/A	0.5 mm x 0.9 mm	0.3 mm x 0.45 mm
FOM	−174 dBc/Hz	−179 dBc/Hz	−182 dBc/Hz
Technology	0.13−um Standard CMOS	0.12−um Standard CMOS	0.18−um Standard CMOS

(b)

Parameter	[23]	This Work
Output Freq.	20 GHz	20 GHz
Multiply Ratio	32	32
Clock Jitter	0.65 ps,rms 4.9 ps,pp	0.2 ps,rms < 4.53 ps,pp
Supply Voltage	1.5 V	1.8 V
Power Diss	480 mW	40 mW
Chip Area	1.7 mm^2	0.64 mm^2
Technology	0.13−um CMOS	0.18−um CMOS

(c)

Since the excessive phase reaches a maximum at $t = (2k + 1)\pi/(2\omega_{\rm ref})$ where $k = 0, 1, 2, \ldots$, the peak-to-peak jitter can be calculated as

$$(\Delta T)_{\rm pp} = \frac{2K_{\rm VCO}V_m}{M\omega_{\rm ref}^2}. \tag{9}$$

Equations (8) and (9) reveal that the jitter caused by the reference feedthrough is proportional to the ripple amplitude V_m, disclosing the advantage of higher-order loop filters that reduce the control line disturbance without degrading the stability.

V. EXPERIMENTAL RESULTS

All three circuits have been fabricated in 0.18-μm CMOS technology and tested on a high-speed probe station. The on-chip high-speed lines are realized as 50-Ω microstrip structures to absorb the routing capacitance. Spiral inductors are made with line widths commensurate with the electromigration limitations to minimize the parasitics, and symmetry is preserved through careful layout. The measurements are summarized in the following subsections.

A. 20-Gb/s MUX

Fig. 14(a) shows the die photo of the MUX, which measures 0.7×0.7 mm^2. Due to the lack of dual PRBS generators,

the arrangement of retiming latches is modified to provide two input data sequences with sufficient randomness [Fig. 14(b)]. The latches are realized with resistive loads and gate-controlled current switching, where the bias circuit is shared. Fig. 15 depicts the differential output waveform operating at 20 Gb/s, suggesting an rms and peak-to-peak jitter of 1.85 ps and 11.6 ps, respectively. Note that the 10-Gb/s input itself (from the PRBS generator) has an rms jitter of 1.5 ps and a peak-to-peak jitter of 11.5 ps. The total power consumption (excluding the output buffer) is 22 mW from a 1.8-V supply.

B. 40-GHz VCO

Shown in Fig. 16(a) is the chip micrograph of the VCO, occupying an area of 0.3×0.45 mm^2. A spectrum analyzer and harmonic mixer are used in this measurement, as illustrated in Fig. 16(b). The VCO achieves a phase noise of -90 dBc/Hz at 1-MHz offset while consuming 1 mW from a 1.3-V supply. Fig. 17 plots the spectrum and the tuning characteristic. A range of 1.4 GHz is obtained when the supply voltage is equal to 1.8 V. The output power of the VCO reads -19.4 dBm from the spectrum analyzer, in the presence of a 2.5-dB loss from the cables and the connectors. The *in-situ* measurement [19] suggests that the inductor along with the varactor presents a Q of 12 at 40 GHz.[1] The VCO begins to oscillate at a tail current of 450 μA with a 1.0-V supply. This design presents a figure of merit $[\mathcal{L}(\Delta f/f)^2 P]$ of -182 dBc/Hz.

C. 20-GHz CMU

Fig. 18 shows the die of the CMU circuit, which measures 0.8×0.8 mm^2 including pads. The loop filter is built on-chip to avoid external noise. Skews and jitters are minimized through symmetric layout and balanced routing. The circuit consumes 40 mW from a 1.8-V supply.

Shown in Fig. 19 is the free-running spectrum and tuning characteristic of the 20-GHz VCO, indicating phase noise of -102 dBc/Hz at 2-MHz offset and a tuning range of 1.6 GHz.[2] The output clock is plotted in Fig. 20(a), suggesting an rms and peak-to-peak jitter of 0.87 ps and 4.5 ps, respectively. However, the reference clock and the oscilloscope itself contribute an rms jitter of 0.84 ps (as shown in the inset). As a result, the circuit actually presents an rms jitter of 0.2 ps ($= \sqrt{0.87^2 - 0.84^2}$, [19]) and a peak-to-peak jitter of less than 4.5 ps. A 50% duty cycle is observed on the output clock. The output spectrum under locked condition is shown in Fig. 20(b), revealing a loop bandwidth of approximately 4.1 MHz. Note that this value is slightly less than expected because the VCO gain (K_{VCO}) is somewhat lower in the vicinity of this locking frequency (i.e., 18.24 GHz).

Table IV summarizes the performance of these three circuits and compares with several CMOS works recently reported in the literature. These circuits achieve comparable (or even better) performance with bulky devices while consuming much less power.

[1]The Q of the varactors becomes nontrivial at such a high frequency.

[2]In a redesign, the VCO frequency should be raised by 5%.

VI. Conclusion

This paper presents the design and experimental verification of a MUX, a VCO, and a PLL operating at tens of gigahertz in 0.18-μm CMOS technology. The MUX and the VCO employ various techniques to extend the available bandwidth, and the PLL incorporates a dual-loop architecture as well as a higher-order loop filter to increase the performance and robustness. These improvements provide promising solutions for next-generation wireline communications.

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