CHAPTER 10 OPERATIONAL-AMPLIFIER CIRCUITS

Chapter Outline
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10.1 The Two-Stage CMOS Op Amp

Multi-stage amplifiers
- Practical transistor amplifiers usually consist of a number of stages connected in cascade
- Input stage:
  - High input resistance to avoid signal loss due to high-resistance source
  - Voltage gain
  - Large CMRR for differential amplifiers
- Middle stages:
  - Voltage gain
  - Shifting of the dc level for required voltage swing
  - Differential to single-ended conversion if necessary
- Output stage:
  - Low output resistance to avoid loss of gain due to low-resistance load
  - Current supply required by the load
  - Sufficient voltage swing required by the load
  - Small-signal approximation may not apply
Circuit Configuration

- Most widely used op amp in VLSI circuits
- Bias circuit: $I_{REF}$ and $Q_8$
- Input stage: $Q_1$-$Q_5$
  - Active-loaded MOS differential pair
  - Differential input and single-ended output
  - Provides voltage gain and high input resistance
- Output stage: $Q_6$-$Q_7$
  - Active-loaded common-source amplifier
  - Provides voltage gain
  - High output resistance (not suitable for low-impedance loads)
- DC arrangement:
  - The bias current of the input differential pair is provided by $Q_5$
  - The bias current of the second stage is provided by $Q_7$
  - To avoid systematic (predictable) offset:
    \[
    \frac{(W/L)_6}{(W/L)_4} = 2 \frac{(W/L)_2}{(W/L)_5}
    \]
Input common-mode range and output swing

- The transistors are supposed to be in saturation for proper circuit operation
- ICMR: \(-V_{SS} + V_{OV3} + V_m - |V_{tp}| \leq V_{ICM} \leq V_{DD} - |V_{tp}| - |V_{OV5}|\)
- Output swing: \(-V_{SS} + V_{OV6} \leq v_o \leq V_{DD} - |V_{OV7}|\)

Voltage gain

- Low-frequency small-signal gain:
  \[
  G_{m1} = g_{m1} = g_{m2} \\
  R_1 = r_{o2} \parallel r_{o4} \\
  A_1 = -G_{m1}R_1 = -g_{m1}(r_{o2} \parallel r_{o4}) \\
  G_{m2} = g_{m6} \\
  R_2 = r_{o6} \parallel r_{o7} \\
  A_2 = -G_{m2}R_2 = -g_{m6}(r_{o6} \parallel r_{o7}) \\
  A_i = A_1A_2 = g_{m1}(r_{o2} \parallel r_{o4})g_{m6}(r_{o6} \parallel r_{o7})
  \]

- Amplifier prototype:
  - Input resistance: \(R_i = \infty\)
  - Output resistance: \(R_o = r_{o6} \parallel r_{o7}\)
  - Transconductance: \(G_m = -g_{m1}(r_{o2} \parallel r_{o4})g_{m6}\)

- Common-mode rejection ratio:
  \[
  CMRR = g_{m1}(r_{o2} \parallel r_{o4}) \cdot 2g_{m3}R_{SS}
  \]
Frequency response

- Poles and zeros
  
  \[
  C_1 = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_{gs6} \\
  C_2 = C_{db6} + C_{db7} + C_{gs7} + C_z
  \]

  \[
  f_{p1} \approx \frac{1}{2\pi R_1 G_{m2} R_2 C_C}
  \]

  \[
  f_{p2} \approx \frac{1}{2\pi} \frac{G_{m2}}{C_2}
  \]

  \[
  f_{z1} \approx \frac{1}{2\pi} \frac{G_{m2}}{C_C}
  \]

  → \( f_{p2} \) decreases for a capacitive load
  → May result in stability issue

- Unity-gain frequency for a dominant pole case

  \[
  f_r \approx |A_r| f_{p1} = \frac{1}{2\pi} \frac{G_{m1}}{C_C}
  \]

  \[
  \frac{G_{m1}}{C_C} < \frac{G_{m2}}{C_2} \quad \text{and} \quad G_{m1} < G_{m2}
  \]

- Phase margin

  \[
  \phi_{p2} = -\tan^{-1}(f_r / f_{p2})
  \]

  \[
  \phi_z = -\tan^{-1}(f_r / f_z)
  \]

  \[
  \phi_{total} = 90^\circ + \tan^{-1}(f_r / f_{p2}) + \tan^{-1}(f_r / f_z)
  \]

  \[
  PM = 180^\circ - \phi_{total} = 90^\circ - \tan^{-1}(f_r / f_{p2}) - \tan^{-1}(f_r / f_z)
  \]
Phase margin improvement technique
- Adding a series resistance in the feedback path
- The zero is defined by

\[ \frac{V_{i2}}{R + \frac{1}{sC}} = G_{m2}V_{i2} \quad \Rightarrow \quad s = \frac{1}{\frac{1}{C_C} \left( \frac{1}{G_{m2}} - R \right)} \]

- The zero can be moved toward higher frequencies for better phase margin

**Slew rate**
- Slew rate is defined as the maximum voltage change rate at output
- Associated with charging/discharging time of $C_C$
- Extreme cases:
  - Limited by bias current of $Q_5$ (typical case): $SR = I/C_C$
  - Limited by bias current of $Q_7$: $SR = I_f/C_C$
- Relationship between $SR$ and $f_t$
  - $SR = 2\pi f_t V_{OV} = \omega V_{OV}$
  - Slew rate is determined by the overdrive voltage for a given unity-gain frequency
  - PMOS devices are preferred for the differential pair with a fixed current $I$ at the cost of lower gain
Power-supply rejection ratio (PSRR)

- PSRR is defined as the ratio of the amplifier differential gain to the gain from the supply voltage
  \[
  PSRR^+ = \frac{A_d}{A^+} = \frac{v_o/v_{id}}{v_o/v_{dd}}
  \]
  \[
  PSRR^- = \frac{A_d}{A^-} = \frac{v_o/v_{id}}{v_o/v_{ss}}
  \]

Design trade-offs

- CMOS two-stage op amp performance is determined by
  - The channel length of the MOSFETs
  - The overdrive voltage of the MOSFETs

- Performance benefit for a larger channel length: gain, CMRR, PSRR
- Performance benefit for a smaller overdrive voltage: gain, CMRR, PSRR, ICMR, output swing and offset
- Performance benefit for a larger overdrive voltage: high-frequency characteristics (gain)

\[
f_T = \frac{1}{2\pi} \frac{g_m}{C_{gs} + C_{gd}} \approx \frac{1}{2\pi} \frac{1.5 \mu V_{OV}}{L^2}
\]

- For modern submicron CMOS technologies:
  - Typical $V_{OV}$ between 0.1 to 0.3 V
  - Channel length is at least 1.5 to 2 times minimum length ($L_{min}$)
10.2 The Folded-Cascode CMOS Op Amp

Circuit Configuration

- Cascode topology to increase the gain of the input differential pair
- Folded topology to improve the ICMR and to reduce the required supply voltage
- Is generally considered a single-stage amplifier
- Also called operational transconductance amplifier (OTA)

DC bias:
- Bias current for $Q_1$-$Q_2$ is $I/2$
- Bias current for $Q_5$-$Q_8$ is $I_B - I/2$
- $I_B$ can be realized by MOS current mirrors
Input common-mode range and output swing

- ICMR: \(-V_{SS} + V_{OV11} + V_{OV1} + V_m \leq V_{ICM} \leq V_{DD} - |V_{OV9}| + V_m\)
- Output swing: \(-V_{SS} + V_{OV5} + V_{OV7} + V_m \leq V_O \leq V_{DD} - |V_{OV10}| - |V_{OV4}|\)

**Voltage gain**

\[ G_m = g_{m1} = g_{m2} \]
\[ R_o = R_{o4} \parallel R_{o6} = [g_{m4}r_{o4}(r_{o2} \parallel r_{o10})](g_{m6}r_{o6}r_{o8}) \]
\[ A_v = G_mR_o \approx g_{m1}[g_{m4}r_{o4}(r_{o2} \parallel r_{o10})](g_{m6}r_{o6}r_{o8}) \]

- High voltage gain due to increased output resistance
- Not desirable for applications where low output resistance is needed for the op amp

**Frequency response**

- Dominant pole at the output node
- Excellent high-frequency response

\[ \frac{V_o}{V_{id}} = \frac{G_mR_o}{1+sc_LR_o} \quad \Rightarrow \quad f_c = \frac{1}{2\pi} \frac{G_m}{C_L} \]

**Slew rate**

- The slew rate is limited by the bias current \(I\) and the load \(C_L\)
- Slew rate \(SR = \frac{I}{C_L} = 2\pi f_c V_{OV1}\) for \(I_B > I\)
- Typically \(I_B\) is set 10% ~ 20% larger than \(I\)
**Increasing the ICMR: rail-to-rail input operation**

- NMOS and PMOS differential pairs in parallel
- ICMR exceeds the power supply voltage
- Differential output voltage provided
- ICM in the middle:
  - Both pairs operate simultaneously
  - \( A_v = 2G_mR_o \)
- ICM near supply voltage:
  - Only one of the pairs is operational
  - Gain drops to half

**Increasing the output voltage range: wide-swing current mirror**

- Modified cascode current mirror
- Output swing increased by \( V_t \)
- Output resistance remains the same
- A proper dc bias voltage \( V_{BIAS} \) is needed
8.3 The 741 Op-Amp Circuit

741 Op-Amp

- Device parameters:
  - npn: $I_S = 10^{-14}$ A, $\beta = 200$, $V_A = 125$ V
  - pnp: $I_S = 10^{-14}$ A, $\beta = 50$, $V_A = 50$ V
Bias circuit:
- Reference current generated by $Q_{11}$, $Q_{12}$ and $R_5$
- Bias for input stage: Widlar current source ($Q_{10}$, $Q_{11}$ and $R_4$) and current mirror $Q_8$, $Q_9$
- Bias for second stage: current mirror $Q_{12}$, $Q_{13B}$ ($Q_{13}$ is a two-output current source)
- Bias for output stage: current mirror $Q_{12}$, $Q_{13A}$/$Q_{18}$-$Q_{19}$ provides $2V_{BE}$ drop between $V_{B14}$ and $V_{B20}$

Input stage: ($Q_1$-$Q_7$, $R_1$-$R_3$)
- Input emitter follower ($Q_1$-$Q_2$): high input resistance
- Current-mirror load ($Q_5$-$Q_7$, $R_1$-$R_3$): high output resistance and differential to single-ended conversion
- Level shifting ($Q_3$ and $Q_4$): for required voltage swing and dc level at the input of the second stage

Second stage: ($Q_{16}$-$Q_{17}$, $Q_{13B}$, $R_8$-$R_9$)
- Emitter follower $Q_{16}$ for high input resistance
- Common-emitter $Q_{17}$ for voltage gain
- Miller compensation technique by $C_C$

Output stage: ($Q_{14}$, $Q_{20}$)
- Complementary pair $Q_{14}$ and $Q_{20}$
- Low output resistance
- Relatively large load current without dissipating a large amount of power
- Emitter follower $Q_{23}$ to increase input resistance of the output stage

Short-circuit protection circuitry $Q_{15}$, $Q_{21}$, $Q_{24}$, $Q_{22}$, $R_6$, $R_7$, $R_{11}$
10.4 DC Analysis of the 741

Reference bias current
- Provided by $Q_{11}$, $Q_{12}$ and $R_5$
  \[ I_{REF} = \frac{V_{CC} - V_{EB12} - V_{BE11} - (-V_{EE})}{R_5} \]
  \[ \Rightarrow I_{REF} = 0.73 \text{ mA (for } V_{CC} = V_{EE} = 15 \text{ V)} \]

Input-stage bias
- Widlar current source $Q_{11}$, $Q_{10}$ and $R_4$:
  \[ V_T \ln \left( \frac{I_{REF}}{I_{C10}} \right) = I_{C10} R_4 \]
  \[ \Rightarrow I_{C10} = 19 \text{ \(\mu\)A} \]
- Current mirror $Q_8$ and $Q_9$:
  \[ \frac{2I}{1 + 2/\beta_p} + \frac{2I}{\beta_p} = I_{C10} \]
  \[ \Rightarrow I_{C1} = I_{C2} \cong I_{C3} = I_{C4} = 9.5 \text{ \(\mu\)A} \]
  \[ \Rightarrow Q_1-Q_4 \text{ and } Q_8-Q_9 \text{ form a negative feedback loop} \]
  \[ \Rightarrow \text{Bias current can be stabilized by the negative feedback} \]
Current-source load $Q_5$-$Q_7$ and $R_1$-$R_3$

\[ I_{C7} \approx I_{E7} = \frac{2I}{\beta_N} + \frac{V_{BE6} + IR_2}{R_3} = \frac{2I}{\beta_N} \ln\left(\frac{I}{I_S}\right) + IR_2 \]

\[ \Rightarrow I_{C7} = 10.5 \, \mu A \]

Input bias current and offset currents

- **Input bias current:**
  \[ I_B = \frac{I_{B1} + I_{B2}}{2} = \frac{I}{\beta_N} \]
  \[ \Rightarrow I_B = 47.5 \, nA \]

- **Input offset current:**
  \[ I_{OS} = |I_{B1} - I_{B2}| \]
  \[ \Rightarrow \text{Non-zero input offset due to mismatches in the } \beta \text{ value} \]

Input common-mode range:

- Input common-mode voltage over which the input stage remains in the linear active mode
- The upper end limited by saturation of $Q_1$ and $Q_2$
- The lower end limited by saturation of $Q_3$ and $Q_4$
Second-stage bias

\[ I_{C17} \approx I_{C13B} \approx 0.75I_{\text{REF}} \]

\[ V_{BE17} = V_T \ln \left( \frac{I_{C17}}{I_S} \right) \]

\[ I_{C16} \approx I_{E16} = I_{B17} + \frac{I_{E17}R_8 + V_{BE17}}{R_9} \]

\[ \Rightarrow I_{C17} \approx I_{C13B} = 550 \mu A \]

\[ V_{EB17} = 618 \text{ mV and } I_{C16} = 16.2 \mu A \]

Output-stage bias

- DC for \( Q_{23} \):
  \[ I_{C23} \approx I_{E23} \approx 0.25I_{\text{REF}} \]
  \[ \Rightarrow I_{C23} \approx 180 \mu A \text{ (} I_{B23} \approx 3.6 \mu A \text{ negligible for } I_{C17} \) \]

- DC for \( Q_{18} - Q_{19} \):
  \[ I_{C18} \approx 0.25I_{\text{REF}} - V_{BE18}/R_{10} \]
  \[ V_{BE18} = V_T \ln \left( \frac{I_{C18}}{I_S} \right) \]
  \[ \Rightarrow I_{C18} \approx 165 \mu A \text{ and } I_{C19} \approx V_{BE18}/R_{10} + I_{B18} = 15.8 \mu A \]

- DC for \( Q_{14} \) and \( Q_{20} \):
  \[ V_{BB} = V_{BE18} + V_{BE19} = 588 \text{ mV} + 530 \text{ mV} = 1.118 \text{ V} \]
  \[ I_{C14} = I_{C20} = 154 \mu A \text{ (for } I_{S14} = I_{S20} = 3 \times 10^{-14} \text{ A} \)
10.5 Small-Signal Analysis of the 741

The input stage

- **Differential input resistance:**
  \[ i_e = v_i / (4r_e) \]
  \[ R_id = 4(\beta_\infty + 1)r_e \]
  \[ \Rightarrow r_e = 2.63 \, k\Omega \text{ and } R_id = 2.1 \, M\Omega \]

- **Transconductance:**
  \[ G_m1 \equiv \frac{i_e}{v_i} \approx \frac{2a_i e}{v_i} = \frac{\alpha}{2r_e} = \frac{1}{2} g_m1 \]
  \[ \Rightarrow G_m1 = 0.19 \, mA/V \]

- **Output resistance:**
  \[ R_o = r_o[1 + g_m(R_e || r_\pi)] \]
  \[ \Rightarrow R_{o4} = r_o4[1 + g_{m4}(r_e4||r_\pi)] = 10.5 \, M\Omega \]
  \[ \Rightarrow R_{o6} = r_o6[1 + g_{m6}(R_2||r_\pi6)] = 18.2 \, M\Omega \]
  \[ \Rightarrow R_{o1} = R_{o4}||R_{o6} = 6.7 \, M\Omega \]

- **Equivalent circuit for the input stage:**

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**Diagram:**

- Circuit diagram showing the input stage with components labeled as follows:
  - Input voltage \( v_i \)
  - Resistance \( R_id \)
  - Transconductance \( G_m1 \)
  - Output resistances \( R_o4 \) and \( R_o6 \)
  - Collector capacitance \( C_6 \)
  - Additional components and connections as per the diagram.
The second stage

- Input resistance
  \[ R_{i2} = (\beta_{16} + 1) \left\{ r_{e16} + [R_9 \parallel (\beta_{17} + 1)(r_{e17} + R_8)] \right\} \]
  \[ \Rightarrow R_{i2} \approx 4 \text{ M}\Omega \]

- Transconductance
  \[ G_{m2} = \frac{i_{e17}}{v_{i2}} = \frac{\alpha \cdot R_9 \parallel R_{i17}}{r_{e17} + R_8 \parallel R_{i17}} \]
  \[ \Rightarrow G_{m2} = 6.5 \text{ mA/V} \]

- Output resistance
  \[ R_{o2} = R_{o13B} \parallel R_{o17} \approx r_{o17} [1 + g_{m17}(r_{\pi17} \parallel R_8)] \]
  \[ \Rightarrow R_{o2} = 81 \text{ k}\Omega \]

- Equivalent circuit for the second stage:
The output stage

- Output voltage limits
  \[ v_{O\text{max}} = V_{CC} - |V_{CES}| - V_{BE14} \]
  \[ v_{O\text{min}} = -V_{EE} + V_{CES} + V_{EB23} + V_{EB20} \]
  ➜ approximately 1 V below \( V_{CC} \) and 1.5 V above \( -V_{EE} \)

- Input resistance (for \( R_L = 2 \) k\( \Omega \), \( I_{C20} = 5 \) mA and \( I_{C14} = 0 \))
  \[ R_{120} = r_{\pi20} + (1 + \beta_{20})R_L \approx \beta_{20}R_L \]
  \[ R_{in3} \approx r_{\pi23} + (1 + \beta_{23})(R_{120} || r_{o13,4}) \approx \beta_{23}(R_{120} || r_{o13,4}) \]
  ➜ \( R_{in3} \approx 3.7 \) M\( \Omega \)

- Open-circuit voltage gain
  \[ G_{vo3} = \frac{V_o}{V_o} \bigg|_{R_L=\infty} \approx 1 \]

- Transconductance
  \[ v_{13} = v_{b23} \approx v_{e23} = v_{b20} \]
  \[ G_{m3} \equiv \frac{i_o}{v_{13}} \bigg|_{R_L=0} \approx \frac{1}{r_{e20}} \approx g_{m20} \]
Output resistance

\[ R_{o23} = r_{e23} + \frac{R_{o2}}{\beta_{23} + 1} \]

\[ R_{out} = r_{e20} + \frac{R_{o23} \parallel r_{o13,4}}{\beta_{20} + 1} \approx r_{e20} + \frac{R_{o23}}{\beta_{20} + 1} \]

\[ \Rightarrow R_{out} \approx 34 \, \Omega \]

Equivalent circuit for the output stage

Output short-circuit protection

- One of the two output transistors could conduct a large amount of current if output is short-circuited.
- Short-circuit protection is adopted in the 741 op amp.
- For current source case (\( I_{C14} > 20 \, mA \))
  \[ \Rightarrow V_{BE15} > 540 \, mA \]
  \[ \Rightarrow Q_{15} \text{ turns on and takes away the base current of } Q_{14} \]
  \[ \Rightarrow I_{C14} \text{ is limited as the base current is reduced} \]
- Similar case for current sink case (\( I_{C20} > 20 \, mA \))
10.6 Gain, Frequency Response and Slew Rate of the 741

**Small-signal gain**

\[ A_v = \frac{v_o}{v_i} = \frac{\frac{v_{o2}}{v_{i2}}}{\frac{v_{o1}}{v_{i1}}} = -G_m (R_{o1} \parallel R_{o2})(-G_m R_{o2})G_{v0} \frac{R_f}{R_L + R_{out}} \]

\[ A_v = 243147 \text{ V/V} = 107.7 \text{ dB} \]

**Frequency response**

\[ C_{in} = C_C (1 + |A_v|) \]
\[ R_e = R_{o1} \parallel R_{o2} \]
\[ f_P = \frac{1}{2\pi C_{in} R_e} \]
\[ f_t = A_v f_P \]

\[ f_P = 4.1 \text{ Hz} \]
\[ f_t = 1 \text{ MHz} \]

**Slew rate**

\[ SR = \frac{2I}{C_C} \]

\[ SR = 0.63 \text{ V/\mu s} \]

- Relationship between \( f_t \) and slew rate

\[ SR = 4V_T \omega_t \]

\[ \Rightarrow \text{Slew rate of MOS opamp with same } f_t \text{ is 2~3 times higher than the 741} \]

\[ \Rightarrow G_m \text{-reduction method: total bias current is kept constant with reduced } G_{m1} \]