CHAPTER 7 DIFFERENTIAL AND MULTISTAGE AMPLIFIERS

Chapter Outline
7.1 The CMOS Differential Pair
7.2 Small-Signal Operations of the MOS Differential Pair
7.3 The BJT Differential Pair
7.4 Other Nonideal Characteristics of the Differential Amplifier
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7.1 The MOS Differential Pair

The differential pair (differential amplifier) configuration

- Widely used building block in analog integrated circuit design
  - Performance depends critically on the matching of the devices
  - Utilizes more components than single-ended circuits
  - Well suited for IC fabrication

- Advantages of using differential pair
  - Less sensitive to noise and interference than single-ended circuits
  - Bias is provided without the need for bypass and coupling capacitors

The CMOS differential pair

- The design philosophy for ICs is different from that of discrete-component circuits
  - Two matched transistors are used
  - The source terminals are connected together
  - Identical device parameters
    - \( k_n, V_T \), and even layout) for \( Q_1 \) and \( Q_2 \)
  - Biased by a constant-current source
  - Resistive loads are used for simplicity
  - Differential input at the gates
  - Differential output at the drains
Operation with a common-mode input voltage

- Circuit analysis
  - Both input terminals are connected to a common-mode voltage $V_{CM}$
  - The current divides equally due to device matching

\[
\frac{I}{2} = \frac{1}{2} k_n \frac{W}{L} (V_{GS} - V_t)^2
\]

\[
V_S = V_{CM} - V_{GS} = V_{CM} - \left( \frac{I}{\sqrt{k_n'(W/L)}} - V_t \right)
\]

\[
V_{OV} = \frac{I}{\sqrt{k_n'(W/L)}}
\]

\[
v_{d1} = v_{d2} = V_{DD} - \frac{I}{2} R_D
\]

- The differential pair does not respond to common-mode input signals

- Input common-mode range:
  - The range of $V_{CM}$ for proper operation
  - Both $Q_1$ and $Q_2$ should be in saturation

\[
V_{CM_{max}} = V_{DD} - \frac{I}{2} R_D + V_t
\]

\[
V_{CM_{min}} = -V_{SS} + V_{CS} + V_{GS} = -V_{SS} + V_{CS} + V_{OV} + V_t
\]
Operation with a differential input voltage

- A difference voltage $v_{id}$ exists between the input terminals
- The current of $Q_1$ is different from that of $Q_2$ due to differential input voltage
- The overall current $I$ remains unchanged
- The value of $v_{id}$ at which the entire bias current $I$ is steered into $Q_1$ is

$$v_{GS1} = V_i + \frac{2I}{k'(W/L)} = V_i + \sqrt{2V_{OV}}$$

$$v_{id\text{max}} = V_i + \sqrt{2V_{OV}} - V_i = \sqrt{2V_{OV}}$$

- The current $I$ can be steered from one transistor to the other by varying $v_{id}$ in the range

$$-\sqrt{2V_{OV}} \leq v_{id} \leq \sqrt{2V_{OV}}$$

$\Rightarrow$ The range of differential-mode operation

- Differential pair as a linear amplifier
  - Keep the differential input voltage $v_{id}$ small
  - The currents of the transistor pair become $I/2 \pm \Delta I$
  - A differential output voltage is taken between the two drains as $2\Delta I R_D$
Large-signal operation

\[ v_{id} = v_{GS1} - v_{GS2} = \frac{2i_{D1}}{k_n'(W/L)} - \frac{2i_{D2}}{k_n'(W/L)} \]

\[ I = i_{D1} + i_{D2} \]

- Drain currents of the differential pair

\[ i_{D1} = \frac{I}{2} + \left( \frac{I}{V_{OV}} \right) \left( \frac{v_{id}}{2} \right) \sqrt{1 - \left( \frac{v_{id}}{2V_{OV}} \right)^2} \]

\[ i_{D2} = \frac{I}{2} - \left( \frac{I}{V_{OV}} \right) \left( \frac{v_{id}}{2} \right) \sqrt{1 - \left( \frac{v_{id}}{2V_{OV}} \right)^2} \]

- Normalized transfer characteristics
  - Nonlinear transfer characteristics
  - The overdrive voltage \( V_{OV} \) is calculated as
    \[ i_{D1} = i_{D2} = I/2 \]

- Small-signal approximation
  - Linear I-V characteristics for small \( v_{id} \)

\[ i_{D1} \approx \frac{I}{2} + \left( \frac{I}{V_{OV}} \right) \left( \frac{v_{id}}{2} \right) \]

\[ i_{D2} \approx \frac{I}{2} - \left( \frac{I}{V_{OV}} \right) \left( \frac{v_{id}}{2} \right) \]
Linearity of the differential pair

- The linearity of the differential pair can be increased by increasing the overdrive voltage $V_{OV}$
- Linearity-transconductance trade-off:
  - Smaller aspect ratio ($W/L$) of $Q_1$ and $Q_2$ at fixed bias current $I$
  - Resulting in smaller transconductance and gain

- Linearity-power trade-off:
  - Larger bias current $I$ with fixed aspect ratio
  - Resulting in larger transconductance and gain at the cost of higher power dissipation
7.2 Small-Signal Operation of the MOS Differential Pair

**Differential gain**
- The differential input signal \( v_{id} \) is applied in a **complementary** (or balanced) manner.
- **Single-ended outputs** \( v_{o1} \) and \( v_{o2} \): output taken between one of the drains and ground.
- **Differential output** \( v_{od} \): output taken between the two drains.

**Small-signal circuit analysis:**

\[
g_m = \sqrt{k'_{n}(W/L)}I = \frac{I}{v_{ov}}
\]

\[
v_{o1} = -g_m R_D \frac{v_{id}}{2}
\]

\[
v_{o2} = g_m R_D \frac{v_{id}}{2}
\]

- **Single-ended gain:**

\[
\frac{v_{o1}}{v_{id}} = -\frac{1}{2} g_m R_D
\]

\[
\frac{v_{o2}}{v_{id}} = \frac{1}{2} g_m R_D
\]

- **Differential gain:**

\[
A_d \equiv \frac{v_{od}}{v_{id}} = \frac{v_{o2} - v_{o1}}{v_{id}} = g_m R_D
\]
The differential half-circuit

Virtual ground:
- Differential operation for a symmetrical circuit
- The voltage at the joint source connection must be zero
- A signal ground is established at the source terminals without a large bypass capacitor
- Performance of a symmetrical differential circuit can be evaluated by considering only half the circuit

\[ A_d = \frac{v_{od}}{v_{id}} = g_m (R_D \parallel r_o) \]
The differential amplifier with current-source load

\[ A_d = \frac{v_{os}}{v_{id}} = g_m \left( r_{o1} \parallel r_{o3} \right) \]

\[ A_d = \frac{v_{os}}{v_{id}} = g_m \left( R_{on} \parallel R_{op} \right) = g_m \left( g_{m3} r_{o3} r_{o1} \parallel g_{m5} r_{o3} r_{o7} \right) \]
Common-mode gain of a differential pair

- A differential pair with ideal current source
  - The output resistance ($R_{SS}$) is infinite
  - Drain currents of $Q_1$ and $Q_2$ do not change with $V_{CM}$
  - The single-ended outputs remain unchanged
  - The differential output voltage and common-mode gain are zero

- A differential pair with a practical current source
  - The output resistance ($R_{SS}$) is finite
  - Drain currents of $Q_1$ and $Q_2$ change simultaneously with $V_{CM}$
  - The single-ended outputs vary with $V_{CM}$
  - The differential output voltage and common-mode gain are zero

- The differential pair rejects common-mode signals regardless the value of $R_{SS}$

\[
v_{icm} = i \left( \frac{1}{g_m} + 2R_{SS} \right) \Rightarrow i = \frac{v_{icm}}{1/g_m + 2R_{SS}}
\]

\[
v_{o1} = v_{o2} = -\frac{R_D}{1/g_m + 2R_{SS}}v_{icm} \approx -\frac{R_D}{2R_{SS}}v_{icm}
\]

\[
v_{od} = v_{o2} - v_{o1} = 0
\]
Common-mode half-circuit

- Circuit analysis technique for symmetrical circuit with common-mode operation
- The symmetrical points are equal potential
- No current flowing across the symmetrical line
- The performance can be evaluated by common-mode half-circuit

\[
v_{o1} = v_{o2} = \frac{R_D}{\frac{1}{g_m} + 2R_{SS}} v_{icm}
\]
Effect of resistance mismatch

- **Common-mode gain:**
  
  $$v_{ol} = -\frac{R_D}{1/g_m + 2R_{SS}} v_{icm} \approx -\frac{R_D}{2R_{SS}} v_{icm}$$
  
  $$v_{o2} = -\frac{R_D + \Delta R_D}{1/g_m + 2R_{SS}} v_{icm} \approx -\frac{R_D + \Delta R_D}{2R_{SS}} v_{icm}$$
  
  $$A_{cm} \equiv \frac{v_{o2}}{v_{icm}} v_{o1} = \frac{R_D}{2R_{SS}} \left( \frac{\Delta R_D}{R_D} \right)$$

- Mismatch in $R_D$ causes a finite common-mode gain

- **Common-mode rejection ratio (CMRR):**
  
  - CMRR is defined as the ratio of differential-mode gain and the common-mode gain
  - A measure of the effectiveness of the differential pair in rejecting common-mode interference
  - Is usually expressed in decibels
    
    $$CMRR \equiv \left| \frac{A_d}{A_{cm}} \right|$$
    
    $$CMRR(dB) = 20 \log \left| \frac{A_d}{A_{cm}} \right|$$

- **CMRR** of the differential amplifier with respect to the resistance mismatch
  
  $$CMRR = \frac{2g_m R_{SS}}{\Delta R_D / R_D}$$

  - Utilizes a bias current source with a high output resistance
  - High degree of matching between the drain resistance
Effect of transconductance mismatch

- Mismatch exists between $Q_1$ and $Q_2$
  
  \[ g_{m1} = g_m + \Delta g_m / 2 \]
  
  \[ g_{m2} = g_m - \Delta g_m / 2 \]
  
  \[ \Delta g_m = g_{m1} - g_{m2} \]

- Common-mode gain:
  
  \[ i_1 = \frac{g_{m1}v_{lcm}}{1 + (g_{m1} + g_{m2})R_S} \]
  
  \[ i_2 = \frac{g_{m2}v_{lcm}}{1 + (g_{m1} + g_{m2})R_S} \]
  
  \[ v_{o1} = -i_1R_D = -\frac{g_{m1}R_D}{1 + (g_{m1} + g_{m2})R_S}v_{lcm} \]
  
  \[ v_{o2} = -i_2R_D = -\frac{g_{m2}R_D}{1 + (g_{m1} + g_{m2})R_S}v_{lcm} \]
  
  \[ v_{od} = v_{o2} - v_{o1} = \frac{\Delta g_m R_D}{1 + 2g_mR_S}v_{lcm} \]
  
  \[ A_{cm} = \frac{v_{od}}{v_{lcm}} = \frac{\Delta g_m R_D}{1 + 2g_mR_S} \approx \left( \frac{R_D}{2R_S} \right) \left( \frac{\Delta g_m}{g_m} \right) \]

- CMRR:
  
  \[ CMRR = \frac{2g_mR_S}{\Delta g_m / g_m} \]
7.3 The BJT Differential Pair

**Circuit configuration**
- Two identical BJT transistors $Q_1$ and $Q_2$ with emitters jointed together
- Biased with a current source

**Input common-mode range**
- Allowable range of $V_{CM}$ for $Q_1$ and $Q_2$ in active
  \[ V_{CM_{\text{max}}} \approx V_c + 0.4 = V_{cc} - \alpha R_c \left( \frac{I}{2} \right) + 0.4 \]
  \[ V_{CM_{\text{min}}} = -V_{EE} + V_{cs} + V_{BE} \]

**Common-mode operation**
- Common-mode input voltage $V_{CM}$ for $v_{B1}$ and $v_{B2}$
- Single-ended output voltage:
  \[ V_{c1} = V_{cc} - \alpha R_c \left( \frac{I}{2} \right) \]
  \[ V_{c2} = V_{cc} - \alpha R_c \left( \frac{I}{2} \right) \]
- Differential output voltage:
  \[ V_{od} = V_{c2} - V_{c1} = 0 \]
- Finite output resistance of the current source
  - Single-ended output change with $V_{CM}$
  - Differential output is still zero
**Large-signal operation**

- **Transfer characteristics**
  \[
  \frac{i_{E1}}{i_{E2}} = \frac{I_s e^{(v_{g1}−v_{g2})/V_T}}{I_s e^{(v_{g1}−v_{g2})/V_T}} = e^{(v_{g1}−v_{g2})/V_T}
  \]
  \[
  i_{E1} = \frac{I}{1+\exp(-v_{id}/V_T)}
  \]
  \[
  i_{E2} = \frac{I}{1+\exp(v_{id}/V_T)}
  \]
  \[
  i_{E1} + i_{E2} = I
  \]

- **Normalized characteristics**
  - The bias current is divided equally for \(v_{id} = 0\)
  - Unequal current through \(Q_1\) and \(Q_2\) for \(v_{id} \neq 0\)
  - A relatively small \(v_{id}\) for complete current switching
  - The linearity can be improved by emitter degeneration \(R_e\)
  - Transconductance and gain decrease due to emitter degeneration

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Small-signal operation

- Small-signal current
  - Differential pair: \( i_c = \frac{g_m v_{id}}{2} \)
  - Differential pair with emitter degeneration: \( i_c = \frac{\alpha v_{id}}{2} \left( \frac{2 r_e + 2 R_e}{(\beta + 1) r_e} \right) \approx \frac{g_m v_{id}}{2} \left( 1 + g_m R_e \right) \)

- Input differential resistance
  - Differential pair: \( R_{id} = \frac{v_{id}}{i_b} = 2 r_\pi \)
  - Differential pair with emitter degeneration: \( R_{id} = (\beta + 1) (2 r_e + 2 R_e) \approx 2 [R_e + r_\pi (1 + g_m R_e)] \)
Differential voltage gain

- Differential pair: \( A_d = \frac{v_{od}}{v_{id}} = g_m R_C \)
- Differential pair with emitter degeneration: \( A_d = \frac{\alpha}{1 + g_m R_e} \)
- The differential amplifier can also be fed in a single-ended fashion

Equivalent circuit model
Common-mode gain and CMRR

- Differential pair with device matching:

\[ v_{o1} = v_{o2} = -\frac{\alpha R_C}{r_e + 2R_{EE}} v_{icm} \]

\[ v_{od} = v_{o2} - v_{o1} = 0 \]

- Differential pair with resistance mismatch:

\[ v_{o1} = -\frac{\alpha R_C}{r_e + 2R_{EE}} v_{icm} \]

\[ v_{o2} = -\frac{\alpha (R_C + \Delta R_C)}{r_e + 2R_{EE}} v_{icm} \]

\[ v_{od} = v_{o2} - v_{o1} = -\frac{\alpha \Delta R_C}{r_e + 2R_{EE}} v_{icm} \]

\[ A_{cm} = \frac{v_{od}}{v_{icm}} = -\frac{\alpha \Delta R_C}{r_e + 2R_{EE}} \approx -\frac{R_C}{2R_{EE}} \frac{\Delta R_C}{R_C} \]

\[ CMRR = \frac{2g_m R_{EE}}{\Delta R_C / R_C} \]

- High output resistance is desirable
- The resistance mismatch should be minimized

- Common-mode input resistance

\[ R_{icm} \approx R_{EE} \beta \frac{1 + R_C / (r_e \beta)}{1 + (R_C + 2R_{EE}) / r_o} \]
7.4 Other Nonideal Characteristics of the Differential Amplifier

**Input offset voltage of the MOS differential pair**

- **Output dc offset voltage**: the finite output voltage with both input grounded
- **Input offset voltage** ($V_{OS}$): the input referred offset voltage as the output offset divided by gain
  - Output voltage becomes zero if $-V_{OS}$ is applied between the inputs
  - Its polarity can not be predetermined
- Factors contribute to the dc offset voltage:
  - Mismatch in load resistance
  - Mismatch in aspect ratio ($W/L$)
  - Mismatch in threshold voltage $V_t$
Input offset voltage due to load resistance mismatch

\[ R_{d1} = R_D + \frac{\Delta R_D}{2} \]
\[ R_{d2} = R_D - \frac{\Delta R_D}{2} \]

\[ V_{os} = \frac{V_o}{g_m R_D} = \frac{I}{2} \frac{\Delta R_D}{g_m R_D} = \frac{V_{ov}}{2} \frac{\Delta R_D}{R_D} \]

Input offset voltage due to aspect ratio mismatch

\[ \left( \frac{W}{L} \right)_1 = \left( \frac{W}{L} \right) + \frac{1}{2} \Delta \left( \frac{W}{L} \right) \]
\[ I_1 = \frac{I}{2} \left[ 1 + \frac{\Delta (W/L)}{2(W/L)} \right] \]

\[ \left( \frac{W}{L} \right)_2 = \left( \frac{W}{L} \right) - \frac{1}{2} \Delta \left( \frac{W}{L} \right) \]
\[ I_2 = \frac{I}{2} \left[ 1 - \frac{\Delta (W/L)}{2(W/L)} \right] \]

\[ V_{os} = \frac{R_D (I_2 - I_1)}{g_m R_D} = \frac{V_{ov}}{2} \frac{\Delta (W/L)}{(W/L)} \]

Input offset voltage due to threshold voltage mismatch

\[ V_{t1} = V_t + \frac{\Delta V_t}{2} \]
\[ I_1 = \frac{1}{2} k_n \left( \frac{W}{L} \right) (V_{os} - V_t)^2 \left[ 1 - \frac{\Delta V_t}{2(V_{os} - V_t)} \right]^2 \approx \frac{I}{2} \left( 1 - \frac{\Delta V_t}{V_{os} - V_t} \right) \]

\[ V_{t2} = V_t - \frac{\Delta V_t}{2} \]
\[ I_2 = \frac{1}{2} k_n \left( \frac{W}{L} \right) (V_{os} - V_t)^2 \left[ 1 + \frac{\Delta V_t}{2(V_{os} - V_t)} \right]^2 \approx \frac{I}{2} \left( 1 + \frac{\Delta V_t}{V_{os} - V_t} \right) \]

\[ V_{os} = \frac{(I_2 - I_1) R_D}{g_m R_D} = \Delta V_t \]

Input offset voltage:

- The three mismatch factors are uncorrelated

\[ V_{os} = \sqrt{\left( \frac{V_{ov}}{2} \frac{\Delta R_D}{R_D} \right)^2 + \left( \frac{V_{ov}}{2} \frac{\Delta (W/L)}{(W/L)} \right)^2 + (\Delta V_t)^2} \]

- To minimize the input offset voltage
  - Decrease overdrive voltage \( V_{ov} \)
  - Minimize the device mismatch ratio
**Input offset voltage of the bipolar differential pair**

- Factors contribute to offset voltage
  - Mismatch in load resistance
  - Mismatch in junction area
  - Mismatch in $\beta$

- Input offset voltage due to load resistance mismatch
  \[
  R_{c1} = R_c + \Delta R_c / 2 \\
  R_{c2} = R_c - \Delta R_c / 2 \\
  \Rightarrow \quad V_{os} = \left( \alpha \frac{I}{2} \frac{\Delta R_c}{R_c} \right) / g_m R_c = V_T \left( \frac{\Delta R_c}{R_c} \right)
  \]

- Input offset voltage due to emitter area mismatch
  \[
  I_{s1} = I_s + \frac{\Delta I_s}{2} \\
  I_{s2} = I_s - \frac{\Delta I_s}{2} \\
  I_{e1} = \frac{I}{2} \left( 1 + \frac{\Delta I_s}{2 I_s} \right) \\
  I_{e2} = \frac{I}{2} \left( 1 - \frac{\Delta I_s}{2 I_s} \right) \\
  \Rightarrow \quad V_{os} = \alpha \left( \frac{I}{2} \frac{\Delta I_s}{I_s} \right) R_c / (g_m R_c) = V_T \left( \frac{\Delta I_s}{I_s} \right)
  \]

- Input offset voltage:
  - The factors are uncorrelated
  - The offset voltage can be minimized by reducing the device mismatch ratios
  - The input offset voltage for BJT (proportional to $V_T$) is typically smaller than its MOS counterpart (proportional to $V_{OV}$)
Input bias current and offset currents of the bipolar differential pair

- **Input bias current:**
  - Finite bias currents are required at the input terminals of BJT differential pair
  - The input bias currents are simply the base current of the BJT transistors
    \[
    I_{B1} = I_{B2} = \frac{I}{2(\beta+1)}
    \]

- **Input offset current:**
  - Offset in the input bias currents due to device mismatch
  - Mostly from the mismatch in \( \beta \)
    \[
    \beta_1 = \beta + \frac{1}{2} \Delta \beta \\
    I_{B1} = \left( \frac{1}{2} \right) \left( \frac{1}{\beta + 1 + \Delta \beta / 2} \right) \approx \left( \frac{1}{2} \right) \left( \frac{1}{\beta + 1} \right) \left( 1 - \frac{\Delta \beta}{2 \beta} \right)
    \]
    \[
    \beta_2 = \beta - \frac{1}{2} \Delta \beta \\
    I_{B2} = \left( \frac{1}{2} \right) \left( \frac{1}{\beta + 1 - \Delta \beta / 2} \right) \approx \left( \frac{1}{2} \right) \left( \frac{1}{\beta + 1} \right) \left( 1 + \frac{\Delta \beta}{2 \beta} \right)
    \]
    \[
    I_{OS} = \frac{I}{2(\beta+1)} \frac{\Delta \beta}{\beta} = I_B \left( \frac{\Delta \beta}{\beta} \right)
    \]

Comparison for MOS and bipolar differential pair

- Bipolar differential pair typically has smaller input offset voltage
- Bipolar differential pair suffers from input offset current
7.5 The Differential Amplifier with Active Load

Differential to single-ended conversion

- Differential pair with differential output
  - Improved CMRR: suppress the influence of the common-mode interference
  - Higher voltage gain: gain is increased by a factor or 2
- Differential pair with single-ended output
  - Certain applications require single-ended output
  - A resistive load differential pair can simply provide the differential to single-ended conversion

- The active-loaded MOS differential pair
  - Utilizes a current mirror ($Q_3$ and $Q_4$) as the active load
  - Provides single-ended output for the differential pair
Basic circuit operation

- Quiescent point:
  - Perfect matching case:
    - Bias current is equally divided for $Q_1$ and $Q_2$
    - The current of $Q_1$ also flows through $Q_3$
    - Current of $Q_3$ is mirrored to $Q_4$
    - All currents are identical ($I_{D1} = I_{D2} = I_{D3} = I_{D4} = I/2$)
    - The currents of $Q_2$ and $Q_4$ balance out
    - Zero output current to the following stage
    - Quiescent output voltage $= V_{DD} - V_{SG3}$
  - Mismatch in the devices:
    - Nonzero net current at the output node
    - The current flows into the output resistances of $Q_2$ and $Q_4$
    - The output voltage deviates from $V_{DD} - V_{SG3}$

- Applying differential input voltage:
  - A difference current between $Q_1$ and $Q_2$
  - The net difference current exists at the output
Voltage gain of the active-loaded MOS differential pair

- Transconductance $G_m$:
  \[ v_{g3} = -g_{m1} \left( \frac{v_{id}}{2} \right) \left( \frac{1}{g_{m3}} \parallel r_{o3} \parallel r_{o3} \right) \approx -g_{m1} \left( \frac{v_{id}}{2} \right) \]
  \[ i_o = -g_{m3} v_{g3} + g_{m2} \left( \frac{v_{id}}{2} \right) = g_{m1} \left( \frac{g_{m1}}{g_{m3}} \right) \left( \frac{v_{id}}{2} \right) + g_{m2} \left( \frac{v_{id}}{2} \right) \approx g_{m1} v_{id} \]
  \[ G_m \approx g_{m1} = g_{m2} \]

- Output resistance $R_o$:
  \[ R_{in1} = r_{o1} + r_L = \frac{1}{g_{m1}} + \frac{1}{g_{m2}} \approx \frac{1}{g_{m1}} \]
  \[ R_{o2} = R_{in1} + r_{o2} + g_{m2} r_{o2} \approx \frac{1}{g_{m1}} + r_{o2} + \frac{g_{m2}}{g_{m1}} r_{o2} \approx 2r_{o2} \]
  \[ i = \frac{v_x}{R_{o2}} \]
  \[ i_o = i + i + \frac{v_x}{r_{o4}} = 2 \frac{v_x}{R_{o2}} + \frac{v_x}{r_{o4}} \]
  \[ R_o = r_{o2} \parallel r_{o4} \]

- Differential gain
  \[ A_d \equiv \frac{v_o}{v_{id}} = G_m R_o = g_{m1} (r_{o2} \parallel r_{o4}) \approx \frac{1}{2} g_{m1} r_o = \frac{A_0}{2} \]
Common-mode gain and CMRR

- The active-loaded CMOS differential pair has a high CMRR even with a single-ended output.
- Common-mode half-circuit is not applicable as the circuit is not symmetrical.
- $Q_1$ and $Q_2$ can be treated as two separated CS transistor with source degeneration.

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Common-mode gain:

\[ v_s = \frac{2R_{SS} \| r_{o1}}{2R_{SS} \| r_{o1} + 1/g_m} v_{icm} \approx v_{icm} \]

\[ i_o = \frac{v_{icm}}{2R_{SS}} \]

\[ G_{mcem} = \frac{i_o}{v_{icm}} = \frac{1}{2R_{SS}} \]

\[ R_{o1} = 2R_{SS} + r_{o1} + g_m r_{o1}(2R_{SS}) \]

\[ R_{o2} = 2R_{SS} + r_{o2} + g_m r_{o2}(2R_{SS}) \]

\[ v_{g3} = -G_{mcem} v_{icm} \left( R_{o1} \| r_{o3} \| \frac{1}{g_{m3}} \right) \]

\[ i_4 = g_m v_{g3} = g_m v_{g3} = -g_m G_{mcem} v_{icm} \left( R_{o1} \| r_{o3} \| \frac{1}{g_{m3}} \right) \]

\[ v_o = -v_{icm} \frac{r_{o4}}{2R_{SS}} \left[ 1 - g_m \left( R_{o1} \| r_{o3} \| \frac{1}{g_{m3}} \right) \right] \]

\[ A_{cm} = \frac{v_o}{v_{icm}} \approx \frac{r_{o4}}{2R_{SS} \left[ 1 + g_m r_{o3} \right]} \approx -\frac{1}{2g_m R_{SS}} \]

CMRR

\[ CMRR = \frac{|A_{d}|}{|A_{cm}|} = \left| g_m (r_{o2} \| r_{o1}) \right| \cdot (2g_m R_{SS}) \]
The bipolar differential pair with active load

- Circuit schematic:
  - Bipolar differential pair $Q_1$ and $Q_2$
  - Bipolar current mirror $Q_3$ and $Q_4$ as active load
  - Constant current source for dc bias
  - The bias current is equally divided for $Q_1$ and $Q_2$

- Input resistance ($R_i$):
  - Differential input resistance is defined at input $R_i = 2r_\pi$

- Transconductance ($G_m$):
  \[
  v_{b3} = -g_{m1}\left(\frac{v_{id}}{2}\right)(r_{e3} \parallel r_{o3} \parallel r_{o4} \parallel r_{\pi4}) 
  \approx -g_{m1}r_{e3}\left(\frac{v_{id}}{2}\right)
  \]
  \[
  g_{m4}v_{b4} = -g_{m4}g_{m1}r_{e3}\left(\frac{v_{id}}{2}\right)
  \]
  \[
  i_o = g_{m2}\left(\frac{v_{id}}{2}\right) - g_{m4}v_{b4} = (g_{m2} + g_{m4}g_{m1}r_{e3})\left(\frac{v_{id}}{2}\right)
  \]
  \[
  G_m \equiv \frac{i_o}{v_{id}} = \frac{g_{m2} + g_{m4}g_{m1}r_{e3}}{2} \approx g_m
  \]
- Output resistance ($R_o$):

$$R_{o2} \approx r_{o2} \left[ 1 + g_{m2} (r_{el} \parallel r_{\pi2}) \right] \approx r_{o2} (1 + g_{m2} r_{el}) \approx 2r_{o2}$$

$$i = \frac{v_x}{R_{o2}} = \frac{v_x}{2r_{o2}}$$

$$i_x = 2i + \frac{v_x}{r_{o4}} = \frac{v_x}{r_{o2}} + \frac{v_x}{r_{o4}}$$

$$R_o \equiv \frac{v_x}{i_x} = r_{o2} \parallel r_{o4}$$

- Differential gain:

$$A_d \equiv \frac{v_o}{v_{in}} = G_m R_o = g_m (r_{o2} \parallel r_{o4}) \approx \frac{1}{2} g_m r_o$$

- Common-mode gain:

$$i_1 \approx i_2 \approx \frac{v_{cm}}{2R_{EE}}$$

$$v_{b3} = -i \left( \frac{1}{g_{m3}} \parallel r_{\pi3} \parallel r_{o3} \parallel r_{\pi4} \right)$$

$$v_o = -r_{o4} (g_{m4} v_{b3} + i_2)$$

$$A_{cm} \equiv \frac{v_o}{v_{cm}} = \frac{r_{o4}}{2R_{EE}} g_{m4} \left( \frac{1}{g_{m3}} \parallel r_{\pi3} \parallel r_{o3} \parallel r_{\pi4} \right) - 1 \approx -\frac{r_{o4}}{2R_{EE}} g_{m3} + \frac{2}{r_{\pi3}} \approx -\frac{r_{o4}}{\beta_3 R_{EE}}$$

- CMRR:

$$CMRR = \frac{|A_d|}{|A_{cm}|} = g_m (r_{o2} \parallel r_{o4}) \left( \frac{\beta_3 R_{EE}}{r_{o4}} \right) \approx \frac{1}{2} \beta_3 g_m R_{EE}$$
- Systematic input offset voltage
  - Difference current between $Q_3$ and $Q_4$ due to finite $\beta$
  - Net current at output for both input terminals grounded
  - Input offset voltage to eliminate the output current
  - This offset has nothing to do with device mismatch

\[
\frac{I_4}{I_3} = \frac{1}{1 + 2/\beta_p}
\]

\[
I_4 = \alpha \frac{I/2}{1 + 2/\beta_p}
\]

\[
\Delta i = \alpha \frac{I}{2} - \alpha \frac{I/2}{1 + 2/\beta_p} = \alpha \frac{I}{2} + \frac{1}{2 + 2/\beta_p} \approx \alpha \frac{I}{\beta_p}
\]

\[
V_{OS} = -\frac{\Delta i}{G_m} = -\frac{2V_T}{\beta_p}
\]

- Improved current mirror can be used to reduce the systematic input offset