CHAPTER 7 BUILDING BLOCKS OF INTEGRATED-CIRCUIT AMPLIFIERS

Chapter Outline
7.1 IC Design Philosophy
7.2 The Basic Gain Cell
7.3 The Common-Gate and Common-Base Amplifiers
7.4 The Cascode Amplifier
7.5 IC Biasing
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7.1 IC Design Philosophy

Integrated circuits
- More and more electronics circuits are integrated in a single chip
  - More complicated functions
  - Smaller size and lower cost
  - Suitable for mass-production
- Implementation cost depends on device area rather than device count
  - Large/moderate-value resistors should be avoided
  - Larger/moderate-value capacitors should be avoided
  - Preferable to use transistors due to chip-area consideration

Design philosophy
- The design philosophy for ICs is different from that of discrete-component circuits
  - Realize as many of functions as possible by using transistors only
  - Rely on device matching or size ratios for circuit design
  - Active loads are typically used for amplifier designs
7.2 The Basic Gain Cell

The CS and CE amplifier with current-source loads

- Current-source-load CS amplifier:
  - Equivalent circuit
    \[ R_{in} = \infty \]
    \[ A_{vo} = -g_m r_o \]
    \[ R_o = r_o \]
  - Intrinsic gain
    \[ g_m = \frac{I_D}{V_{OV}/2} = \sqrt{2\mu_n C_{ox}(W/L)}I_D \]
    \[ r_o = \frac{V_A}{I_D} = \frac{V_A^L}{I_D} \]
    \[ A_0 \equiv g_m r_o = \frac{V_A}{V_{OV}/2} = \frac{2V_A^L}{V_{OV}} = V_A' \sqrt{\frac{2\mu_n C_{ox}WL}{I_D}} \]

- Intrinsic gain is only 20 to 40 V/V for a MOSFET in a modern short-channel technology
- For a given technology (fixed \( \mu_n C_{ox}, V_T \) and \( V'_A \)): larger \( A_0 \) as \( L \) increases
- For a given transistor (fixed \( \mu_n C_{ox}, V_T, V'_A, W \) and \( L \)): \( A_0 \) increases as \( V_{OV} \) and \( I_D \) decrease
- Gain levels off at very low currents as the MOSFET enters the subthreshold region operation where the drain current deviates from the saturation mode and becomes similar to a BJT with an exponential current-voltage characteristics
Output resistance of the current-source load

- The current source can be realized by using a PMOS in saturation
  - The output resistance is no longer infinite due to channel-length modulation
    \[ I = \frac{1}{2} \mu_p C_{ox} \left( \frac{W}{L} \right)_2 (V_{DD} - V_G - |V_{th}|)^2 \]
    \[ r_{o2} = \frac{|V_{Ap}|}{I} \]

- Voltage gain of the CS amplifier with a current-source load
  \[ A_v \equiv \frac{V_o}{V_i} = -g_{m1}(r_{o1})|r_{o2}| \]
  - The voltage gain is reduced due to the finite output resistance of the current-source load
  - The gain is reduced by half if \( Q_1 \) has the same Early voltage as \( Q_2 \) does \( (r_{o1} = r_{o2}) \)
Increasing the gain of the basic cell

- The gain is proportional to the resistance at the output
- It can be effectively increased by raising the output resistance of the gain cell
- Adding a current buffer:
  - Passes the current but raises the resistance level
  - The only candidate is CG or CB amplifier
  - Placing CG (or CB) on top of the CS (or CE) amplifying transistor is called cascoding

Gain enhancement:
- It is not sufficient to raise the output resistance of the amplifying transistor only
- A current buffer is also needed to raise the output resistance of the current-source load
Current-source-load CE amplifier:

- Equivalent circuit
  \[ R_{\text{in}} = r_\pi \]
  \[ A_{vo} = -g_m r_o \]
  \[ R_o = r_o \]

- Intrinsic gain
  \[ A_0 = g_m r_o = \frac{I_C V_A}{V_T I_C} = \frac{V_A}{V_T} \]

- Maximum gain obtainable in a CE amplifier (assuming an ideal dc current source)
- Technology-determined parameter
- Independent of the transistor junction area and the bias current for a given fabrication process
- \( V_A \) ranges from 5 to 35 V for modern IC fabrication process
- \( V_A \) ranges from 100 to 130 V for high-voltage process
- Intrinsic gain ranges from 200 to 5,000 V/V
7.3 The Common-Gate and Common-Base Amplifiers

The common-gate amplifier

- Circuit topology:
  - The signal source is connected to the source (input)
  - The load is connected to the drain (output)

- Input resistance:
  - The resistance looking into the source terminal
  - A load resistance $R_L$ is specified at the output
  - The input resistance is given by
    \[ R_{in} = \frac{r_o + R_L}{1 + g_m r_o} \approx \frac{1}{g_m} + \frac{R_L}{g_m r_o} \]
  - Input resistance reduces to $1/g_m$ if $r_o$ is infinite
  - Input resistance depends on $R_L$ if $r_o$ cannot be neglected
  - The load resistance is transformed to the input by dividing it by the intrinsic gain of the MOSFET
  - Input resistance is typically low for CG amplifiers due to the impedance transformation property
  - The CG amplifier can be used as a current buffer

\[ R_{in} = \frac{v_x}{i_x} \]

\[ R_{in} \approx \frac{v_x}{i_x} = \frac{r_o + R_L}{1 + g_m r_o} \approx \frac{1}{g_m} + \frac{R_L}{g_m r_o} \]
Output resistance:
- The resistance looking into the drain terminal
- A source resistance \( R_s \) is specified at the input
- The output resistance is given by
  \[ R_{out} = g_m r_o R_s + r_o + R_s \approx g_m r_o R_s \]
- Output resistance also depends on source resistance \( R_s \)
- CG amplifier transforms the source resistance \( R_s \) to the output by multiplying it by the intrinsic gain \( A_o \)
- The output resistance can be very large if \( R_s \) is large; this is also an important characteristic of a current buffer

Properties of CG amplifier:
- CG has a unity current gain; a low input resistance; a high output resistance
- It makes for an excellent current buffer
- Suitable for gain enhancement for the gain cell
- Impedance transformation properties can be used for analysis of the cascode amplifier
The common-base amplifier

- Circuit topology:
  - The signal source is connected to the emitter (input)
  - The load is connected to the collector (output)

- Input resistance:
  - The resistance looking into the emitter terminal
  - A load resistance $R_L$ is specified at the output
  - The input resistance is given by

$$R_{in} \approx r_e \frac{r_o + R_L}{r_o + R_L/(eta + 1)}$$

- $R_{in}$ reduces to $r_e$ if $r_o$ is infinite
- If $r_o$ cannot be neglected
  - $R_{in} = r_e$ for $R_L = 0$
  - $R_{in} = r_e(\beta+1) = r_\pi$ for $R_L = \infty$
  - $R_{in} \approx r_e + R_L/(g_m r_o)$ for $R_L << (\beta+1)r_o$

$$\ell - v_x/r_e + g_m v_x$$

$$i_x = v_x/r_e + g_m v_x$$

$$i_x - v_x/r_e$$

$$\approx R_{in} = \frac{r_o + R_L}{1 + \frac{r_o}{r_e} + \frac{R_L}{(\beta + 1)r_e} \frac{r_o + R_L}{r_o + \frac{R_L}{\beta + 1}}}$$
Output resistance:

- The resistance looking into the collector terminal
- A source resistance $R_e$ is specified at the input
- The output resistance is given by
  $$R_{out} = g_m r_o (R_e || r_\pi) + r_o + R_e || r_\pi \approx g_m r_o (R_e || r_\pi) + r_o$$
- Similar to CG as $r_\pi$ and $R_e$ are considered in parallel
- Output resistance also depends on source resistance $R_e$
- CB has an important impedance transformation property that raises the output resistance
- Unlike CG, the output resistance of the CB circuit has an absolute maximum value as $R_e$ becomes infinite:
  $$R_{out\mid \text{max}} = r_o (\beta + 1)$$

Properties of CB amplifier:

- CB has a low input resistance; a high output resistance
- It makes for an excellent current buffer
- Suitable for gain enhancement for the gain cell
- Impedance transformation properties can be used for analysis of the cascode amplifier
7.4 Cascode Amplifier

The MOS cascode

- Circuit topology:
  - Putting a CG ($Q_2$: cascode transistor) on top of CS ($Q_1$: amplifying transistor)
  - The cascode transistor passes the small-signal current $g_m v_i$ to the output node while raising the resistance level by a factor of $K$

- Small-signal analysis
  - Transconductance: $G_m \approx g_m$

\[
\begin{align*}
    v_x \quad & v_{g1} = v_i \\
    g_m v_x & \quad v_1 / r_{o1} \\
    g_m v_x + v_1 / r_{o1} + g_m v_1 + v_1 / r_{o2} = 0 \\
    i_o + g_m v_1 + v_1 / r_{o2} = 0 \\
    \Rightarrow G_m = \frac{i_o}{v_x} = g_m \frac{g_m + r_{o2}^{-1}}{g_m + r_{o1}^{-1} + r_{o2}^{-1}} \approx g_m
\end{align*}
\]
Output resistance: \( R_o \approx g_{m2} r_{o2} r_{o1} = A_{o2} r_{o1} \)

- Voltage gain of the cascode amplifier
  - With an ideal current source:
    - Equivalent to infinite load resistance
    - \( A_{vo} = -G_m R_o = -g_{m1} r_{o1} g_{m2} r_{o2} = -A_0 r_{o2} \)
  - With a load resistance \( (R_L \ll R_o) \):
    - \( A_v = -G_m (R_o || R_l) \approx -g_{m1} R_l \)
  - With a PMOS current source load:
    - \( A_v = -G_m (R_o || r_{o3}) \approx -g_{m1} r_{o3} \)

\[
\begin{align*}
g_{m2} v_1 + v_1/r_{o1} &= (v_x - v_1)/r_{o2} \\
i_x + g_{m2} v_1 &= (v_x - v_1)/r_{o2} \\
\Rightarrow R_o \equiv \frac{v_x}{i_x} &= \frac{g_{m1} \left( g_{m2} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}} \right)}{\left( g_{m2} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}} \right) \frac{1}{r_{o2}}} \\
&\approx g_{m2} r_{o2} r_{o1} + r_{o1} + r_{o2}
\end{align*}
\]
The cascode amplifier with a cascode current-source load

- The DC voltage sources $V_{\text{DD}}$, $V_{G2}$, $V_{G3}$, and $V_{G4}$ are considered ground for ac analysis
- The cascode stage ($Q_1$-$Q_2$) is modeled by $G_m$ and $R_o$
  - $G_m = g_{m1}$ and $R_o = R_{on} \approx g_{m2}r_{o2}r_{oi}$
- The output resistance of the cascode current-source load:
  - $R_L = R_{op} = g_{m3}r_{o3}r_{o4} + r_{o3} + r_{o4} \approx g_{m3}r_{o3}r_{o4}$
- The voltage gain: $A_v = -G_m(R_o || R_L) = -g_{m4} (g_{m2}r_{o2}r_{oi} || g_{m3}r_{o3}r_{o4})$
- Assume $g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_m$ and $r_{oi} = r_{o2} = r_{o3} = r_{o4} = r_o$; $A_v = (g_m r_o)^2/2 = (A_0)^2/2$
Distribution of voltage gain in a cascode amplifier

- The input resistance of the common-gate transistor:
  \[ R_{in} = \frac{r_o + R_L}{1 + g_m r_o} \approx \frac{1}{g_m} + \frac{R_L}{g_m r_o} \]

- The cascode amplifier gain can be characterized as:
  - \( A_v = (v_o/v_i)(v_o/v_o) = A_{vr} A_{v2} \approx -g_m (g_m r_o || R_L) \)
  - \( A_{v1} \) (voltage gain from \( v_i \) to \( v_o \)) = \( v_o/v_i = -g_m (r_o || R_{in2}) \)
  - \( A_{v2} \) (voltage gain from \( v_{o1} \) to \( v_o \)) = \( A_v/A_{v1} \)
Summary table of gain distribution with small-signal parameters $g_m$ and $r_o$

<table>
<thead>
<tr>
<th>Case</th>
<th>$R_L$</th>
<th>$R_{m2}$</th>
<th>$R_{d1}$</th>
<th>$A_{vl}$</th>
<th>$A_{v2}$</th>
<th>$A_v$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$\infty$</td>
<td>$\infty$</td>
<td>$r_o$</td>
<td>$-g_m r_o$</td>
<td>$g_m r_o$</td>
<td>$-(g_m r_o)^2$</td>
</tr>
<tr>
<td>2</td>
<td>$(g_m r_o) r_o$</td>
<td>$r_o$</td>
<td>$r_o/2$</td>
<td>$-\frac{1}{2}(g_m r_o)$</td>
<td>$g_m r_o$</td>
<td>$-\frac{1}{2}(g_m r_o)^2$</td>
</tr>
<tr>
<td>3</td>
<td>$r_o$</td>
<td>$\frac{2}{g_m}$</td>
<td>$\frac{2}{g_m}$</td>
<td>$-2$</td>
<td>$\frac{1}{2}(g_m r_o)$</td>
<td>$-(g_m r_o)$</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>$\frac{1}{g_m}$</td>
<td>$\frac{1}{g_m}$</td>
<td>$-1$</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
**Double cascoding**

- Even higher output resistance can be achieved in MOSFET circuits by double cascoding.
- Requires higher supply voltage as one more CG transistor is stacked in the gain stage.
- Double cascoding is typically required for the current-source load to boost the voltage gain.
- Double cascode stage is modeled by:
  - $G_m = g_{m1}$
  - $R_o = g_{m3}r_{o3}g_{m2}r_{o2}r_{o1} \approx (A_o)^2r_{o1}$
The folded cascode

- Folded cascode utilizes a PMOS as the cascode transistor
- The dc current of $Q_2$ is $I_2$ and the current of $Q_1$ is $(I_1 - I_2)$
- The voltage limitation due to stacking of NMOS transistors can be alleviated
- Small-signal operation is similar to the case of NMOS cascode
**The BJT cascode**

- The BJT cascode consists of CE and CB transistor in stack
  - The BJT cascode modeled by $R_{in}$, $G_m$ and $R_o$
  - Input resistance: $R_{in} = r_{\pi 1}$

- Transconductance: $G_m \approx g_{m1}$

\[ g_{m1} v_x + v_1/r_{\pi 2} + v_1/r_{\pi 2} + g_{m2} v_1 + v_1/r_{o2} = 0 \]
\[ i_o + g_{m2} v_1 + v_1/r_{o2} = 0 \]
\[ \rightarrow G_m = \frac{i_o}{v_x} = \frac{g_{m1}}{g_{m2} + r_{\pi 2}^{-1} + r_{o1}^{-1} + r_{o2}^{-1}} \approx g_{m1} \]
Output resistance: $R_o = r_{o2} + (r_{o1}||r_{\pi2}) + g_{m2}r_{o2}(r_{o1}||r_{\pi2}) \equiv g_{m2}r_{\pi2}r_{o2} = \beta_2 r_{o2}$

$\Rightarrow$ Double cascoding is not useful for BJT circuits ($R_o$ won’t be further raised by double cascoding)

Open-circuit voltage gain: $A_{vo} = -G_m R_o \equiv -g_m (g_{m2}r_{o2})(r_{o1}||r_{\pi2})$

$\Rightarrow$ For $g_{m1} = g_{m2} = g_m$ and $r_{o1} = r_{o2} = r_o$: $A_{vo} = -G_m R_o = -g_m (g_m r_o)(r_o||r_{\pi}) = -\beta (g_m r_o) = -\beta A_o$

Similar to MOS case with $r_{o1}||r_{\pi2}$
The BJT cascode amplifier with a cascode current-source load

- DC voltage sources $V_{CC}$, $V_{B2}$, $V_{B3}$, and $V_{B4}$ are considered ground for ac analysis
- The cascode stage ($Q_1$-$Q_2$) is modeled by $G_m$ and $R_o$
  \[ G_m = g_{m1} \text{ and } R_o = R_{on} \cong g_{m2}r_{\pi2}r_{o2} = \beta_2 r_{o2} \]
- The output resistance of the cascode current-source load:
  \[ R_L = R_{op} \cong g_{m3}r_{\pi3}r_{o3} = \beta_3 r_{o3} \]
- The voltage gain: $A_v = -G_m(R_o||R_L) = -g_{m1}(\beta_2 r_{o2}||\beta_3 r_{o3})$
- Assume $g_m$, $\beta$ and $r_o$ are identical, $A_v = -\beta g_m r_o/2 = -\beta A_o/2$

**Distribution of voltage gain in a cascode amplifier**

- The input resistance of the common-gate transistor:
  \[ R_{in2} = r_{e2}(r_{o2}+R_L)/[r_{o2}+R_L/(\beta+1)] \]
- The cascode amplifier gain can be characterized as
  \[ A_v = (v_{o1}/v_i)(v_o/v_{o1}) = A_{v1}A_{v2} \cong -g_{m1}(\beta_2 r_{o2}||R_L) \]
  \[ A_{v1} \text{ (voltage gain from } v_i \text{ to } v_{o1}) = v_{o1}/v_i = -g_{m1}(r_{o1}||R_{in2}) \]
  \[ A_{v2} \text{ (voltage gain from } v_{o1} \text{ to } v_o) = A_v/A_{v1} \]

**Double cascoding**

- No significant increase in $R_o$ by using double cascode
- Not a useful technique to boost gain for BJT circuits

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### 7.5 IC Biasing

**Current source for IC biasing**
- Widely used technique for ICs with good device matching
- Can be implemented in MOS and BJT circuits
- Nonideal effect due to finite output resistance

**Basic MOSFET current source**
- MOSFET current mirror
  - Widely used for ICs with good device matching
  - $Q_1$ and $Q_2$ are identical and in saturation:
    \[
    I_{D1} = I_{REF} = \frac{1}{2} k' \frac{W}{L} (V_{GS} - V_{th})^2 = \frac{V_{DD} - V_{GS}}{R}
    \]
    \[
    I_O = I_{D2} = I_{D1} = I_{REF}
    \]
  - Current gain or **current transfer ratio**:
    \[
    \frac{I_O}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}
    \]
- Effect of $V_O$ on $I_O$
  - Current mismatch due to channel-length modulation
    \[
    I_O = \frac{(W/L)_2}{(W/L)_1} I_{REF} \left( 1 + \frac{V_O - V_{GS}}{V_A} \right)
    \]

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MOS current-steering circuits

- **Current sink**: pulls a dc current from a circuit
- **Current source**: pushes a dc current into a circuit
- All transistors should be operated in saturation
- Current mismatch exists for a finite $V_A$ (channel-length modulation)
Basic BJT current mirror

- The case of infinite $\beta$:
  - Current is proportional to the area of EB junction
  \[ \frac{I_O}{I_{REF}} = \frac{I_{S2}}{I_{S1}} = \frac{A_{E2}}{A_{E1}} \]

- The case of finite $\beta$:
  - $Q_1$ and $Q_2$ identical:
  \[ \frac{I_O}{I_{REF}} = \frac{1}{1 + \frac{2}{\beta}} \]
  - Current transfer ratio $m$ (with infinite output resistance):
  \[ \frac{I_O}{I_{REF}} = \frac{m}{1 + \frac{m+1}{\beta}} \]
  - Current transfer ratio $m$ (with finite output resistance):
  \[ \frac{I_O}{I_{REF}} = \frac{m}{1 + \frac{m+1}{\beta}} \left(1 + \frac{V_O - V_{BE}}{V_A}\right) \]
BJT current steering

- Provides current source and current sink by using BJT devices

\[ I_{REF} = \frac{V_{CC} + V_{EE} - V_{BE1} - V_{BE2}}{R} \]

\[ I_1 = \frac{1}{1 + \frac{4}{\beta_{pnp}}} I_{REF} \]

\[ I_2 = \frac{1}{1 + \frac{5}{\beta_{nnp}}} I_{REF} \]

\[ I_3 = \frac{2}{1 + \frac{4}{\beta_{pnp}}} I_{REF} \]

\[ I_4 = \frac{3}{1 + \frac{5}{\beta_{nnp}}} I_{REF} \]
7.6 Current-Mirror Circuits with Improved Performance

The constant-current source
- Used both in biasing and as active load
- Performance improvement of current mirrors
  - The accuracy of the current transfer ratio of the current mirror (BJT)
  - The output resistance of the current source (BJT and MOS)

Cascode MOS current mirrors
- The output resistance is raised by a factor of $g_{m3}r_{o3}$ (the intrinsic gain of the cascode transistor)
- The minimum voltage at the output of the current source is $V_t + 2V_{OV}$ ($V_{OV}$ for basic current source)
A bipolar mirror with base-current compensation

- Base-current compensation by an additional transistor $Q_3$
- The current transfer ratio is much less dependent on $\beta$

\[
\frac{I_O}{I_{REF}} = \frac{1}{1 + \frac{2}{\beta(\beta + 1)}} \approx \frac{1}{1 + \frac{2}{\beta^2}}
\]

- Current transfer ratio $m$:

\[
\frac{I_O}{I_{REF}} = \frac{m}{1 + \frac{m + 1}{\beta(\beta + 1)}} \approx \frac{m}{1 + \frac{m + 1}{\beta^2}}
\]

- Output resistance

\[R_O \approx r_o\]

- The minimum voltage at the output:

\[V_O \geq V_{CE\text{sat}} \approx 0.2V\]

Cascode BJT current mirror

- The current transfer ratio is not improved by cascoding

\[\frac{I_O}{I_{REF}} \approx \frac{1}{1 + 2/\beta}\]

- Output resistance is boosted by cascoding

\[R_O \approx \beta r_o\]

- The minimum voltage at the output:

\[V_O \geq V_BE + V_{CE\text{sat}} \approx 0.9V\]
The Wilson current mirror

- Improving the current transfer ratio and output resistance
- The current transfer ratio:

\[
\frac{I_o}{I_{REF}} = \frac{I_c \left(1 + \frac{2}{\beta}\right) \left(\frac{\beta}{\beta + 1}\right)}{I_c \left[1 + \left(1 + \frac{2}{\beta}\right) \left(\frac{\beta}{\beta + 1}\right)\right]} = \frac{1}{1 + \frac{2}{\beta(\beta + 2)}} \approx \frac{1}{1 + \frac{2}{\beta^2}}
\]

- Output resistance:

\[
R_O \equiv \frac{v_x}{i} = \left(\frac{\beta_3}{2} + 1\right) r_o + \frac{r_e}{2} \approx \frac{1}{2} \beta_3 r_o
\]

- The minimum voltage at the output:

\[
V_o \geq V_{BE} + V_{CESat} \approx 0.9V
\]

- Comparison with cascode current mirror
  - Reduced $\beta$-dependence for the current transfer ratio
  - Output resistance is approximately reduced by half
  - Similar voltage headroom needed at output
The Wilson MOS mirror

- Similar to the bipolar Wilson mirror
- Output resistance:
  \[ R_o = g_{m3} r_{o3} r_{o2} + r_{o3} + 1/g_{m1} \approx g_{m3} r_{o3} r_{o2} \]
- The minimum voltage at the output:
  \[ V_o \geq V_t + 2V_{OV} \]
- Significant difference in \( V_{DS} \) leads to drain current mismatch between \( Q_1 \) and \( Q_2 \)
- Modified circuit by adding \( Q_4 \) to avoid current error
The Widlar current source

- Allows the generation of a small constant current using relatively small resistors
- Advantageous in considerable savings in chip area for integrated circuits
- Circuit performance
  - Output current:
    \[ V_{BE1} = V_T \ln \left( \frac{I_{REF}}{I_S} \right) \]
    \[ V_{BE2} = V_T \ln \left( \frac{I_O}{I_S} \right) \]
    \[ V_{BE1} - V_{BE2} = V_T \ln \left( \frac{I_{REF}}{I_O} \right) = I_0 R_E \]
    \[ \Rightarrow R_E = \frac{V_T}{I_O} \ln \left( \frac{I_{REF}}{I_O} \right) \]
    \[ \Rightarrow I_O = \frac{V_T}{R_E} \ln \left( \frac{I_{REF}}{I_O} \right) \]
  - Output resistance:
    \[ R_o \approx [1 + g_m2(R_E||r_{\pi2})]r_{a2} \]