CHAPTER 7 BUILDING BLOCKS OF INTEGRATED-CIRCUIT AMPLIFIERS

Chapter Outline
7.1 IC Design Philosophy
7.2 The Basic Gain Cell
7.3 The Cascode Amplifier
7.4 IC Biasing
7.5 Current-Mirror Circuits with Improved Performance
7.1 IC Design Philosophy

Integrated circuits

- More and more electronics circuits are integrated in a single chip
  - More complicated functions
  - Smaller size and lower cost
  - Suitable for mass-production
- Implementation cost depends on device area rather than device count
  - Large/moderate-value resistors should be avoided
  - Larger/moderate-value capacitors should be avoided
  - Preferable to use transistors due to chip-area consideration

Design philosophy

- The design philosophy for ICs is different from that of discrete-component circuits
  - Realize as many of functions as possible by using transistors only
  - Rely on device matching or size ratios for circuit design
  - Active loads are typically used for amplifier designs
7.2 The Basic Gain Cell

The CS and CE amplifier with current-source loads

- Active-load CS amplifier:
  - Equivalent circuit
    \[ R_{in} = \infty \]
    \[ A_{vo} = -g_m r_o \]
    \[ R_o = r_o \]
  - Intrinsic gain
    \[ g_m = \frac{I_D}{V_{OV} / 2} = \sqrt{2\mu_n C_{ox} (W/L)} \cdot \sqrt{I_D} \]
    \[ r_o = \frac{V_A}{I_D} = \frac{V'_D}{I_D} \]
    \[ A_0 = \frac{V_A}{V_{OV} / 2} = \frac{2V'_D}{V_{OV}} = \frac{V'_D \sqrt{2\mu_n C_{ox} W L}}{\sqrt{I_D}} \]

  ➤ Intrinsic gain is only 20 to 40 V/V for a MOSFET in a modern short-channel technology
  ➤ For a given technology: larger \( A_o \) as \( V_{OV} \) decreases and \( L \) increases
  ➤ For a given transistor: \( A_o \) increases as \( V_{OV} \) and \( I_D \) decrease
  ➤ Gain levels off at very low currents as the MOSFET enters the subthreshold region operation

  where it becomes similar to a BJT with an exponential current-voltage characteristics

- \( NTUEE \quad Electronics \quad - \quad L.H. \quad Lu \)
Active-load CE amplifier:

- Equivalent circuit
  
  \[ R_{in} = r_z \]
  \[ A_v = -g_m r_o \]
  \[ R_o = r_o \]

- Intrinsic gain
  
  \[ A_0 = g_m r_o = \frac{I_C}{I_T} \cdot \frac{V_A}{V_T} = \frac{V_A}{V_T} \]

  ➤ Maximum gain obtainable in a CE amplifier (assuming an ideal dc current source)
  ➤ Technology-determined parameter
  ➤ Independent of the transistor junction area and the bias current for a given fabrication process
  ➤ \( V_A \) ranges from 5 to 35 V for modern IC fabrication process
  ➤ \( V_A \) ranges from 100 to 130 V for high-voltage process
  ➤ Intrinsic gain ranges from 200 to 5000 V/V
Output resistance of the current-source load

- The current source can be realized by using a PMOS in saturation
  - The output resistance is no longer infinite due to channel-length modulation

$$I = \frac{1}{2} \mu_p C_{ox} \left( \frac{W}{L} \right) \left( V_{DD} - V_G - |V_t| \right)^2$$

$$r_{o2} = \frac{|V_{A2}|}{I}$$

- Voltage gain of the CS amplifier with a current-source load
  - The voltage gain is reduced due to the finite output resistance of the current-source load
  - The gain is reduced by half if $Q_1$ has the same Early voltage as $Q_2$ does ($r_{o1} = r_{o2}$)
Increasing the gain of the basic cell

- The gain is proportional to the resistance at the output
- It can be effectively increased by raising the output resistance of the gain cell
- Adding a current buffer:
  - Passes the current but raises the resistance level
  - The only candidate is CG or CB amplifier
  - Placing CG (or CB) on top of the CS (or CE) amplifying transistor is called **cascoding**

Gain enhancement:

- It is not sufficient to raise the output resistance of the amplifying transistor only
- A current buffer is also needed to raise the output resistance of the current-source load
7.3 Cascode Amplifier

The MOS cascode

- Circuit topology:
  - Putting a CG ($Q_2$: cascode transistor) on top of CS ($Q_1$: amplifying transistor)
  - The cascode transistor passes the small-signal current $g_{m1}v_i$ to the output node while raising the resistance level by a factor of $K$

- Small-signal analysis
  - Transconductance
    $$G_m = g_{m1}$$

Transistor biasing

$$v_x = v_{gs1} = v_1$$

$$g_{m1}v_x$$

$$v_i / r_{o1}$$

$$g_{m2}v_1$$

$$v_i / r_{o2}$$

$$i_o = g_{m2}v_1 + v_i / r_{o2} = 0$$

$$v_{gs2} = v_1$$

$$v_i / r_{o2}$$

$$g_{m1}v_x + v_i / r_{o1} + g_{m2}v_1 + v_i / r_{o2} = 0$$

$$i_o + g_{m2}v_1 + v_i / r_{o2} = 0$$

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Output resistance
\[ R_o = r_{o1} + r_{o2} + g_{m2}r_{o2}r_{o1} \approx g_{m2}r_{o2}r_{o1} \]
\[ K = A_{o2} = g_{m2}r_{o2} \]

Voltage gain of the cascode amplifier with an ideal current source
\[ A_{vo} = \frac{v_o}{v_i} = -g_m R_o = -g_{m1}r_{o1}g_{m2}r_{o2} = -A_{o1}A_{o2} \approx -A_0^2 \]
The cascode amplifier with a cascode current-source load

- The output resistance of the cascode current-source load

\[ R_o = r_{o3} + r_{o4} + g_{m3}r_{o3}r_{o4} \approx g_{m3}r_{o3}r_{o4} \]

- Voltage gain of the amplifier

\[ A_i \equiv \frac{v_o}{v_i} = -g_{m1} \left( R_{on} \parallel R_{op} \right) \]
\[ = -g_{m1} \left[ (g_{m2}r_{o2})r_{o1} \parallel (g_{m3}r_{o3})r_{o4} \right] \approx -\frac{1}{2} A_0^2 \]
Distribution of voltage gain in a cascode amplifier

- The cascode amplifier gain can be characterized as
  - $A_{v1}$: voltage gain from $v_i$ to $v_{o1}$
  - $A_{v2}$: voltage gain from $v_{o1}$ to $v_o$

\[
A_v = A_{v1} \cdot A_{v2} = \frac{v_{o1}}{v_i} \cdot \frac{v_o}{v_{o1}}
\]
\[
R_{in2} \equiv -\frac{v_{g2}}{i} = \frac{R_L + r_{o2}}{1 + g_{m2}r_{o2}} \approx \frac{R_L}{g_{m2}r_{o2}} + 1
\]
\[
A_{v1} = \frac{v_{o1}}{v_i} = -g_{m1}R_{d1} = -g_{m1}(r_{o1} \parallel R_{in2})
\]
\[
A_{v2} = \frac{A_v}{A_{v1}}
\]

$$g_{m2}v_x + \frac{(v_x - v_i)}{r_{o2}} = \frac{v_i}{r_{o2}}$$

$$i_x = g_{m2}v_x + \frac{(v_x - v_i)}{r_{o2}}$$
Summary table of gain distribution with small-signal parameters $g_m$ and $r_o$

$$A_i = -g_m (g_m r_o^2 \parallel R_L) \quad A_{v1} = -g_m (r_o \parallel R_{in2}) \quad A_{v2} = \frac{A_v}{A_{v1}}$$

<table>
<thead>
<tr>
<th>Case</th>
<th>$R_L$</th>
<th>$R_{in2}$</th>
<th>$R_{d1}$</th>
<th>$A_{v1}$</th>
<th>$A_{v2}$</th>
<th>$A_v$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$\infty$</td>
<td>$\infty$</td>
<td>$r_o$</td>
<td>$-g_m r_o$</td>
<td>$g_m r_o$</td>
<td>$-(g_m r_o)^2$</td>
</tr>
<tr>
<td>2</td>
<td>$(g_m r_o) r_o$</td>
<td>$r_o$</td>
<td>$r_o/2$</td>
<td>$-\frac{1}{2} (g_m r_o)$</td>
<td>$g_m r_o$</td>
<td>$-\frac{1}{2} (g_m r_o)^2$</td>
</tr>
<tr>
<td>3</td>
<td>$r_o$</td>
<td>$\frac{2}{g_m}$</td>
<td>$\frac{2}{g_m}$</td>
<td>$-2$</td>
<td>$\frac{1}{2} (g_m r_o)$</td>
<td>$-(g_m r_o)$</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>$\frac{1}{g_m}$</td>
<td>$\frac{1}{g_m}$</td>
<td>$-1$</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Output resistance of a source-degenerated CS amplifier

$$R_o = r_o + R_s + g_m r_o R_s$$
$$= r_o + (1 + g_m r_o) R_s$$

$$R_{in} = \frac{r_o + R_L}{1 + g_m r_o}$$
$$\approx \frac{1}{g_m} + \frac{R_L}{(1 + g_m r_o)}$$

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**Double cascoding**

- Even higher output resistance can be achieved in MOSFET circuits by double cascoding
- Requires higher supply voltage as one more CG transistor is stacked in the gain stage
- Double cascoding is required for the current-source load to realize the advantage in voltage gain

**The folded cascode**

- Folded cascode utilizes a PMOS as the cascode transistor
- The dc current of \( Q_2 \) is \( I_2 \) and the current of \( Q_1 \) is \( (I_1 - I_2) \)
- The voltage limitation due to stacking of NMOS transistors can be alleviated
- Small-signal operation is similar of NMOS cascode

\[
V_{DD} \quad I \quad Q_3 \quad v_o
\]

\[
V_{G3} \quad (g_{m3}r_{o3})(g_{m2}r_{o2})r_{o1} = A_0^3 r_o
\]

\[
V_{G2} \quad Q_2 \quad v_o \quad (g_{m2}r_{o2})r_{o1}
\]

\[
v_i \quad Q_1 \quad r_{o1}
\]

\[
v_o \quad Q_2 \quad V_{G2}
\]

\[
V_{DD} \quad I_1 \quad Q_1 \quad Q_2 \quad v_o
\]

\[
I_2 \quad v_i
\]
The BJT cascode

- Consists of a CE and a CB transistor
  - Equivalent circuit:
  - Input resistance:
    \[ R_m = r_{\alpha 1} \]

- Transconductance:

\[
G_m = \frac{g_{m1}(g_{m2} + r_{o2}^{-1})}{(g_{m2} + r_{\pi 2}^{-1} + r_{o1}^{-1} + r_{o2}^{-1})} \approx g_{m1}
\]
■ Output resistance:

\[ R_o = r_{o2} + (r_{o1} \parallel r_{\pi2}) + g_{m2}r_{o2}(r_{o1} \parallel r_{\pi2}) \approx g_{m2}r_{o2}(r_{o1} \parallel r_{\pi2}) \]

\[ R_o^{\text{max}} = g_{m2}r_{\pi2}r_{o2} = \beta r_{o2} \]

⇒ Double cascoding with a BJT would not be useful \((R_o\) won’t be further raised by double cascoding)

![Diagram of BJT cascode circuit](image)

■ Open-circuit voltage gain:

\[ A_{yo} = \frac{V_o}{V_i} = -G_mR_o = -g_m(g_{m2}r_{o2})(r_{o1} \parallel r_{\pi2}) \]

⇒ For \( g_{m1} = g_{m2} = g_m \) and \( r_{o1} = r_{o2} = r_o \)

\[ A_{yo} = -g_m(g_mr_o)(r_o \parallel r_{\pi}) \]

\[ |A_{yo}|^{\text{max}} = \beta(g_mr_o) = \beta A_0 \]

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BJT cascode amplifier with a cascode current source

Output resistance of an emitter-degenerated CE amplifier

\[ R_{\text{op}} = (g_m r_{o2})(r_{o1}||r_{e2}) \]

\[ R_{\text{on}} = (g_m r_{o2})(r_{o1}||r_{e2}) \]

\[ A_v = -g_m (R_{\text{on}}||R_{\text{op}}) \]

\[ R_0 = r_o + (R_e||r_o) + g_m r_e (R_e||r_o) \]

\[ = r_o [1 + g_m (R_e||r_o)] \]

\[ R_{\text{in}} = \frac{r_o + R_L}{1 + \frac{1}{\alpha} g_m r_o + \frac{R_L}{r_o}} \]

\[ = r_e + \frac{R_L}{1 + g_m r_o} \text{, for } R_L \ll \beta r_o \]

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7.4 IC Biasing

Basic MOSFET current source

- MOSFET current mirror
  - Widely used for ICs with good device matching
  - \( Q_1 \) and \( Q_2 \) are identical and in saturation:
    \[
    I_D = I_{REF} = \frac{1}{2} k' \left( \frac{W}{L} \right)_1 \left( V_{GS} - V_m \right)^2 = \frac{V_{DD} - V_{GS}}{R}
    \]
    \[
    I_o = I_{D2} = I_{REF}
    \]
  - Current gain or current transfer ratio:
    \[
    \frac{I_o}{I_{REF}} = \frac{(W / L)_2}{(W / L)_1}
    \]

- Effect of \( V_O \) on \( I_O \)
  - Current mismatch due to channel-length modulation
    \[
    I_o = \frac{(W / L)_2}{(W / L)_1} I_{REF} \left( 1 + \frac{V_O - V_{GS}}{V_{A2}} \right)
    \]
MOS current-steering circuits

- **Current sink**: pulls a dc current from a circuit
- **Current source**: pushes a dc current into a circuit
- All transistors should be operated in saturation
- Current mismatch exists for a finite $V_A$ (channel-length modulation)
Basic BJT current mirror

- The case of infinite $\beta$:
  - Current is proportional to the area of EB junction
    \[
    \frac{I_O}{I_{REF}} = \frac{I_{S2}}{I_{S1}} = \frac{A_{E2}}{A_{E1}}
    \]

- The case of finite $\beta$:
  - $Q_1$ and $Q_2$ identical:
    \[
    \frac{I_O}{I_{REF}} = \frac{1}{1+\frac{2}{\beta}}
    \]
  - Current transfer ratio $m$ (with infinite output resistance):
    \[
    \frac{I_O}{I_{REF}} = \frac{m}{1+\frac{m+1}{\beta}}
    \]
  - Current transfer ration $m$ (with finite output resistance):
    \[
    \frac{I_O}{I_{REF}} = \frac{m}{1+\frac{m+1}{\beta}} \left(1 + \frac{V_O - V_{BE}}{V_{A2}}\right)
    \]
BJT current steering

- Provides current source and current sink by using BJT devices

\[
I_{\text{REF}} = \frac{V_{CC} + V_{EE} - V_{EB1} - V_{BE2}}{R}
\]

\[
I_1 = \frac{1}{4} I_{\text{REF}} \frac{1}{1 + \frac{4}{\beta_{\text{pnp}}}}
\]

\[
I_2 = \frac{1}{5} I_{\text{REF}} \frac{1}{1 + \frac{5}{\beta_{\text{npn}}}}
\]

\[
I_3 = \frac{2}{4} I_{\text{REF}} \frac{1}{1 + \frac{4}{\beta_{\text{pnp}}}}
\]

\[
I_4 = \frac{3}{5} I_{\text{REF}} \frac{1}{1 + \frac{5}{\beta_{\text{npn}}}}
\]

<Diagram of BJT current steering circuit>

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7.5 Current-Mirror Circuits with Improved Performance

The constant-current source
- Used both in biasing and as active load
- Performance improvement of current mirrors
  - The accuracy of the current transfer ratio of the current mirror
  - The output resistance of the current source

Cascode MOS current mirrors
- The output resistance is raised by a factor of $g_{m3} r_{o3}$ (the intrinsic gain of the cascode transistor)
- The minimum voltage at the output of the current source is $V_t + 2V_{OV}$ ($V_{OV}$ for basic current source)

![Diagram of a cascode MOS current mirror circuit]
A bipolar mirror with base-current compensation

- Base-current compensation by an additional transistor $Q_3$
- The current transfer ratio is much less dependent on $\beta$

$$\frac{I_o}{I_{REF}} = \frac{1}{1 + \frac{2}{\beta(\beta+1)}} \approx \frac{1}{1 + \frac{2}{\beta^2}}$$

- Output resistance
  $$R_o \approx r_{o2}$$

The Wilson current mirror

- Improving the current transfer ratio and output resistance
- The current transfer ratio:

$$\frac{I_o}{I_{REF}} = \frac{I_c \left(1 + \frac{2}{\beta} \left(\frac{\beta}{\beta+1}\right)\right)}{I_c \left[1 + \left(1 + \frac{2}{\beta} \left(\frac{1}{\beta+1}\right)\right)\right]} = \frac{\beta + 2}{\beta + 1 + \frac{\beta+2}{\beta}} = \frac{1}{1 + \frac{2}{\beta(\beta+2)}} \approx \frac{1}{1 + \frac{2}{\beta^2}}$$

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- Output resistance:
  \[ R_o = \frac{v_o}{i_x} = \left( \frac{\beta_1}{2} + 1 \right) r_{o3} + \frac{r_{e1}}{2} \approx \frac{1}{2} \beta_3 r_{o3} \]

- Comparison with cascode current mirror
  - Reduced \( \beta \)-dependence for the current transfer ratio
  - Output resistance is approximately reduced by half
  - Requires an additional \( V_{BE} \) like the cascode mirror

**The Wilson MOS mirror**

- Similar to the bipolar Wilson mirror
  - Output resistance:
    \[ R_o = g_{m3} r_{o3} r_{o2} + \frac{1}{g_{m1}} \approx g_{m3} r_{o3} r_{o2} \]

- Modified circuit to avoid systematic current error resulting from the difference in \( V_{DS} \) between \( Q_1 \) and \( Q_2 \)
The Widlar current source

- Allows the generation of a small constant current using relatively small resistors
- Advantageous in considerable savings in chip area for integrated circuits
- Circuit performance
  - Output current:
    \[ V_{BE1} = V_T \ln \left( \frac{I_{REF}}{I_S} \right) \]
    \[ V_{BE2} = V_T \ln \left( \frac{I_O}{I_S} \right) \]
    \[ V_{BE1} - V_{BE2} = V_T \ln \left( \frac{I_{REF}}{I_O} \right) = I_o R_E \]
  - Output resistance:
    \[ R_o \approx [1 + g_{m3} (R_E || r_\pi)]r_o \]