CHAPTER 14 CMOS DIGITAL LOGIC CIRCUITS

Chapter Outline
14.1 Digital Logic Inverters
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14.4 CMOS Logic-Gate Circuits
14.5 Implications of Technology Scaling: Issues in Deep-Submicron Design
14.1 DIGITAL LOGIC INVERTERS

The Voltage-Transfer Characteristic (VTC)

- The function of the inverter is to invert the logic value of its input signal
- The voltage-transfer characteristic is used to evaluate the quality of inverter operation

![Diagram of inverter circuit and voltage-transfer characteristic curve]

- VTC parameters
  - $V_{OH}$: output high level
  - $V_{OL}$: output low level
  - $V_{IH}$: the minimum value of input interpreted by the inverter as a logic 1
  - $V_{IL}$: the maximum value of input interpreted by the inverter as a logic 0
  - Transition region: input level between $V_{IL}$ and $V_{IH}$
Noise Margins

- The VTC is generally non-linear
- $V_{IH}$ and $V_{IL}$ are defined as the points at which the slope of the VTC is $-1$
- Robustness (noise margin at a high level): $NM_H = V_{OH} - V_{IH}$
- Robustness (noise margin at a low level): $NM_L = V_{IL} - V_{OL}$
- Static inverter characteristics for ideal VTC:
  - $V_{OH} = V_{DD}$
  - $V_{OL} = 0$
  - $V_{IH} = V_{IL} = V_{DD}/2$
  - $NM_H = NM_L = V_{DD}/2$

![Ideal VTC Diagram](image)
Power Dissipation
- Static power dissipation: power dissipated when the inverter stays in logic 0 or logic 1
- Dynamic power dissipation: power dissipated as the output is switching

\[ P_D = f CV_{DD}^2 \]

Propagation Delay
- \( t_{PHL} \): high-to-low propagation delay
- \( t_{PLH} \): low-to-high propagation delay
- \( t_p \) (propagation delay) = ( \( t_{PLH} + t_{PHL} \))/2
- Maximum switching frequency \( f_{max} = 1/2t_p \)
- The output transient of the inverter can be characterized by a \( RC \) charge/discharge model

\[ v_o(t) = V_x - (V_x - V_{0+})e^{-t/RC} \]
**Power-Delay Product and Energy-Delay Product**

- Power and delay are often in conflict for inverter operation
- Power-delay product is a figure-of-merit for comparing logic-circuit technologies or families
- Power-delay product is defined as \( PDP = P_d t_p = C V_{DD}^2 / 2 \)
- Energy-delay product is defined as \( EDP = C V_{DD} V_{pd} / 2 \)

**Silicon Area**

- Area reduction through advances in processing technology
- Area reduction through advances in circuit design techniques
- Area reduction through careful chip layout

**Fan-In and Fan-Out**

- Fan-in of a gate is the number of its inputs
- Fan-out is the maximum number of similar gates that a gate can drive

**Logic-Circuit Families**

[Diagram showing digital IC technologies and logic-circuit families, including CMOS, Bipolar, BiCMOS, GaAs, Complementary CMOS, Pseudo-NMOS, Pass-transistor logic, Dynamic logic, TTL, and ECL.]
**Inverter Implementation**

- Simplest implementation of the inverter with a MOSFET and a load

![Simplest implementation diagram]

- Inverter implementation with complementary switches

![Complementary switches diagram]

- Inverter implementation with a double-throw switch

![Double-throw switch diagram]
14.2 THE CMOS INVERTER

Circuit Operation

- A CMOS inverter consists of an n-channel and a p-channel MOSFET
- The n-channel device turns on and the p-channel device turns off as the input level goes high
- The p-channel device turns on and the n-channel device turns off as the input level goes low
- The turn-on device is modeled by a resistance: \( r_{DSN} = \left[ k_n (W/L_n)(V_{DD} - V_{th}) \right]^1 \) and \( r_{DSP} = \left[ k_p (W/L_p)(V_{DD} - |V_{th}|) \right]^1 \)
- \( V_{OH} = V_{DD} \) and \( V_{OL} = 0 \) for any CMOS inverter
The Voltage-Transfer Characteristic

- The transistors go through five different operation regions as the input goes from 0 to $V_{DD}$
- The operating point is obtained by making $i_{DN} = i_{DP}$

- **Region I:** ($Q_N$ off; $Q_P$ tri.)  
  $i_{DN} = 0 = i_{DP}$

- **Region II:** ($Q_N$ sat.; $Q_P$ tri.)  
  $i_{DN} = \frac{1}{2} k_n (v_I - V_m)^2 = i_{DP} = \frac{1}{2} k_p (V_{DD} - v_I - |V_{tp}|)(V_{DD} - v_O) - \frac{1}{2} (V_{DD} - v_O)^2$

- **Region III:** ($Q_N$ sat; $Q_P$ sat)  
  $i_{DN} = \frac{1}{2} k_n (v_I - V_m)^2 = i_{DP} = \frac{1}{2} k_p (V_{DD} - v_I - |V_{tp}|)^2$

- **Region IV:** ($Q_N$ tri.; $Q_P$ sat.)  
  $i_{DN} = k_n (v_I - V_m)v_O - \frac{1}{2} v_O^2 = i_{DP} = \frac{1}{2} k_p (V_{DD} - v_I - |V_{tp}|)^2$

- **Region V:** ($Q_N$ tri.; $Q_P$ off)  
  $i_{DN} = i_{DP} (= 0)$
Static Characteristics of the CMOS Inverter

- Ratioless logic: $V_{OH}$ and $V_{OL}$ are independent of ratio of the transistors
  - $V_{OH} = V_{DD}$
  - $V_{OL} = 0$
- Static power dissipation is zero for both states
- Noise margins can be determined by the VTC
- The switching voltage (when $v_I = v_O$) is defined by
  $$V_M = \frac{r(V_{DD} - |V_p|) + V_n}{r + 1} \quad \text{where} \quad r = \frac{k_p}{k_n} = \frac{\mu_p(W/L)_p}{\mu_n(W/L)_n}$$
  - $V_M$ increases (VTC shifts) with $r$
  - $NM_L$ increases and $NM_H$ decreases as $r$ increases
  - $NM_L$ decreases and $NM_H$ increases as $r$ decreases

\[ \text{NTUEE Electronics III} \]
The Matched Inverter

- A matched inverter has equivalent pull-up and pull-down device with \( k_n = k_p \) and \( V_{tn} = |V_{tp}| = V_1 \)
- The VTC is symmetric
- Determine \( V_{IL} \) from the VTC in Region II:
  \[
  \frac{1}{2}(v_I - V_I)^2 = \left( (V_{DD} - v_I - V_I)(V_{DD} - v_O) - \frac{1}{2}(V_{DD} - V_O)^2 \right)
  \]
  \[v_I - V_I = -(V_{DD} - v_O) - (V_{DD} - v_I - V_I) \frac{dv_O}{dv_I} + (V_{DD} - v_O) \frac{dv_O}{dv_I}\]
  \[V_{IL} = \frac{1}{8}(3V_{DD} + 2V_I)\]
- Determine \( V_{IH} \) from the VTC in Region IV:
  \[ (v_I - V_I)v_O - \frac{1}{2}v_O^2 = \frac{1}{2}(V_{DD} - v_I - V_I)^2 \]
  \[v_O + (v_I - V_I) \frac{dv_O}{dv_I} - v_O \frac{dv_O}{dv_I} = -(V_{DD} - v_I - V_I)\]
  \[V_{IH} = \frac{1}{8}(5V_{DD} - 2V_I)\]
- Noise margins: \( NM_H = NM_L = (3V_{DD} + 2V_I)/8 \)
- Switching voltage: \( V_M = V_{DD}/2 \)
14.3 DYNAMIC OPERATION OF THE CMOS INVERTER

Determining the Propagation Delay

- Evaluated by charging/discharge the output capacitor \( C \) through \( Q_P \) and \( Q_N \)
- Average current method:
  - \( t_{PHL} \):
    \[
    I_{av} = \frac{1}{2} \left[ i_{DN}(E) + i_{DN}(M) \right]
    \]
    \[
    i_{DN}(E) = \frac{1}{2} k_n (V_{DD} - V_m)^2
    \]
    \[
    i_{DN}(M) = k_n \left( (V_{DD} - V_m) \left( \frac{V_{DD}}{2} \right) - \frac{1}{2} \left( \frac{V_{DD}}{2} \right)^2 \right)
    \]
    \[
    t_{PHL} = \frac{CV_{DD}}{2I_{av}} = \frac{\alpha_n C}{k_n V_{DD}}
    \]
    where \( \alpha_n = 2 \left[ \frac{7}{4} - \frac{3V_m}{V_{DD}} + \frac{V_m^2}{V_{DD}^2} \right] \)
  - \( t_{PLH} \):
    \[
    t_{PLH} = \frac{CV_{DD}}{2I_{av}} = \frac{\alpha_p C}{k_p V_{DD}}
    \]
    where \( \alpha_p = 2 \left[ \frac{7}{4} - \frac{3V_{pp}}{V_{DD}} + \frac{V_{pp}^2}{V_{DD}^2} \right] \)
  - Propagation delay: \( t_p = (t_{PHL} + t_{PLH})/2 \)
An alternative approach:
- Modeling the turn-on device as a resistance
- Use RC charge/discharge behavior to evaluate the propagation delay
- The empirical values of the resistors are given by
  \[ R_N = \frac{12.5}{(W/L)_n} \text{k}\Omega \quad \text{and} \quad R_P = \frac{30}{(W/L)_p} \text{k}\Omega \]
- \( t_{PHL} = 0.69 R_N C \)
- \( t_{PLH} = 0.69 R_P C \)
Determining the Equivalent Load Capacitance

- Components accountable for the equivalent load capacitance
  - Transistor parasitic capacitances
  - Wiring capacitance or interconnect capacitance
  - Input capacitance of the following stages

\[
C = 2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2} + C_{g3} + C_{g4} + C_w
\]
Inverter Sizing

- Minimum length permitted by the technology is usually used as the length for all channels
- Device aspect ratio \((W/L)_n\) is usually selected in the range 1 to 1.5
- The selection of \((W/L)_n\) is relative to \((W/L)_n\)
  - Matched inverter by \((W/L)_p : (W/L)_n = \mu_n : \mu_p\)
  - \((W/L)_p = (W/L)_n\): minimum area, small propagation delay
  - \((W/L)_p = 2(W/L)_n\): a frequently used compromise
- Transistor sizing (aspect ratios are increased by a factor of \(S\)) versus propagation delay
  - Load capacitance: \(C = C_{\text{int}} + C_{\text{ext}} = SC_{\text{int0}} + C_{\text{ext}}\)
  - Equivalent resistance: \(R_{eq} = \frac{1}{2} \left( \frac{R_N}{S} + \frac{R_p}{S} \right) = \frac{R_{eq0}}{S}\)
  - Propagation delay: 
    \[ t_p = 0.69 \left( \frac{R_{eq0}}{S} \right) \left( SC_{\text{int0}} + C_{\text{ext}} \right) = 0.69 \left( R_{eq0}C_{\text{int0}} + \frac{1}{S} R_{eq0}C_{\text{ext}} \right) \]

Dynamic Power Dissipation

- Dynamic power dissipation: \(P_d = fCV_{DD}^2\)
- Peak current: \(I_{\text{peak}} = \frac{1}{2} k_n \left( \frac{V_{DD}}{2} - V_m \right)^2\)

\[\begin{align*}
  & \text{I} \quad \text{I}_{\text{peak}} \\
  & V_m \quad 0 \quad \frac{V_{DD}}{2} \\
  & V_{DD} \quad 0 \quad \frac{V_{DD}}{2} \\
  & V_{DD} \quad 0
\end{align*}\]
The PDN can be most directly synthesized by expressing $\overline{Y}$.

The PUN can be most directly synthesized by expressing $Y$.

The PDN can be obtained from the PUN (and vice versa) using duality property.

However, duality of the PDN and PUN is not a necessary condition.
Transistor Sizing

- The (W/L) ratios are chosen for a worst-case gate delay equal to that of the basic inverter.
- The derivation of equivalent (W/L) ratio is based on the equivalent resistance of the transistors.

\[ r_{DS} \propto (W/L)^{-1} \]

- Series Connection \( (W/L)_{eq} = \left[ \frac{1}{(W/L)_1} + \frac{1}{(W/L)_2} + \ldots \right]^{-1} \)
- Parallel Connection \( (W/L)_{eq} = (W/L)_1 + (W/L)_2 + \ldots \)

Effects of Fan-In and Fan-Out

- Each additional input to a CMOS gate requires two additional transistors.
- Increases the chip area and the propagation delay due to excess capacitive loading.
- The number of NAND gate is typically limited to 4.
- Redesign the logic design may be required for a higher number of inputs.
- Advantages of using CMOS logic: static power dissipation, ratioless design, noise margin.
- Disadvantage of using CMOS logic: area, complexity, capacitive loading, propagation delay.
Examples for CMOS Logic Gates

\[ Y = A + B \]

\[ Y = \overline{A} \overline{B} \]

\[ Y = A(B + CD) \]
14.5 IMPLICATIONS OF TECHNOLOGY SCALING

Moore’s Law

- A new technology is developed for every 2~3 years due to cost and speed requirement
- The trend was predicted more than 40 years ago by Gordon Moore
- For every new technology generation:
  - The minimum length is reduced by a factor of 1.414 and the area is reduced by a factor of 2
  - The cost is reduced by half or the circuit complexity is doubled
  - Device scaling generally decreases the parasitics and enhances the operating speed
  - The operating power is reduced
- The current technology node advances into deep-submicron
- Issues in deep-submicron technologies have to be taken into account for circuit designs
### Scaling Implications

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<th>Parameter</th>
<th>Relationship</th>
<th>Scaling Factor</th>
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<tbody>
<tr>
<td>1</td>
<td>$W, L, t_{ox}$</td>
<td>$1/S$</td>
</tr>
<tr>
<td>2</td>
<td>$V_{DD}, V_i$</td>
<td>$1/S$</td>
</tr>
<tr>
<td>3</td>
<td>Area/Device</td>
<td>$WL$</td>
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<tr>
<td>4</td>
<td>$C_{ox}$</td>
<td>$e_{ox}/t_{ox}$</td>
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<tr>
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<td>$k_n^<em>, k_p^</em>$</td>
<td>$\mu_nC_{ox}, \mu_pC_{ox}$</td>
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<tr>
<td>6</td>
<td>$C_{gate}$</td>
<td>$WLC_{ox}$</td>
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<tr>
<td>7</td>
<td>$t_p$ (intrinsic)</td>
<td>$\alpha C/\kappa V_{DD}$</td>
</tr>
<tr>
<td>8</td>
<td>Energy/Switching cycle (intrinsic)</td>
<td>$CV_{DD}^2$</td>
</tr>
<tr>
<td>9</td>
<td>$P_{dyn}$</td>
<td>$f_{max}CV_{DD}^2 = \frac{CV_{DD}^2}{2t_p}$</td>
</tr>
<tr>
<td>10</td>
<td>Power density</td>
<td>$P_{dyn}/\text{Device area}$</td>
</tr>
</tbody>
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Velocity Saturation

- Long-channel devices:
  - Drift velocity: \( v_n = \mu_n E \)
  - Electric field in the channel: \( E = \frac{V_{DS}}{L} \)
- Short-channel devices:
  - Velocity saturates at a critical field \( E_{cr} \) with \( v_{sat} \approx 10^7 \text{ cm/s} \)
  - The \( V_{DS} \) at which velocity saturates is denoted by \( V_{DS_{sat}} \)
  - \( V_{DS_{sat}} = E_{cr}L = \frac{v_{sat}L}{\mu_n} \)
  - \( V_{DS_{sat}} \) is a device parameter

The I-V Characteristics

- Long-channel devices
  - Saturation current: \( i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2 \)
- Short-channel devices
  - For \( V_{GS} - V_t < V_{DS_{sat}} \): same as long-channel devices
  - For \( V_{GS} - V_t > V_{DS_{sat}} \):
    \[
    I_{D_{sat}} = \mu_n C_{ox} \frac{W}{L} \left[ \left( V_{GS} - V_t \right) V_{DS_{sat}} - \frac{1}{2} V_{DS_{sat}}^2 \right] \\
    = WC_{ox} v_{sat} \left( V_{GS} - V_t - \frac{1}{2} V_{DS_{sat}} \right)
    \]
Current Equation for Velocity Saturation

- For $v_{GS} \geq V_t \geq V_{DSsat}$ and $v_{DS} \geq V_{DSsat}$, the drain current is given by
  \[
  i_D = \mu_C \frac{W}{L} V_{DSsat} \left( v_{GS} - V_t - \frac{1}{2} V_{DSsat} \right) \left( 1 + \lambda V_{DS} \right)
  \]
  - The current is reduced from the prediction of a long-channel device
  - The dependence on $v_{GS}$ is more linear rather than quadratic

- Four regions of operation: cutoff, triode, saturation and velocity saturation
- Short-channel PMOS transistors undergo velocity saturation at the same value of $v_{sat}$
- The effects on PMOS are less pronounced due to lower mobility and higher $V_{DSsat}$
Subthreshold Conduction

- The device is not complete off in deep-submicron devices as $v_{GS} < V_t$
- The subthreshold current is exponentially proportional to $v_{GS}$: $i_D = I_s \exp(v_{GS}/nV_T)$
- It is a problem in digital IC design for two reasons:
  - Such current leads to nonzero static power dissipation for CMOS logics
  - May cause undesirable discharge of capacitors in dynamic CMOS logics

The Interconnect

- The width of the interconnect scales down with the CMOS technology
- The metal wire is no longer an ideal short
  - Series parasitic resistance may cause undesirable voltage drop and excess delay
  - Parasitic capacitance to ground may lead to speed degradation and additional dynamic power