CHAPTER 15 CMOS DIGITAL LOGIC CIRCUITS

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15.1 CMOS Logic-Gate Circuits

Switch-Level Transistor Model
- NMOS and PMOS transistors as switches
- Switch on: small resistance $R_{on}$ or $r_{DS}$
- Switch off: open circuit

The CMOS Inverter
- Invert the logic value of the input
- Represented by Boolean expression $Y = \overline{X}$
- When $X = 1$ ($V_X = V_{DD}$)
  $\rightarrow Y = 0$ ($V_Y = 0V$)
- When $X = 0$ ($V_X = 0V$)
  $\rightarrow Y = 1$ ($V_Y = V_{DD}$)
General Structure of CMOS Logic

- NMOS pull-down network (PDN) and PMOS pull-up network (PUN) operated by input variables in a complementary fashion

Alternative Circuit Symbols for MOSFETS in Digital Circuits
Two-Input Logic Gates

- Two-input NOR gate, two-input NAND gate and Exclusive-OR gate

NOR gate

\[ Y = \overline{A + B} \]

NAND gate

\[ Y = \overline{AB} \]

XOR gate
Synthesis Method for PUN and PDN

- The PDN can be directly synthesized by expressing the inverted Boolean function in uncomplemented variables (inverters are needed if complemented variables appear in the expression).

- The PUN can be directly synthesized by expressing the nonverted Boolean function in complemented variables (inverters are needed if uncomplemented variables appear in the expression).

- The PUN can be also obtained from the PDN (and vice versa) using the duality property.

![Diagrams showing synthesis methods for PUN and PDN](image-url)
Examples for CMOS Logic Gates

\[ Y = \overline{AB} \]

\[ Y = \overline{AB} + \overline{AB} \]

\[ Y = \overline{A + B} \]

\[ Y = \overline{A(B + CD)} \]
15.2 Digital Logic Inverters

The Voltage-Transfer Characteristic (VTC)

- The function of the inverter is to invert the logic value of its input signal
- The voltage-transfer characteristic is used to evaluate the quality of inverter operation

- **VTC parameters**
  - $V_{OH}$: output high level
  - $V_{OL}$: output low level
  - $V_{IH}$: the minimum value of input interpreted by the inverter as a logic 1
  - $V_{IL}$: the maximum value of input interpreted by the inverter as a logic 0
  - Transition region: input level between $V_{IL}$ and $V_{IH}$
Noise Margins

- The VTC is generally non-linear
- $V_{IH}$ and $V_{IL}$ are defined as the points at which the slope of the VTC is -1
- Robustness (noise margin at a high level): $NM_H = V_{OH} - V_{IH}$
- Robustness (noise margin at a low level): $NM_L = V_{IL} - V_{OL}$
- Static inverter characteristics for ideal VTC:
  - $V_{OH} = V_{DD}$
  - $V_{OL} = 0$
  - $V_{IH} = V_{IL} = V_{DD}/2$
  - $NM_H = NM_L = V_{DD}/2$

![Ideal VTC Diagram]
Propagation Delay

- $t_{PHL}$: high-to-low propagation delay
- $t_{PLH}$: low-to-high propagation delay
- $t_p$ (propagation delay) = $(t_{PLH} + t_{PHL})/2$
- Maximum switching frequency $f_{\text{max}} = 1/2t_p$
- The output transient of the inverter can be characterized by a $RC$ charge/discharge model

$$v_O(t) = V_\infty - (V_\infty - V_{0+})e^{-t/RC}$$
Inverter Implementation

- Simplest implementation of the inverter with a MOSFET and a load

- Inverter implementation with complementary switches

- Inverter implementation with a double-throw switch
15.3 The CMOS Inverter

Circuit Operation
- A CMOS inverter consists of an n-channel and a p-channel MOSFET
- The n-channel device turns on and the p-channel device turns off as the input level goes high
- The p-channel device turns on and the n-channel device turns off as the input level goes low
- The turn-on device is modeled by a resistance: \( r_{DSN} = \left[ k_n (W/L)_n (V_{DD} - V_{th}) \right]^{-1} \) and \( r_{DSP} = \left[ k_p (W/L)_p (V_{DD} - |V_{th}|) \right]^{-1} \)
- \( V_{OH} = V_{DD} \) and \( V_{OL} = 0 \) for any CMOS inverter
The transistors go through five different operation regions as the input goes from 0 to $V_{DD}$

- **Region I:** ($Q_N$ off; $Q_P$ tri.)
  \[ i_{DN} = 0 = i_{DP} \]

- **Region II:** ($Q_N$ sat.; $Q_P$ tri.)
  \[ i_{DN} = \frac{1}{2} k_n (v_I - V_{in})^2 = i_{DP} = k_p \left[ (V_{DD} - v_I - |V_{in}|)(V_{DD} - v_O) - \frac{1}{2} (V_{DD} - v_O)^2 \right] \]

- **Region III:** ($Q_N$ sat; $Q_P$ sat)
  \[ i_{DN} = \frac{1}{2} k_n (v_I - V_{in})^2 = i_{DP} = \frac{1}{2} k_p (V_{DD} - v_I - |V_{in}|)^2 \]

- **Region IV:** ($Q_N$ tri.; $Q_P$ sat.)
  \[ i_{DN} = k_n \left[ (v_I - V_{in})v_O - \frac{1}{2} v_O^2 \right] = i_{DP} = \frac{1}{2} k_p (V_{DD} - v_I - |V_{in}|)^2 \]

- **Region V:** ($Q_N$ tri.; $Q_P$ off)
  \[ i_{DN} = i_{DP} (= 0) \]
Static Characteristics of the CMOS Inverter

- Ratioless logic: $V_{OH}$ and $V_{OL}$ are independent of ratio of the transistors
  - $V_{OH} = V_{DD}$
  - $V_{OL} = 0$
- Static power dissipation is zero for both states
- Noise margins can be determined by the VTC
- The switching voltage (when $v_i = v_O$) is defined by
  $$V_M = \frac{r(V_{DD} - |V_{tp}|) + V_{in}}{r+1}$$
  where
  $$r = \sqrt{\frac{k_p}{k_n}} = \sqrt{\frac{\mu_p(W/L)_p}{\mu_n(W/L)_n}}$$
  - $V_M$ increases with $r$ (not a strong function)
  - $NM_L$ increases and $NM_H$ decreases as $r$ increases
  - $NM_L$ decreases and $NM_H$ increases as $r$ decreases
The Matched Inverter

- A matched inverter has equivalent pull-up and pull-down device with $k_n = k_p$ and $V_{tn} = |V_{tp}| = V_t$
- The VTC is symmetric
- Determine $V_{IL}$ from the VTC in Region II:
  \[
  \frac{1}{2}(v_i - V_i)^2 = (V_{DD} - v_i - V_i)(V_{DD} - V_o) - \frac{1}{2}(V_{DD} - v_o)^2
  \]
  \[
  v_i - V_i = -(V_{DD} - v_o) - (V_{DD} - v_i - V_i) \frac{dv_o}{dv_i} + (V_{DD} - v_o) \frac{dv_o}{dv_i}
  \]
  \[
  V_{IL} = \frac{1}{8}(3V_{DD} + 2V_i)
  \]
- Determine $V_{IH}$ from the VTC in Region IV:
  \[
  (v_i - V_i)v_o - \frac{1}{2}v_o^2 = \frac{1}{2}(V_{DD} - v_i - V_i)^2
  \]
  \[
  v_o + (v_i - V_i) \frac{dv_o}{dv_i} - v_o \frac{dv_o}{dv_i} = -(V_{DD} - v_i - V_i)
  \]
  \[
  V_{IH} = \frac{1}{8}(5V_{DD} - 2V_i)
  \]
- Noise margins: $NM_H = NM_L = (3V_{DD} + 2V_i)/8$
- Switching voltage: $V_M = V_{DD}/2$

\[\text{NTUEE  Electronics III} \quad 15-14\]
15.4 Dynamic Operation of the CMOS Inverter

Determining the Propagation Delay

- Evaluated by charging/discharge the output capacitor $C$ through $Q_P$ and $Q_N$
- Average current method:

  - $t_{PHL}$:
    \[
    I_{av} = \frac{1}{2} \left[ i_{DN}(E) + i_{DN}(M) \right]
    \]
    \[
    i_{DN}(E) = \frac{1}{2} k_n (V_{DD} - V_{tn})^2
    \]
    \[
    i_{DN}(M) = k_n \left[ (V_{DD} - V_{tn}) \left( \frac{V_{DD}}{2} - \frac{1}{2} \left( \frac{V_{DD}}{2} \right)^2 \right) \right]
    \]
    \[
    t_{PHL} = \frac{CV_{DD}}{2I_{av}} = \frac{\alpha_n C}{k_n V_{DD}}
    \]
    where $\alpha_n = 2 / \left[ \frac{7}{4} - \frac{3}{2} \left( \frac{V_{tn}}{V_{DD}} \right)^2 \right]$  

  - $t_{PLH}$:
    \[
    t_{PLH} = \frac{CV_{DD}}{2I_{av}} = \frac{\alpha_p C}{k_p V_{DD}}
    \]
    where $\alpha_p = 2 / \left[ \frac{7}{4} - \frac{3}{2} \left( \frac{V_{tp}}{V_{DD}} \right)^2 \right]$  

- Propagation delay: $t_P = (t_{PHL} + t_{PLH}) / 2$
An alternative approach:
- Modeling the turn-on device as a resistance.
- Use RC charge/discharge behavior to evaluate the propagation delay.
- The empirical values of the resistors are given by
  \[ R_N = \frac{12.5}{(W/L)_n} (k\Omega) \quad \text{and} \quad R_P = \frac{30}{(W/L)_p} (k\Omega) \]
- \( t_{PHL} = 0.69R_NC \) and \( t_{PLH} = 0.69R_PC \)
- Step function at input may underestimate propagation delay \( t_{PHL} \approx R_NC \) and \( t_{PLH} \approx R_PC \)
Determining the Equivalent Load Capacitance

- Components accountable for the equivalent load capacitance
  - Transistor parasitic capacitances from $Q_1$ and $Q_2$ (intrinsic component)
  - Input capacitance of the following stages (extrinsic component)
  - Wiring capacitance or interconnect capacitance (extrinsic component)

\[
C = (2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2}) + (C_{g3} + C_{g4} + C_w) = C_{int} + C_{ext}
\]
15.5 Transistor Sizing

Inverter Sizing

- Minimum length permitted by the technology is usually used as the length for all channels
- Device aspect ratio \((W/L)_n\) is usually selected in the range 1 to 1.5
- The selection of \((W/L)_p\) is relative to \((W/L)_n\)
  - Matched inverter by \((W/L)_p : (W/L)_n = \mu_n : \mu_p\)
  - \((W/L)_p = (W/L)_n\): minimum area, small propagation delay
  - \((W/L)_p = 2(W/L)_n\): a frequently used compromise
- Transistor sizing (aspect ratios are increased by a factor of \(S\)) versus propagation delay
  - Load capacitance: \(C = C_{int} + C_{ext} = SC_{int0} + C_{ext}\)
  - Equivalent resistance: \(R_{eq} = \frac{1}{2} \left( \frac{R_N}{S} + \frac{R_p}{S} \right) = \frac{R_{eq0}}{S}\)
  - Propagation delay: \(t_p = 0.69 \left( \frac{R_{eq0}}{S} \right)(SC_{int0} + C_{ext}) = 0.69 \left( R_{eq0}C_{int0} + \frac{1}{S} R_{eq0}C_{ext} \right)\)

- The propagation decreases as \(S\) increases for cases where \(C_{ext}\) dominates
- The propagation is nearly independent of the transistor sizing \((S)\) for cases where \(C_{int}\) dominates
Transistor Sizing

- The \((W/L)\) ratios are chosen for a worst-case gate delay equal to that of the basic inverter (assuming \(C\) is constant)
- The derivation of equivalent \((W/L)\) ratio is based on the equivalent resistance of the transistors

\[
r_{DS} \propto (W/L)^{-1}
\]

\[
(W/L)_{eq} = \left[ \frac{1}{(W/L)_1} + \frac{1}{(W/L)_2} + \ldots \right]^{-1}
\]

Effects of Fan-In and Fan-Out

- Each additional input to a CMOS gate requires two additional transistors
- Increases the chip area and the propagation delay due to excess capacitive loading
- The number of NAND gate is typically limited to 4
- Redesign the logic design may be required for a higher number of inputs
- Advantages of using CMOS logic: static power dissipation, ratioless design, noise margin
- Disadvantage of using CMOS logic: area, complexity, capacitive loading, propagation delay
Driving a Large Capacitance

- A large capacitive load drastically increases the propagation delay
- Use a large inverter to drive the load could alleviate the propagation delay
- The input capacitance increases accordingly equivalently shifting the burden forward
- Chain of scaled inverters in cascade to alleviate the problem with large capacitive load
15. 6 Power Dissipation

Power Dissipation

- Static power dissipation: power dissipated when the inverter stays in logic 0 or logic 1
- Dynamic power dissipation: power dissipated as the output is switching
  - 0.5C(V_{DD})^2 is dissipated in the PUN in each cycle
  - 0.5C(V_{DD})^2 is dissipated in the PDN in each cycle
  - Dynamic power dissipation: \( P_D = f C(V_{DD})^2 \)

- Another component of power dissipation during switching results from the current conduction through \( Q_P \) and \( Q_N \) and the peak current for a matched inverter is given by

\[
I_{\text{peak}} = \frac{1}{2} k_n \left( \frac{V_{DD}}{2} - V_{in} \right)^2
\]

Power-Delay Product and Energy-Delay Product

- Power and delay are often in conflict for inverter operation
- Power-delay product is a figure-of-merit for comparing logic-circuit technologies or families
- Power-delay product is defined as \( PDP = P_D t_P = CV_{DD}^2 / 2 \)
- Energy-delay product (energy per transition) is defined as \( EDP = CV_{DD}^2 t_P / 2 \)