CHAPTER 16 ADVANCED MOS AND BIPOLAR LOGIC CIRCUITS

Chapter Outline

16.1 Implications of Technology Scaling
16.2 Digital IC Technology, Logic-Circuit Family and Design Methodologies
16.3 Pseudo-NMOS Logic Circuits
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16.1 Implications of Technology Scaling

Moore’s Law
- A new technology is developed for every 2~3 years due to cost and speed requirement
- The trend was predicted more than 40 years ago by Gordon Moore
- For every new technology generation:
  - The minimum length is reduced by a factor of $1.414$ and the area is reduced by a factor of 2
  - The cost is reduced by half or the circuit complexity is doubled
  - Device scaling generally decreases the parasitics and enhances the operating speed
  - The operating power is reduced
- The current technology node advances into deep-submicron
- Issues in deep-submicron technologies have to be taken into account for circuit designs
Scaling Implications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Relationship</th>
<th>Scaling Factor</th>
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<td>1</td>
<td>$W, L, t_{ox}$</td>
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<td>$V_{DD}, V_i$</td>
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<td>Area/Device</td>
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<td>$e_{ox}/t_{ox}$</td>
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<td>$S$</td>
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<tr>
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<td>$k'_n, k'_p$</td>
<td>$\mu_n C_{ox}, \mu_p C_{ox}$</td>
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<tr>
<td></td>
<td>$S$</td>
<td></td>
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<td>6</td>
<td>$C_{gate}$</td>
<td>$WLC_{ox}$</td>
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<td>$1/S$</td>
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<td>7</td>
<td>$t_p$ (intrinsic)</td>
<td>$aC/k'V_{DD}$</td>
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<td>8</td>
<td>Energy/Switching cycle (intrinsic)</td>
<td>$CV_{DD}^2$</td>
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<td>$1/S^3$</td>
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<td>$f_{max} CV_{DD}^2 = \frac{CV_{DD}^2}{2t_p}$</td>
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<td>$1/S^2$</td>
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<td>10</td>
<td>Power density</td>
<td>$P_{dyn}$ /Device area</td>
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<tr>
<td></td>
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Velocity Saturation

- Long-channel devices:
  - Drift velocity: \( v_n = \mu_n E \)
  - Electric field in the channel: \( E = \frac{v_{DS}}{L} \)

- Short-channel devices:
  - Velocity saturates at a critical field \( E_{cr} \) with \( v_{sat} \approx 107 \text{ cm/s} \)
  - The \( v_{DS} \) at which velocity saturates is denoted by \( V_{DSSat} \)
  - \( V_{DSSat} = E_{cr} L = \frac{v_{sat} L}{\mu_n} \)
  - \( V_{DSSat} \) is a device parameter

The I-V Characteristics

- Long-channel devices
  - Saturation current \( i_{dp} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2 \)

- Short-channel devices
  - For \( V_{GS} - V_t < V_{DSSat} \): same as long-channel devices
  - For \( V_{GS} - V_t > V_{DSSat} \):
    \[
    I_{Dsat} = \mu_n C_{ox} \frac{W}{L} \left( (V_{GS} - V_t)V_{DSSat} - \frac{1}{2} V_{DSSat}^2 \right) \\
    = WC_{ox} v_{sat} \left( V_{GS} - V_t - \frac{1}{2} V_{DSSat} \right)
    \]
Current Equation for Velocity Saturation

- For $v_{GS} - V_t \geq V_{DSsat}$ and $v_{DS} \geq V_{DSsat}$, the drain current is given by
  $$i_D = \mu_n C_{ox} \frac{W}{L} V_{DSsat} \left( v_{GS} - V_t - \frac{1}{2} V_{DSsat} \right) \left(1 + \lambda V_{DS} \right)$$

- The current is reduced from the predication of a long-channel device
- The dependence on $v_{GS}$ is more linear rather than quadratic

- Four regions of operation: cutoff, triode, saturation and velocity saturation
- Short-channel PMOS transistors undergo velocity saturation at the same value of $v_{sat}$
- The effects on PMOS are less pronounced due to lower mobility and higher $V_{DSsat}$
Subthreshold Conduction

- The device is not complete off in deep-submicron devices as \( v_{GS} < V_t \)
- The subthreshold current is exponentially proportional to \( v_{GS} \): \( i_D = I_s \exp(v_{GS}/nV_T) \)
- It is a problem in digital IC design for two reasons:
  - Such current leads to nonzero static power dissipation for CMOS logics
  - May cause undesirable discharge of capacitors in dynamic CMOS logics

The Interconnect

- The width of the interconnect scales down with the CMOS technology
- The metal wire is no longer an ideal short
  - Series parasitic resistance may cause undesirable voltage drop and excess delay
  - Parasitic capacitance to ground may lead to speed degradation and additional dynamic power
16.2 Digital IC Technology, Logic-Circuit Families, and Design Methodologies

Logic-Circuit Families

- Classified by fabrication technology: CMOS, Bipolar, BiCMOS, GaAs
- Most widely logic-circuit technology is CMOS
- Various logic families are implemented in CMOS technology

Digital IC technologies and logic-circuit families

- CMOS
  - Complementary CMOS
  - Pseudo-NMOS
  - Dynamic logic
- Bipolar
- BiCMOS
- GaAs
- TTL
- ECL

Styles for Digital System Design

- Assemble the system using standard IC packages of various levels of complexity
- Application specific IC (ASIC) with customized digital design when large volume is required
- Semicustom design:
  - Gate-array (unconnected logic gates) with final customized metallization step
  - Field-programmable gate array (FPGA) can be programmed by the user
16.3 The Pseudo-NMOS Logic Circuits

The Voltage-Transfer Characteristic (VTC)

- The function of the inverter is to invert the logic value of its input signal
- The voltage-transfer characteristic is used to evaluate the quality of inverter operation

- VTC parameters
  - $V_{OH}$: output high level
  - $V_{OL}$: output low level
  - $V_{IH}$: the minimum value of input interpreted by the inverter as a logic 1
  - $V_{IL}$: the maximum value of input interpreted by the inverter as a logic 0
  - Transition region: input level between $V_{IL}$ and $V_{IH}$
NMOS Inverter Circuits

- A simple inverter circuit is composed of a NMOS and a load
- The load can be realized by a resistor or another NMOS device

Resistive Load NMOS Inverter

Enhancement Load NMOS Inverter

Depletion Load NMOS Inverter

Pseudo-NMOS Inverters

- Use a PMOS transistor as the load
- Does not suffer from body effect
- Directly compatible with complementary CMOS circuits
- Area and delay penalties arising from the fan-in in complementary CMOS gate is reduces
Static Characteristics

- Load curve represents a much lower saturation current
- $k_n$ is usually greater than $k_p$ by a factor of 4 to 10
- A ratioed type logic with $r = k_n/k_p$
- The logic is typically operated in two extremely cases:
  - $v_i = 0$: $v_O = V_{OH} = V_{DD}$
  - $v_i = V_{DD}$: $v_O = V_{OL} > 0$ (nonzero $V_{OL}$ for pseudo-NMOS)
- The VTC can be derived based on $i_{DN}$ and $i_{DP}$:
  \[
  i_{DN} = \frac{1}{2} k_n (v_i - V_t)^2 \quad \text{for } v_O \geq v_i - V_t \quad \text{(saturation)}
  \]
  \[
  i_{DN} = k_n \left[ (v_i - V_t) v_O - \frac{1}{2} v_O^2 \right] \quad \text{for } v_O \leq v_i - V_t \quad \text{(triode)}
  \]
  \[
  i_{DP} = \frac{1}{2} k_p (V_{DD} - V_t)^2 \quad \text{for } v_O \leq V_t \quad \text{(saturation)}
  \]
  \[
  i_{DP} = k_p \left[ (V_{DD} - V_t)(V_{DD} - v_O) - \frac{1}{2} (V_{DD} - v_O)^2 \right] \quad \text{for } v_O \geq V_t \quad \text{(triode)}
  \]
Derivation of the VTC

- Assume \( V_{tn} = |V_{tp}| = V_t \) for the derivations
- Region I (Segment AB):
  \[ v_O = V_{OH} = V_{DD} \]
- Region II (Segment BC):
  \[ v_O = V_i + \sqrt{(V_{DD} - V_t)^2 - r(v_i - V_t)^2} \]
- Region III (Segment CD):
  \[ r\left[ (v_i - V_t)v_O - \frac{1}{2} v_O^2 \right] = \left[ (V_{DD} - V_t)(V_{DD} - v_O) - \frac{1}{2}(V_{DD} - V_t)^2 \right] \]
- Region IV (Segment DE):
  \[ v_O = (v_i - V_t) - \sqrt{(v_i - V_t)^2 - \frac{1}{r}(V_{DD} - V_t)^2} \]
- Static Characteristics:
  \[
  \begin{align*}
  V_{OH} &= V_{DD} \\
  V_{OL} &= (V_{DD} - V_t)(1 - \sqrt{1 - k_p / k_n}) \\
  V_{IH} &= V_i + \frac{2}{\sqrt{3k_n / k_p}}(V_{DD} - V_t) \\
  V_{IL} &= V_i + \frac{V_{DD} - V_t}{\sqrt{(k_n / k_p)(k_n / k_p + 1)}} \\
  N M_H &= V_{OH} - V_{IH} \\
  N M_L &= V_{IL} - V_{OL} \\
  V_M &= V_i + \frac{V_{DD} - V_t}{\sqrt{k_n / k_p + 1}}
  \end{align*}
  \]

<table>
<thead>
<tr>
<th>Region</th>
<th>VTC Segment</th>
<th>( Q_N )</th>
<th>( Q_P )</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>AB</td>
<td>Cut-off</td>
<td>Triode</td>
<td>( v_I &lt; V_t )</td>
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<tr>
<td>II</td>
<td>BC</td>
<td>Saturation</td>
<td>Triode</td>
<td>( v_O &gt; v_I - V_t )</td>
</tr>
<tr>
<td>III</td>
<td>CD</td>
<td>Triode</td>
<td>Triode</td>
<td>( V_t &lt; v_O &lt; v_I - V_t )</td>
</tr>
<tr>
<td>IV</td>
<td>DE</td>
<td>Triode</td>
<td>Saturation</td>
<td>( v_O &lt; V_t )</td>
</tr>
</tbody>
</table>
Dynamic Operation

- Determine $t_{PLH}$:
  - The analysis is identical to the CMOS inverter and the output capacitance $C$ is charged by PMOS
  - $t_{PLH} = \frac{\alpha_p C}{k_p V_{DD}}$ where $\alpha_p = 2 \left[ \frac{7}{4} - \frac{3 (V_t / V_{DD}) + (V_t / V_{DD})^2}{4} \right]$

- Determine $t_{PHL}$:
  - The discharge current is $i_{DN} - i_{DP}$ while $i_{DP}$ is typically negligible as $r$ is large
  - $t_{PHL} = \frac{\alpha_n C}{k_n V_{DD}}$ where $\alpha_n = 2 \left[ 1 + \frac{3}{4} \left( 1 - \frac{1}{r} \right) - \left( 3 - \frac{1}{r} \right) \frac{V_t}{V_{DD}} + \left( \frac{V_t}{V_{DD}} \right)^2 \right]$

- $\alpha_n \cong \alpha_p$ for a large value of $r$ and $t_{PHL}$ is much larger than $t_{PLH}$

Design of Pseudo-NMOS Inverter

- Determine ratio $r = k_n / k_p$
  - The larger the value of $r$, the lower $V_{OL}$ is and the wider the noise margins are
  - A larger $r$ increases the asymmetry in the dynamic response
  - Usually, $r$ is selected in the range of 4 to 10

- Determine $(W/L)_n$ and $(W/L)_p$
  - A smaller $(W/L)$ to keep the gate area small and thus obtain a small value for $C$
  - A smaller $(W/L)$ to keeps $I_{sat}$ of $Q_p$ and static power dissipation low
  - Larger $(W/L)$ ratios in order to obtain low $t_p$ and thus fast response
Gate Circuits
- Identical to PDN of CMOS gate except for the load device
- The ratio $r$ determines all the breakpoints of the VTC
  - The larger the value of $r$, the lower $V_{OL}$ is and the wider the noise margins are
  - A larger $r$ increases asymmetry in the dynamic response
  - Usually, $r$ is selected in the range of 4 to 10
- Determine $(W/L)_n$ and $(W/L)_p$
  - Smaller $(W/L)$ for small area and capacitance
  - Smaller $(W/L)$ for lower $I_{sat}$ of $Q_p$ and static power dissipation
  - Larger $(W/L)$ ratios in order to obtain low $t_P$ and thus fast response

Concluding Remarks
- In pseudo-NMOS, NOR gates are preferred over NAND gates in order to use minimum-size devices
- Pseudo-NMOS is particularly suited for applications in which output remains high most of the time
  - Static power dissipation can be reasonably low
  - The output transitions that matter would presumably be high-to-low ones where the propagation delay can be made as short as necessary
16.4 Pass-Transistor Logic Circuits

Design of Pass-Transistor Logic (PTL) Circuits

- Using series and parallel combinations of switches
- The switches are controlled by input logic variables to connect the input and output nodes
- Can be implemented by a single NMOS transistor or CMOS transmission gate
- Every circuit node has at all times a low-resistance path to $V_{DD}$ or ground

\[ Y = ABC \]

\[ Y = A(B + C) \]
Operation with NMOS Transistor as the Switch

- Pass-transistor with output high ("poor 1")
  - The output node refers to the source terminal of the NMOS
  - During the charging process, $Q$ is in saturation
  - $V_t$ increases with $v_O$ due to body effect, resulting in a large $t_{PLH}$
  - $V_{OH} = V_{DD} - V_t$, reducing the gate noise immunity

- Pass-transistor with output low ("good 0")
  - The input node refers to the source terminal of the NMOS
  - No body effect
  - The output node can be discharged completely $\rightarrow V_{OL} = 0$
Restoring the Output Level

- The circuit-based approach by adding a feedback loop with $Q_R$
  - The PMOS $Q_R$ turns on by $v_{O2} (= \text{"0"})$ to restore the signal loss at $v_{O1} = \text{"1"}$
  - The PMOS $Q_R$ is turn off by $v_{O2} (= \text{"1"})$ when $v_{O1} = \text{"0"}$
  - Operation is more involved than it appears due to the positive feedback
  - $Q_R$ has to be a “weak PMOS transistor” in order not to play a major role in the circuit operation

- The alternative approach by process technology
  - The signal loss is due to the threshold voltage of the NMOS devices
  - Threshold adjustment by ion implantation to make zero-threshold devices
  - Subthreshold conduction becomes significant for zero-threshold devices
The Use of CMOS Transmission Gates as Switches

- PMOS and NMOS are in parallel with complementary control signal
- Both NMOS and PMOS provide charging/discharging current
- Good logic level with $V_{OH} = V_{DD}$ and $V_{OL} = 0$
- The complexity, silicon area and load capacitance are increased
- Body effect has to be taken into account to evaluate $i_{DN}$ and $i_{DP}$
The Equivalent Resistance of the Transmission Gate

- The equivalent resistance of $Q_N$:
  - For $v_O \leq V_{DD} - V_{tn}$:
    $$i_{DN} = \frac{1}{2} k_n (V_{DD} - V_{tn} - v_O)^2 \quad \text{and} \quad R_{Neq} = \frac{V_{DD} - v_O}{\frac{1}{2} k_n (V_{DD} - V_{tn} - v_O)^2}$$
  - For $v_O > V_{DD} - V_{tn}$:
    $$i_{DN} = 0 \quad \text{and} \quad R_{Neq} = \infty$$

- The equivalent resistance of $Q_P$:
  - For $v_O \leq |V_{tp}|$:
    $$i_{DP} = \frac{1}{2} k_p (V_{DD} - |V_{tp}|)^2 \quad \text{and} \quad R_{Peq} = \frac{V_{DD} - v_O}{\frac{1}{2} k_p (V_{DD} - |V_{tp}|)^2}$$
  - For $v_O > |V_{tp}|$:
    $$i_{DP} = k_p \left[ (V_{DD} - |V_{tp}|)(V_{DD} - v_O) - \frac{1}{2} (V_{DD} - v_O)^2 \right] \quad \text{and} \quad R_{Peq} = \frac{V_{DD} - v_O}{k_p \left[ (V_{DD} - |V_{tp}|)(V_{DD} - v_O) - \frac{1}{2} (V_{DD} - v_O)^2 \right]}$$

- Empirical formula for the equivalent resistance:
  $$R_{TG} = \frac{12.5}{(W/L)_n} (k\Omega)$$
Calculation of Propagation Delay in the Signal Path

- The signal path containing multiple transmission gates can be modeled by resistors and capacitors

- The model is in a form of an RC ladder network

- The propagation delay is given by Elmore delay formula as
  \[ t_p = 0.69\left[(C_{out1} + C_{TG1})R_{P1} + (C_{TG2} + C_{in2})(R_{P1} + R_{TG})\right] \]

- Elmore delay formula is given by
  \[ t_p = 0.69\left[C_1R_1 + C_2(R_1 + R_2) + C_3(R_1 + R_2 + R_3) + ... \right] \]
Pass-Transistor Logic Circuit Examples

Final Remarks

- Advantages of CMOS transmission gate over pass-transistor logic with NMOS devices
  - Logic level: good “1” and “0”
  - No level restoring technique needed

- Disadvantages of CMOS transmission gate over pass-transistor logic with NMOS devices
  - Silicon area and complexity: an additional input requires one NMOS and one PMOS devices
  - Complementary control signal required
  - Propagation delay: more capacitive loading from the MOSFETs
16.5 Dynamic MOS Logic Circuits

Principle of Dynamic Logic Circuits

- Rely on the storage of signal voltage on parasitic capacitances at certain circuit nodes
- The circuits need to be periodically refreshed
- Maintain the low device count of pseudo-NMOS while reducing the static power dissipation to zero

Operation of Dynamic Logic Circuits

- Precharge phase: $Q_p$ on and $Q_e$ off → charge the output node to $V_{DD}$
- Evaluation phase: $Q_p$ off and $Q_e$ on → selectively discharge the output node through PDN

![Diagram of Dynamic MOS Logic Circuits]
Nonideal Effects

- **Noise margin:**
  - Since \( V_{IL} \approx V_{IH} \approx V_{tn} \), the resulting noise margins are \( NM_L \approx V_{tn} \) and \( NM_H \approx V_{DD} - V_{tn} \)
  - Asymmetric noise immunity (poor \( NM_L \))

- **Output voltage decay due to leakage effects:**
  - When PDN is off, leakage current will slowly discharge the output node
  - The leakage is from the reversed-biased junctions and possibly the subthreshold conduction

- **Charge sharing:**
  - Some of the internal nodes in PDN will share the charge in \( C_L \) even the PDN path is off
  - Can be solved by adding a permanently turn-on transistor \( Q_L \) at the cost of static power dissipation
Domino CMOS Logic

- Problem with cascading dynamic logic gates: errors caused by undesirable premature discharge

- Domino CMOS logic:
  - A dynamic logic with a static CMOS inverter connected to its output
  - The output to the following stages is 0 during the precharge phase
  - Can alleviate the premature discharge problem
A cascade of Domino CMOS logic:
- Each stage has to wait for the rising edge from the preceding stage
- The rising edge propagates through a cascade of gates

Concluding Remarks
- Advantages of Domino logic: small area, high-speed operation, and zero static power dissipation
- Disadvantages of Domino logic:
  - Asymmetric noise margin
  - Leakage issue
  - Charge sharing
  - Dead time: unavailability of output during precharge phase
16.6 Bipolar and BiCMOS Logic Circuits

**Basic Principle**

- High speed is achieved by operating all transistor out of saturation to avoid storage time delays
- By keeping the logic signal swings relatively small (~0.8V) to reduce charging/discharging time
- One of the inputs is connected to a reference voltage $V_R$
  - When $v_1$ is greater than $V_R$ by about $4V_T \rightarrow v_{O1} = V_{CC} - I \times R_C$ and $v_{O2} = V_{CC}$
  - When $v_1$ is smaller than $V_R$ by about $4V_T \rightarrow v_{O1} = V_{CC}$ and $v_{O2} = V_{CC} - I \times R_C$.

- Important features of ECL:
  - The differential nature of the circuit makes it less susceptible to picked-up noise
  - Current drawn from the power supply remains constant during switching $\rightarrow$ no current spikes
  - The output signal levels are both referenced to $V_{CC}$ and can be made stable with $V_{CC} = 0V$
  - Some means are needed to make the output signal levels compatible with those at the input
  - The availability of complementary output considerably simplifies logic design with ECL

![ECL Circuit Diagram]
The Basic Gate Circuit

- Bias network:
  - The network generates a reference voltage $V_R$ of $-1.32V$ at room temperature
  - $V_R$ is made to change with $T$ in a predetermined manner so as to keep noise margins constant
  - $V_R$ is also made relatively insensitive to variations in the power supply voltage $V_{EE}$

![Diagram of the basic gate circuit]

$R_{C1} = 220 \, \Omega$

$R_{C2} = 245 \, \Omega$

$R_1 = 907 \, \Omega$

$R_a = 50 \, k\Omega$

$R_b = 50 \, k\Omega$

$R_e = 779 \, \Omega$

$V_{CC2}$

$V_{EE}$

$R_3 = 6.1 \, k\Omega$

$R_5 = 4.98 \, k\Omega$

$D_1$

$D_2$

$Q_1$

$Q_2$

$Q_3$

$V_{CC1}$

$A$

$B$

$V_R$

$-V_{EE} (-5.2 \, V)$

Differential input amplifier

Temperature- and voltage-compensated bias network

Emitter-follower outputs

OR Output

NOR Output

NTUEE  Electronics III  16-26
Differential input stage:
- Paralleling input transistors ($Q_A$ and $Q_B$) are used to implement OR and NOR functions
- Current in $R_E$ remains approximately constant over the normal range of operation
- Resistors to connect each input terminal to negative supply → can leave unused inputs open

Emitter-follower output stage:
- On-chip loads are not included as the gate drives a transmission line terminated at the other end in most of high-speed logic
- Emitter followers shift the level by one $V_{BE}$ drop → the shifted levels are centered around $V_R$
- Provide low output resistance and large current driving capability
- Separate power-supply prevents coupling of power-supply spikes from output to gate circuit

**ECL Families**
- ECL 100K: $t_p \approx 0.75$ns and $P_D \approx 40$mW → $PDP = 30$pJ
- ECL 10K: $t_p \approx 2$ns and $P_D \approx 25$mW → $PDP = 50$pJ
- A variant of ECL (current-mode logic) has become popular in VLSI applications
Voltage Transfer Characteristics

- Definition of unity-gain: $Q_A$ (or $Q_R$) is conducting 1% (or 99%) of $I_E$
- Assuming $V_{BE} = 0.75V$ at a emitter current of 1 mA for an ECL transistor

**OR Transfer Curve**

\[
\begin{align*}
V_{t} &= -2 V \\
V_{EE} &= -5.2 V \\
V_{t} &= -2 V
\end{align*}
\]

\[
I_E\bigg|_{Q_R} = 99 \rightarrow V_{BE}\bigg|_{Q_e} - V_{BE}\bigg|_{Q_A} = V_T \ln 99 = 115mV
\]

\[
V_{IL} = -1.32 - 0.115 = -1.435V
\]

\[
V_{IH} = -1.32 + 0.115 = -1.205V
\]

for $v_i < V_{IL}$: $I_E = \frac{V_R - V_{BE}\bigg|_{Q_e} + V_{EE}}{R_E} = \frac{-1.32 - 0.75 + 5.2}{0.779} = 4mA$

\[
V_{OL} = -4 \times 0.245 - 0.75 = -1.73V
\]

\[
V_{OH} = -0.88V
\]

\[
NM_L = V_{IL} - V_{OL} = -1.435 - (-1.77) = 0.335V
\]

\[
NM_H = V_{OH} - V_{IH} = -0.88 - (-1.205) = 0.325V
\]
NOR Transfer Curve

\[ I_E \mid_{Q_R} = 99 \rightarrow V_{BE} \mid_{Q_R} - V_{BE} \mid_{Q_A} = V_T \ln 99 = 115mV \]

\[ V_{IL} = -1.32 - 0.115 = -1.435V \]

\[ V_{IH} = -1.32 + 0.115 = -1.205V \]

for \( v_I < V_{IL} \): \( V_{OH} = -0.88V \)

for \( v_I = V_{IH} \):

\[ I_E = \frac{V_{IH} - V_{BE} \mid_{Q_A} + V_{EE}}{R_E} = \frac{-1.205 - 0.75 + 5.2}{0.779} = 4.17mA \]

\[ v_O = -4.17 \times 0.22 - 0.75 = -1.667V \]

for \( v_I = V_{OH} \):

\[ I_E = \frac{V_{OH} - V_{BE} \mid_{Q_A} + V_{EE}}{R_E} = \frac{-0.88 - 0.75 + 5.2}{0.779} = 4.58mA \]

\[ V_{OL} = -4.58 \times 0.22 - 0.75 = -1.758V \]

\[ NM_L = V_{IL} - V_{OL} = -1.435 - (-1.758) = 0.323V \]

\[ NM_H = V_{OH} - V_{IH} = -0.88 - (-1.205) = 0.325V \]
Manufacturers’ Specifications

- $V_{IL_{\text{max}}} = -1.475 \text{ V}$  
  $V_{IH_{\text{min}}} = -1.105 \text{ V}$
- $V_{OL_{\text{max}}} = -1.630 \text{ V}$  
  $V_{OH_{\text{min}}} = -0.980 \text{ V}$

Fan-Out

- $I_{IL} = (-1.77+5.2)/50 = 69 \text{ mA}$  
  $I_{IH} = (-0.88+5.2)/50 + 4/101 = 126 \text{ mA}$
- Input currents are small and output resistance is small $\rightarrow$ fan-out of ECL not limited by logic-level
- The fan-out is limited by considerations of circuit speed

Operating Speed

- Speed is measured by the delay of its basic gate and by the rise and fall times of output waveforms
- Using emitter follower as the output stage, the ECL gate exhibit shorter rise time than its fall time

Signal Transmission

- ECL is particularly sensitive to ringing because the signal levels are so small
- One solution is to keep the wires very “short” with respect to the signal rise/fall time
  $\rightarrow$ the reflections return while the input is still rising/falling
- If greater lengths are needed, then transmission lines must be used
  $\rightarrow$ the reflection is suppressed with proper termination
Power Dissipation
- Gate power dissipation of unterminated ECL remain relatively constant independent of the logic state
- No current spikes are introduced on the supply line
- The need for supply-line bypassing in ECL is not as great as in TTL

Thermal Effects
- The reference voltage $V_R$ is $-1.32V$ at room temperature
- $V_R$ is made to change with $T$ in a predetermined manner so as to keep the noise margins almost constant
- A demonstration of the high degree of design optimization of this gate circuit

Wired-OR Capability
- The emitter follower output stage of the ECL family allows wired-OR for logic design
- The OR function is implemented by wiring the output of several gates in parallel
The BiCMOS Circuits

- BiCMOS Technology combines Bipolar and CMOS Circuits on one IC chip
- CMOS (low-power, high input impedance, wide noise margins) + Bipolar (high current-driving capability)
- Particularly useful for logic with large fan-out (large capacitive load)

The Simple BiCMOS Inverter

- Cascading each of the $Q_N$ and $Q_P$ devices of the MCOS inverter with an $npn$ transistor
- Input high:
  - $Q_N$ turns on and the drain current flows into the base of $Q_2$ as the base current
  - The initial discharge current $\approx i_{DN} + b_i_{DN} \rightarrow v_O$ drops
  - $Q_N$ in deep triode with $i_D = 0$ as $v_O$ drops to $V_{BEon} (\approx 0.7V) \rightarrow V_{OL} = V_{BEon}$
- Input low:
  - $Q_P$ turns on and the drain current flows into the base of $Q_1$ as the base current
  - The initial discharge current $\approx (b + 1) i_{DP} \rightarrow v_O$ increases
  - $Q_P$ in deep triode with $i_{DP}=0$ as $v_O$ drops to $V_{BEon} (\approx 0.7V) \rightarrow V_{OH} = V_{DD} - V_{BEon}$
- $Q_1$ and $Q_2$ are operating in nonsaturation mode and will not turn on simultaneously
- Reduced noise margin due to smaller logic swing
- No base discharge path to speed up the turn-off of $Q_1$ and $Q_2 \rightarrow$ long turn-off delays.
BiCMOS Inverter with “Bleeder Resistors”

- Resistor $R_1$ and $R_2$ are added to provide base discharge paths for $Q_1$ and $Q_2$ turn-off
- Input high:
  - $Q_N$ turns on and $Q_P$ turns off → provides discharging current through $Q_N$ and $Q_2$
  - $v_O$ is discharged below $V_{BEon}$ through $Q_N$ and $R_2$ → improved noise margin
  - Pulling $v_O$ from $V_{BEon}$ to ground is rather slow due to the high impedance path ($Q_N$ and $R_2$)
- Input low:
  - $Q_N$ turns off and $Q_P$ turns on → provides charging current through $Q_P$ and $Q_1$
  - A dc current path exist from $V_{DD}$ to ground through $Q_P$ and $R_1$ when $Q_1$ is off
  - $v_O$ can only be charged up to $V_{DD} - V_{DS,P} - V_{BEon}$ by $Q_1$
- $R_1$ and $R_2$ take some of the drain currents of $Q_P$ and $Q_N$ away from the bases of $Q_1$ and $Q_2$ and thus slightly reduce the output charging/discharging currents of the gate
- $R_1$ and $R_2$ are typically implemented by MOSFET $Q_{R1}$ and $Q_{R2}$
- $Q_{R1}$ conducts only when $v_I$ is high → $R_1$ to discharge $Q_1$
- $Q_{R2}$ conducts only when $v_I$ is low → $R_2$ to discharge $Q_2$
BiCMOS Inverter “R-circuit”

- $R_1$ is connected to the output node rather than returning to ground:
- The problem of static power dissipation is now solved
- $R_1$ now functions as a pull-up resistor, pulling the output node voltage up to $V_{DD}$
Dynamic Operation

- The detailed analysis of the dynamic operation is rather complex
- Propagation delay is estimated by the time required to charge and discharge a load capacitance $C$
- Such an approximation is justified in cases where $C$ is relatively large
- Usually the case for application of BiCMOS inverters

\[
 i_D = \frac{1}{2} k_p \left( \frac{W}{L} \right)_p (V_{DD} - |V_{ip}|)^2
\]

\[
 i_R = \frac{V_{BEon}}{R_1}
\]

\[
 i_B = i_D - i_R
\]

\[
 i = (1 + \beta) i_B + i_R
\]

\[
 t_{PLH} \approx \frac{CV_{DD}}{2i}
\]
BiCMOS Logic Gates

- BiCMOS logic gates can be implemented following the same approach as the inverters
- The bipolar portion simply functions as an output stage
- $Q_N$ and $Q_P$ are replaced by pull-down network and pull-up network