# CHAPTER 16 ADVANCED MOS AND BIPOLAR LOGIC CIRCUITS

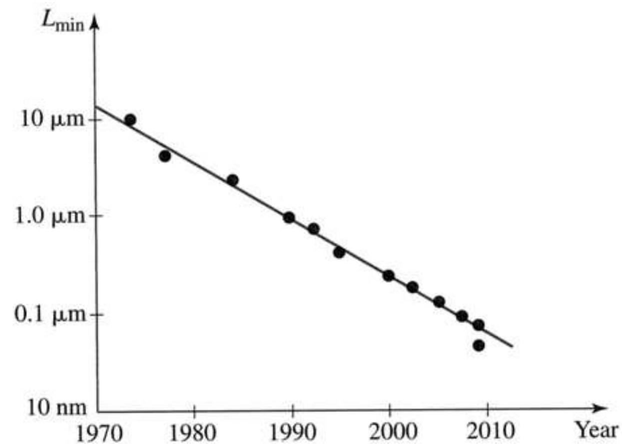
## Chapter Outline

16.1 Implications of Technology Scaling
16.2 Digital IC Technology, Logic-Circuit Family and Design Methodologies
16.3 Pseudo-NMOS Logic Circuits
16.4 Pass-Transistor Logic Circuits
16.5 Dynamic MOS Logic Circuits

# 16.1 Implications of Technology Scaling

## Moore's Law

- ❑A new technology is developed for every 2~3 years due to cost and speed requirement
- ❑The trend was predicted more than 40 years ago by Gordon Moore
- ❑For every new technology generation:
  - ■ The minimum length is reduced by a factor of 1.414 and the area is reduced by a factor of 2
  - ■ The cost is reduced by half or the circuit complexity is doubled
  - ■ Device scaling generally decreases the parasitics and enhances the operating speed
  - ■ The operating power is reduced
- ❑The current technology node advances into deep-submicron
- ❑Issues in deep-submicron technologies have to be taken into account for circuit designs

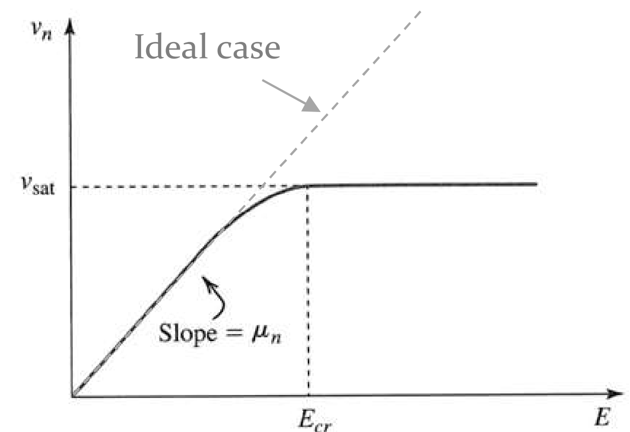


## Scaling Implications

| Implications of Device and Voltage Scaling | | | |
|---|---|---|---|
| | Parameter | Relationship | Scaling Factor |
| 1 | $W, L, t_{ox}$ | | $1/S$ |
| 2 | $V_{DD}, V_t$ | | $1/S$ |
| 3 | Area/Device | $WL$ | $1/S^2$ |
| 4 | $C_{ox}$ | $\varepsilon_{ox}/t_{ox}$ | $S$ |
| 5 | $k_n', k_p'$ | $\mu_n C_{ox}, \mu_p C_{ox}$ | $S$ |
| 6 | $C_{gate}$ | $WLC_{ox}$ | $1/S$ |
| 7 | $t_P$ (intrinsic) | $\alpha C/k' V_{DD}$ | $1/S$ |
| 8 | Energy/Switching cycle (intrinsic) | $CV_{DD}^2$ | $1/S^3$ |
| 9 | $P_{dyn}$ | $f_{max} CV_{DD}^2 = \frac{CV_{DD}^2}{2t_P}$ | $1/S^2$ |
| 10 | Power density | $P_{dyn}$/Device area | 1 |

## Velocity Saturation

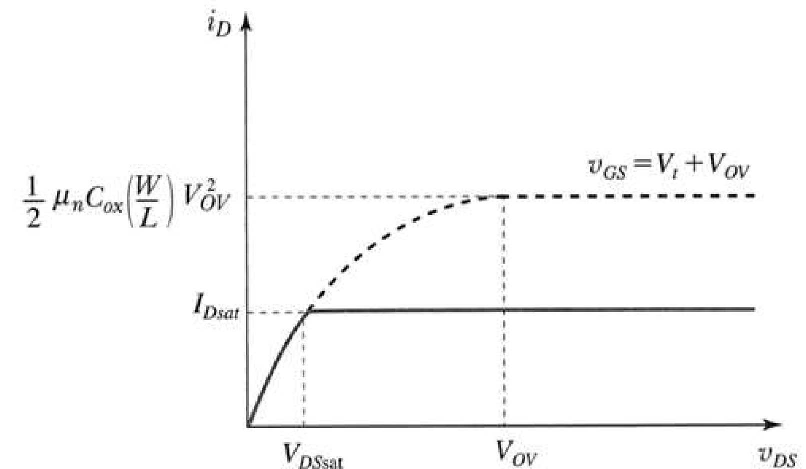
- Long-channel devices:
  - Drift velocity: $v_n = \mu_n E$
  - Electric field in the channel: $E = v_{DS}/L$
- Short-channel devices:
  - Velocity saturates at a critical field $E_{cr}$ with $v_{sat} \cong 10^7$ cm/s
  - The $v_{DS}$ at which velocity saturates is denoted by $V_{DSsat}$
  - $V_{DSsat} = E_{cr}L = v_{sat}L/\mu_n$
  - $V_{DSsat}$ is a device parameter




## The I-V Characteristics

- Long-channel devices
  - Saturation current: $i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)^2$
- Short-channel devices
  - For $v_{GS}$-$V_t$ < $V_{DSsat}$: same as long-channel devices
  - For $v_{GS}$-$V_t$ > $V_{DSsat}$:

$$I_{Dsat} = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS}-V_t)V_{DSsat}-\frac{1}{2}V_{DSsat}^2\right]$$
$$= WC_{ox}v_{sat}\left(V_{GS}-V_t-\frac{1}{2}V_{DSsat}\right)$$

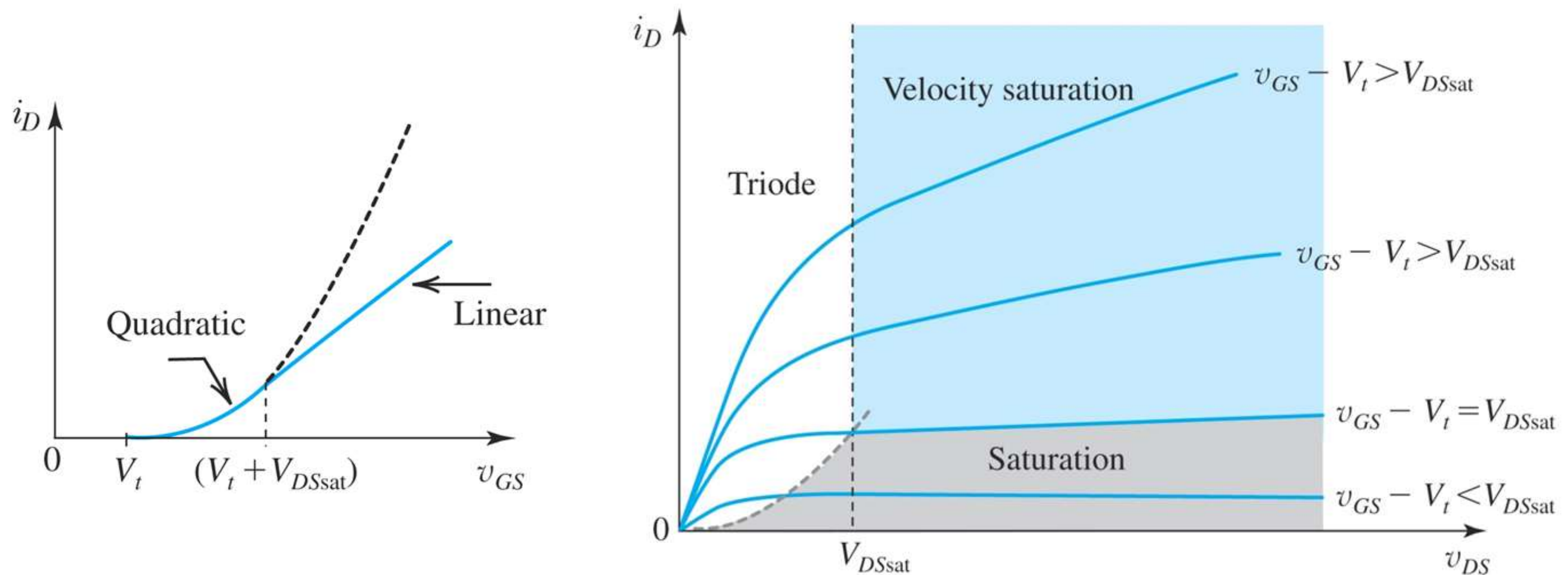


## Current Equation for Velocity Saturation

- For $v_{GS}$-$V_t \geq V_{DSsat}$ and $v_{DS} \geq V_{DSsat}$, a general expression of the drain current is given by

$$i_D = \mu_n C_{ox} \frac{W}{L} V_{DSsat} \left( v_{GS} - V_t - \frac{1}{2} V_{DSsat} \right) (1 + \lambda V_{DS})$$

  - The current is reduced from the predication of a long-channel device
  - The dependence on $v_{GS}$ is more linear rather than quadratic
- Four regions of operation: cutoff, triode, saturation and velocity saturation
- Short-channel PMOS transistors undergo velocity saturation at the same value of $v_{sat}$
- The effects on PMOS are less pronounced due to lower mobility and higher $V_{DSsat}$

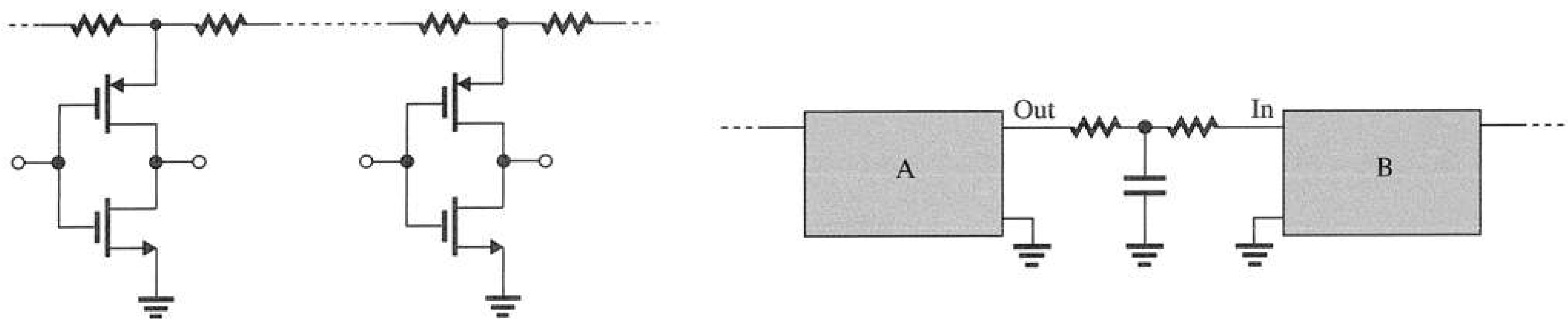


## Subthreshold Conduction

- The device is not complete off in deep-submicron devices as $v_{GS} < V_t$
- The subthreshold current is exponentially proportional to $v_{GS}$: $i_D = I_s \exp(v_{GS}/nV_T)$
- It is a problem in digital IC design for two reasons:
  - Such current leads to nonzero static power dissipation for CMOS logics
  - May cause undesirable discharge of capacitors in dynamic CMOS logics

## The Interconnect

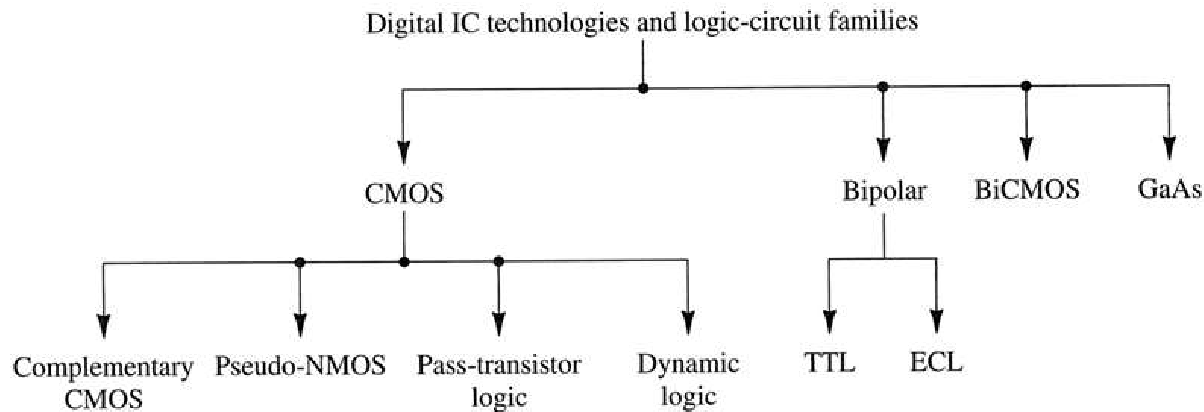
- The width of the interconnect scales down with the CMOS technology
- The metal wire is no longer an ideal short
  - Series parasitic resistance may cause undesirable voltage drop and excess delay
  - Parasitic capacitance to ground may lead to speed degradation and additional dynamic power



# 16.2 Digital IC Technology, Logic-Circuit Families, and Design Methodologies

## Logic-Circuit Families

- ❑ Classified by fabrication technology: CMOS, Bipolar, BiCMOS, GaAs
- ❑ Most widely logic-circuit technology is CMOS
- ❑ Various logic families are implemented in CMOS technology



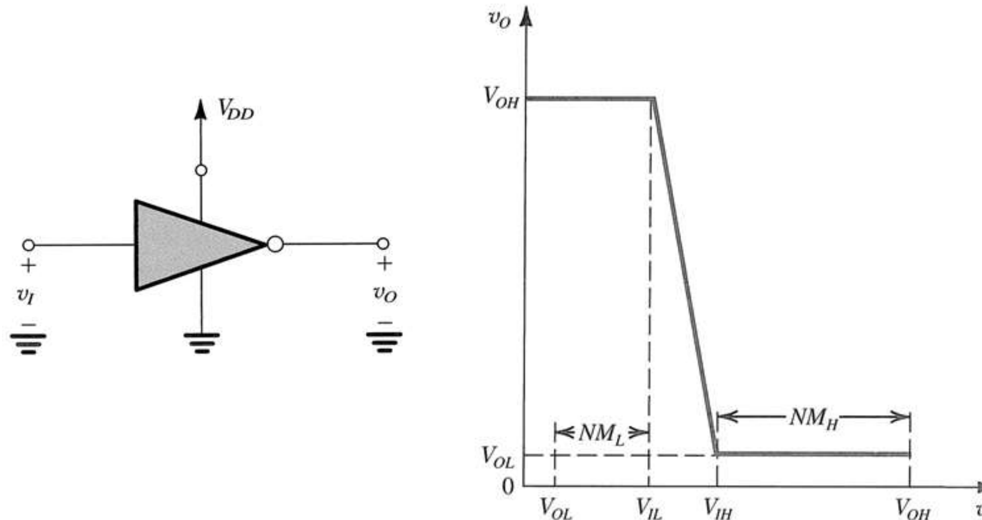

## Styles for Digital System Design

- ❑ Assemble the system using standard IC packages of various levels of complexity
- ❑ Application specific IC (ASIC) with customized digital design when large volume is required
- ❑ Semicustom design:
  - ■ Gate-array (unconnected logic gates) with final customized metallization step
  - ■ Field-programmable gate array (FPGA) can be programmed by the user

# 16.3 The Pseudo-NMOS Logic Circuits

## The Voltage-Transfer Characteristic (VTC)

- The function of the inverter is to invert the logic value of its input signal
- The voltage-transfer characteristic is used to evaluate the quality of inverter operation

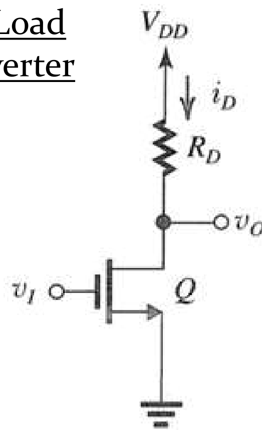



- VTC parameters
  - $V_{OH}$: output high level
  - $V_{OL}$: output low level
  - $V_{IH}$: the minimum value of input interpreted by the inverter as a logic 1
  - $V_{IL}$: the maximum value of input interpreted by the inverter as a logic 0
  - Transition region: input level between $V_{IL}$ and $V_{IH}$

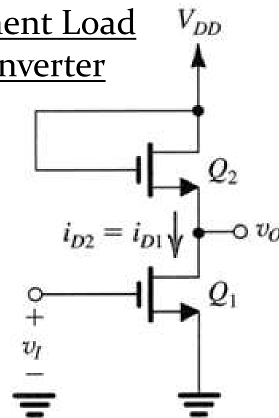
## NMOS Inverter Circuits

- A simple inverter circuit is composed of a NMOS and a load
- The load can be realized by a resistor or another NMOS device

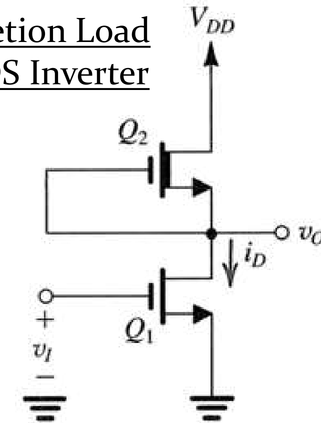
Resistive Load NMOS Inverter




Enhancement Load NMOS Inverter



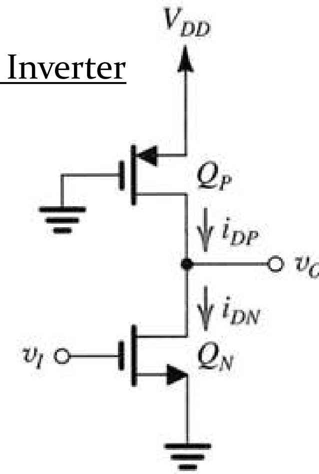

Depletion Load NMOS Inverter




## Pseudo-NMOS Inverters

- Use a PMOS transistor as the load
- Does not suffer from body effect
- Directly compatible with complementary CMOS circuits
- Area and delay penalties arising from the fan-in in complementary CMOS gate is reduces

Pseudo-NMOS Inverter



## Static Characteristics

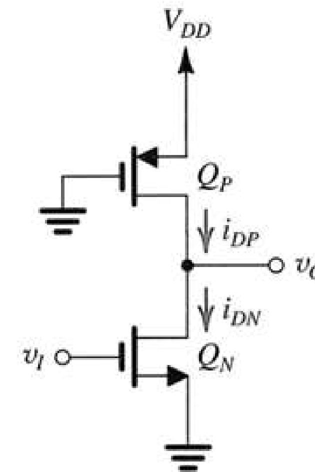
- Load curve represents a much lower saturation current
- $k_n$ is usually greater than $k_p$ by a factor of 4 to 10
- A ratioed type logic with $r \equiv k_n/k_p$
- The logic is typically operated in two extremely cases:
  - $v_I = 0$: $v_O = V_{OH} = V_{DD}$
  - $v_I = V_{DD}$: $v_O = V_{OL} > 0$ (nonzero $V_{OL}$ for pseudo-NMOS)
- The VTC can be derived based on $i_{DN}$ and $i_{DP}$:

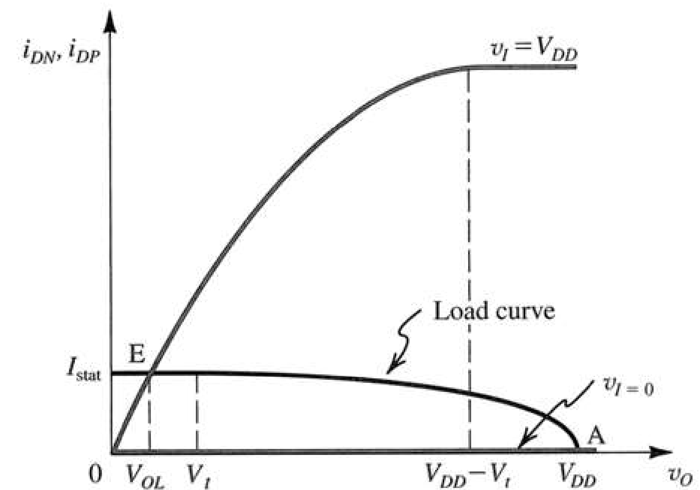
$$i_{DN} = \frac{1}{2} k_n (v_I - V_t)^2 \quad \text{for } v_O \geq v_I - V_t \quad \text{(saturation)}$$

$$i_{DN} = k_n \left[ (v_I - V_t) v_O - \frac{1}{2} v_O^2 \right] \quad \text{for } v_O \leq v_I - V_t \quad \text{(triode)}$$

$$i_{DP} = \frac{1}{2} k_p (V_{DD} - V_t)^2 \quad \text{for } v_O \leq V_t \quad \text{(saturation)}$$

$$i_{DP} = k_p \left[ (V_{DD} - V_t)(V_{DD} - v_O) - \frac{1}{2} (V_{DD} - v_O)^2 \right] \quad \text{for } v_O \geq V_t \quad \text{(triode)}$$



## Derivation of the VTC

- Assume $V_{tn} = |V_{tp}| = V_t$ for the derivations
- Region I (Segment AB):

$$v_O = V_{OH} = V_{DD}$$

- Region II (Segment BC):

$$v_O = V_t + \sqrt{(V_{DD} - V_t)^2 - r(v_I - V_t)^2}$$

- Region III (Segment CD):

$$r\left[(v_I - V_t)v_O - \frac{1}{2}v_O^2\right] = \left[(V_{DD} - V_t)(V_{DD} - v_O) - \frac{1}{2}(V_{DD} - v_O)^2\right]$$

- Region IV (Segment DE):

$$v_O = (v_I - V_t) - \sqrt{(v_I - V_t)^2 - \frac{1}{r}(V_{DD} - V_t)^2}$$

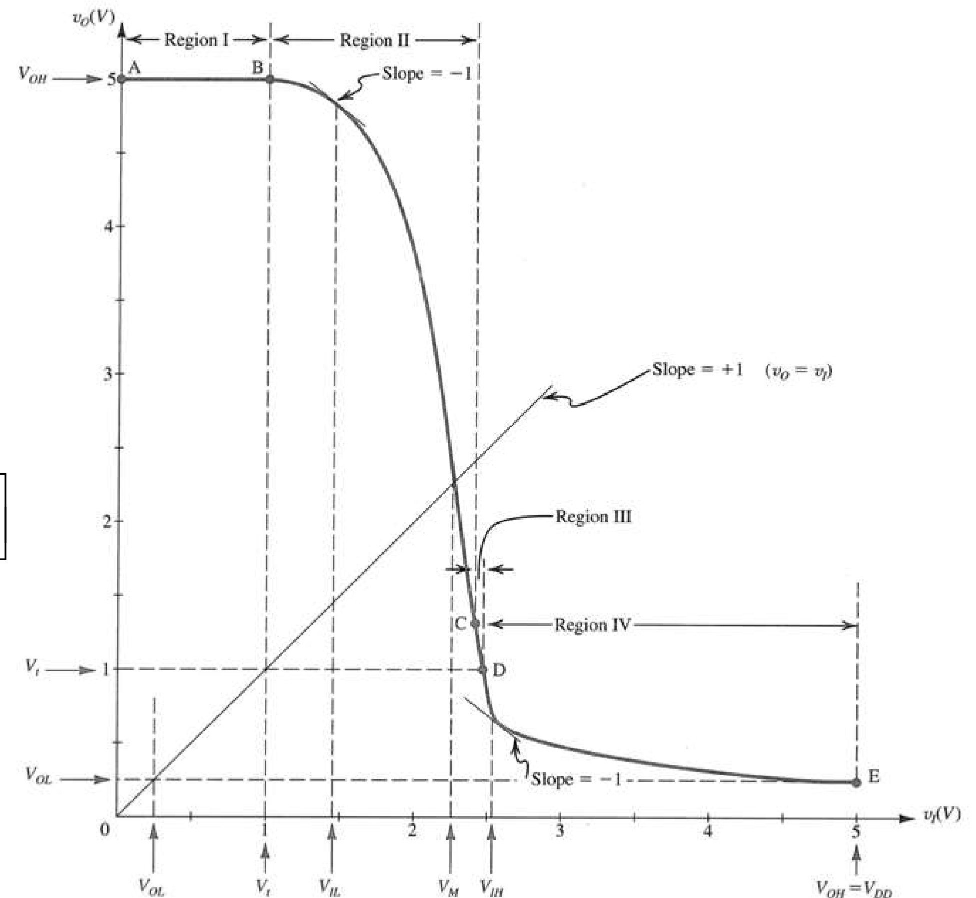
- Static Characteristics:

$$V_{OH} = V_{DD} \qquad V_{OL} = (V_{DD} - V_t)(1 - \sqrt{1 - k_p / k_n})$$

$$V_{IH} = V_t + \frac{2}{\sqrt{3k_n / k_p}}(V_{DD} - V_t) \qquad V_{IL} = V_t + \frac{V_{DD} - V_t}{\sqrt{(k_n / k_p)(k_n / k_p + 1)}}$$

$$NM_H = V_{OH} - V_{IH} \qquad NM_L = V_{IL} - V_{OL}$$

$$V_M = V_t + \frac{V_{DD} - V_t}{\sqrt{k_n / k_p + 1}}$$




| Region | VTC Segment | $Q_N$ | $Q_P$ | Condition |
|---|---|---|---|---|
| I | AB | Cut-off | Triode | $v_I < V_t$ |
| II | BC | Saturation | Triode | $v_O > v_I - V_t$ |
| III | CD | Triode | Triode | $V_t < v_O < v_I - V_t$ |
| IV | DE | Triode | Saturation | $v_O < V_t$ |

## Dynamic Operation

- Determine $t_{PLH}$:
  - The analysis is identical to the CMOS inverter and the output $C$ is charged by PMOS

$$t_{PLH} = \frac{\alpha_p C}{k_p V_{DD}} \quad \text{where} \quad \alpha_p = 2 \Big/ \left[ \frac{7}{4} - 3\left(\frac{V_t}{V_{DD}}\right) + \left(\frac{V_t}{V_{DD}}\right)^2 \right]$$

- Determine $t_{PHL}$:
  - The discharge current is $i_{DN} - i_{DP}$ while $i_{DP}$ is typically negligible as $r$ is large

$$t_{PHL} = \frac{\alpha_n C}{k_n V_{DD}} \quad \text{where} \quad \alpha_n = 2 \Big/ \left[ 1 + \frac{3}{4}\left(1 - \frac{1}{r}\right) - \left(3 - \frac{1}{r}\right)\left(\frac{V_t}{V_{DD}}\right) + \left(\frac{V_t}{V_{DD}}\right)^2 \right]$$

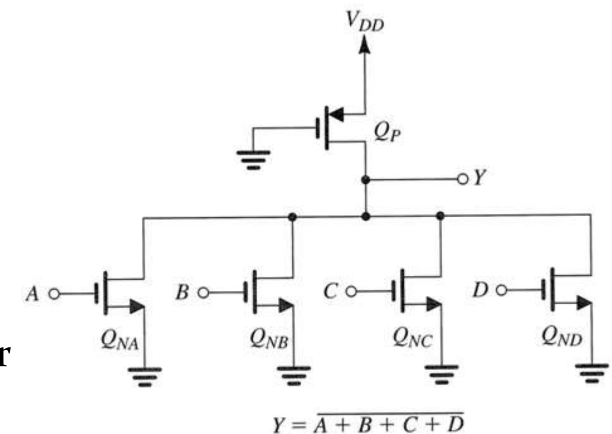
- $\alpha_n \cong \alpha_p$ for a large value of $r$ and $t_{PLH}$ is much larger than $t_{PHL}$

## Design of Pseudo-NMOS Inverter

- Determine ratio $r = k_n / k_p$
  - The larger the value of $r$, the lower $V_{OL}$ is and the wider the noise margins are
  - A larger $r$ increases the asymmetry in the dynamic response
  - Usually, $r$ is selected in the range of 4 to 10
- Determine $(W/L)_n$ and $(W/L)_p$
  - A smaller $(W/L)$ to keep the gate area small and thus obtain a small value for $C$
  - A smaller $(W/L)$ to keeps $I_{sat}$ of $Q_P$ and static power dissipation low
  - Larger $(W/L)$ ratios in order to obtain low $t_P$ and thus fast response

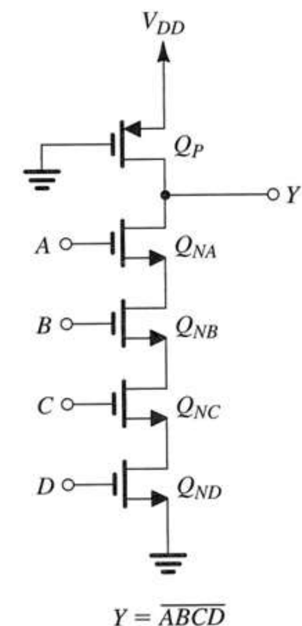
## Gate Circuits

- ❑ Identical to PDN of CMOS gate except for the load device
- ❑ The $(W/L)$ ratio of the load device is chosen as the basic inverter
- ❑ The $(W/L)$ ratios of the PDN are chosen for a worst-case gate delay equal to that of the basic inverter (assuming $C$ is constant)




## Concluding Remarks

- ❑ In pseudo-NMOS, NOR gates are preferred over NAND gates in order to use minimum-size devices
- ❑ Pseudo-NMOS is particularly suited for applications in which output remains high most of the time
  - ■ Static power dissipation can be reasonably low
  - ■ The output transitions that matter would presumably be high-to-low



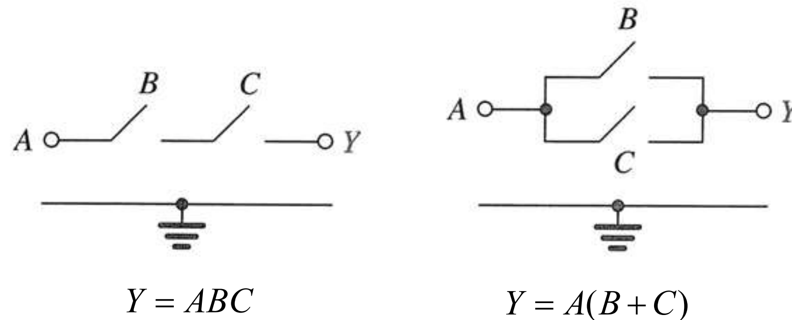

## Comparison with CMOS Logic

- ❑ The transistor number is reduced for lower implementation cost
- ❑ The routing complexity is reduced
- ❑ Output capacitance is reduced for higher speed
- ❑ Rationed design
- ❑ Nonzero static power dissipation

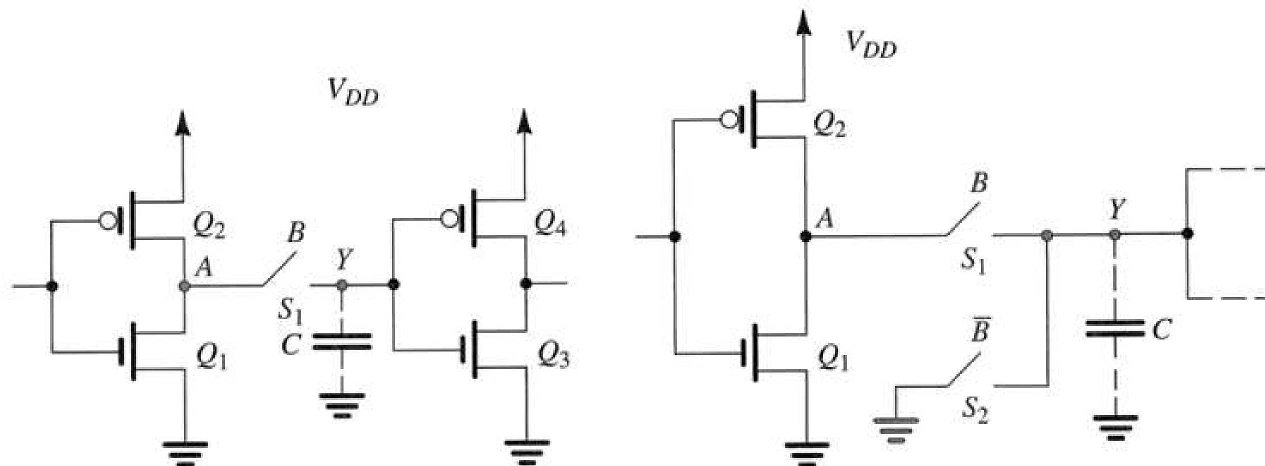
# 16.4 Pass-Transistor Logic Circuits

## Design of Pass-Transistor Logic (PTL) Circuits

- Using series and parallel combinations of switches
- The switches are controlled by input logic variables to connect the input and output nodes
- Can be implemented by a single NMOS transistor or CMOS transmission gate
- Every circuit node has **at all times** a low-resistance path to $V_{DD}$ or ground

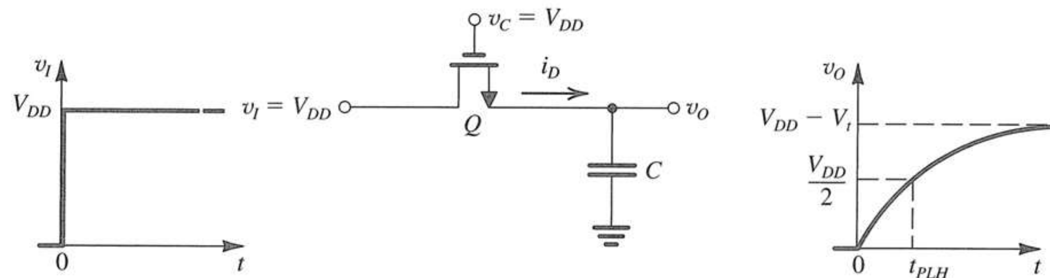



$Y = ABC$ $\qquad$ $Y = A(B+C)$

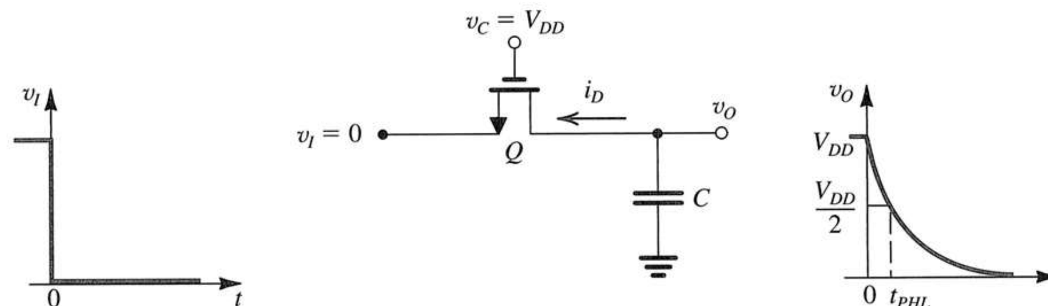


## Operation with NMOS Transistor as the Switch

- Pass-transistor with output high ("*poor 1*")
  - The output node refers to the source terminal of the NMOS
  - $Q$ is in saturation during the charging process
  - $V_t$ increases with $v_O$ due to body effect → resulting in a large $t_{PLH}$
  - $V_{OH} = V_{DD} - V_t$ → reduced gate noise immunity and possible static power for the following CMOS inverter stage

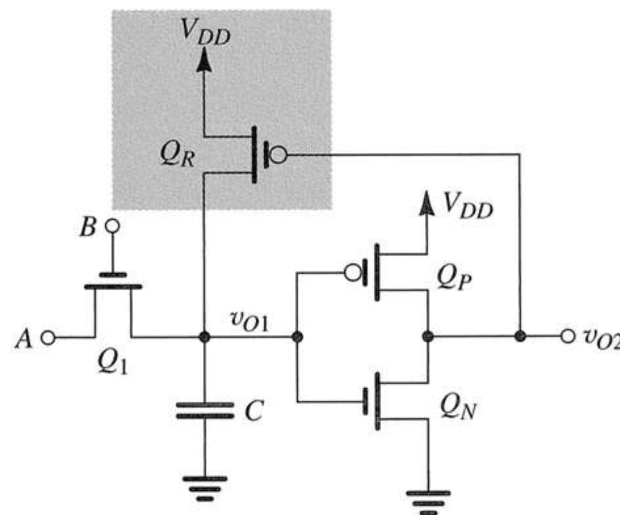



- Pass-transistor with output low ("*good 0*")
  - The input node refers to the source terminal of the NMOS (Body Effect is neglected)
  - The output node can be discharged completely → $V_{OL}$ = 0



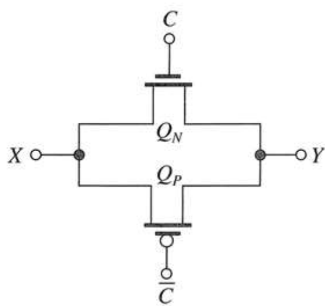
## Restoring the Output Level

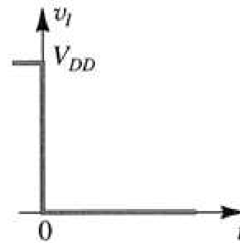
- The circuit-based approach by adding a feedback loop with $Q_R$
  - The PMOS $Q_R$ turns on by $v_{O2}$ (= "0") to restore the signal loss at $v_{O1}$ = "1"
  - The PMOS $Q_R$ is turn off by $v_{O2}$ (= "1") when $v_{O1}$ = "0"
  - Operation is more involved than it appears due to the positive feedback
  - $Q_R$ has to be a "weak PMOS transistor" in order not to play a major role in the circuit operation
- The alternative approach by process technology
  - The signal loss is due to the threshold voltage of the NMOS devices
  - Threshold adjustment by ion implantation to make zero-threshold devices
  - Subthreshold conduction becomes significant for zero-threshold devices

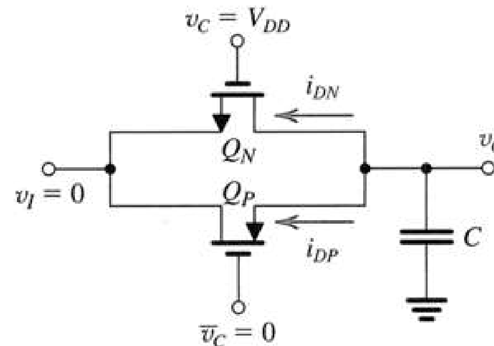


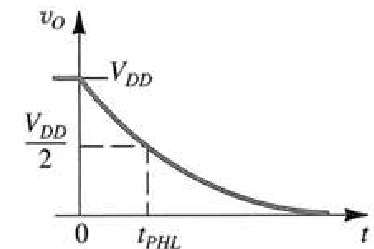
## The Use of CMOS Transmission Gates as Switches

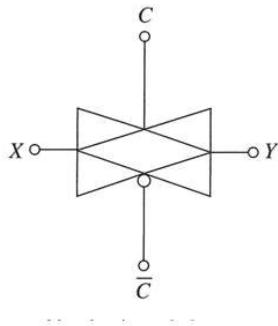
- ❑ PMOS and NMOS are in parallel with complementary control signal
- ❑ Both NMOS and PMOS provide charging/discharging current
- ❑ Good logic level with $V_{OH} = V_{DD}$ and $V_{OL} = 0$
- ❑ The complexity, silicon area and load capacitance are increased
- ❑ Body effect has to be taken into account to evaluate $i_{DN}$ and $i_{DP}$

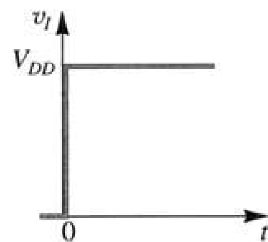


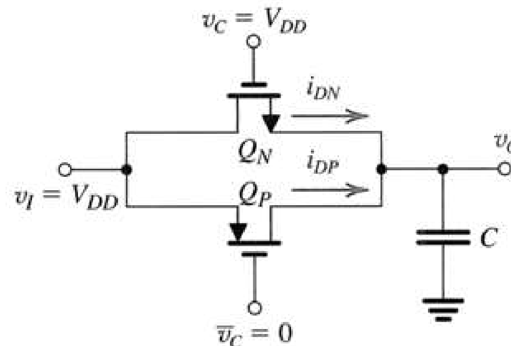



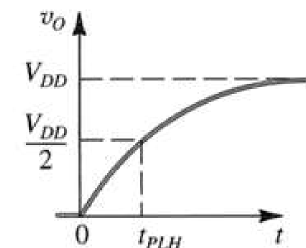



## The Equivalent Resistance of the Transmission Gate

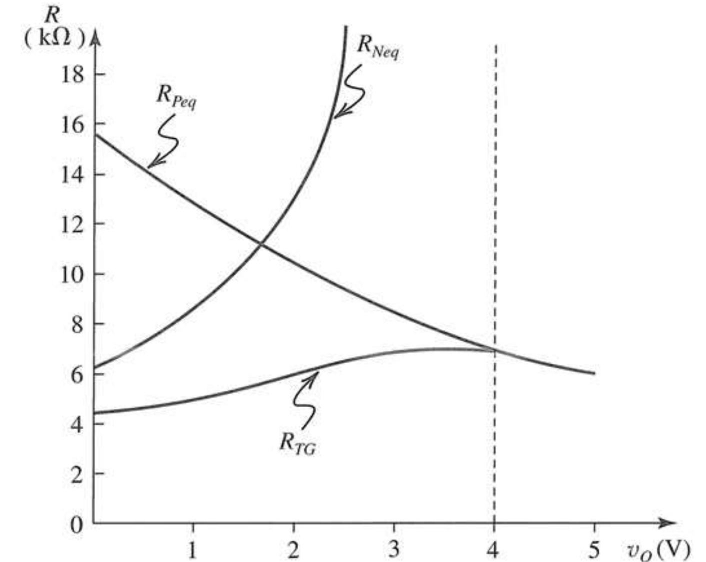
- The CMOS transmission gate in charging case is modeled by
- The equivalent resistance of $Q_N$:
  - For $v_O \le V_{DD} - V_{tn}$:

    $i_{DN} = \frac{1}{2}k_n(V_{DD} - V_{tn} - v_O)^2$ and $R_{Neq} = \dfrac{V_{DD} - v_O}{\frac{1}{2}k_n(V_{DD} - V_{tn} - v_O)^2}$
  - For $v_O > V_{DD} - V_{tn}$:

    $i_{DN} = 0$ and $R_{Neq} = \infty$
- The equivalent resistance of $Q_P$:
  - For $v_O \le |V_{tp}|$:

    $i_{DP} = \frac{1}{2}k_p(V_{DD} - |V_{tp}|)^2$ and $R_{Peq} = \dfrac{V_{DD} - v_O}{\frac{1}{2}k_p(V_{DD} - |V_{tp}|)^2}$
  - For $v_O > |V_{tp}|$:

$$i_{DP} = k_p\left[(V_{DD} - |V_{tp}|)(V_{DD} - v_O) - \frac{1}{2}(V_{DD} - v_O)^2\right] \text{ and } R_{Peq} = \frac{V_{DD} - v_O}{k_p\left[(V_{DD} - |V_{tp}|)(V_{DD} - v_O) - \frac{1}{2}(V_{DD} - v_O)^2\right]}$$

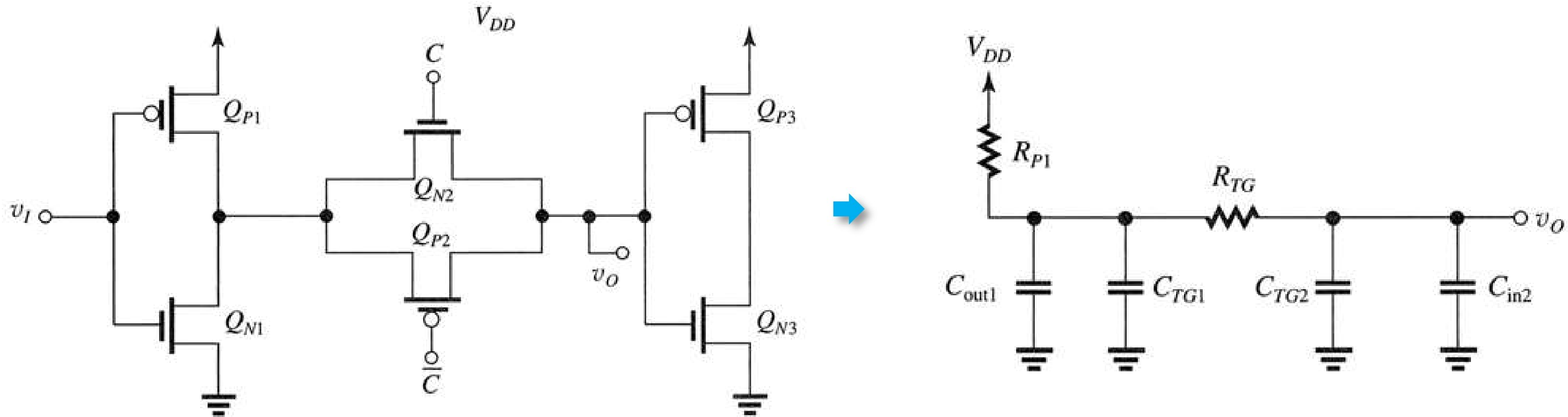



- $R_{TG} = R_{Neq}||R_{Peq}$ remains relatively constant over the full range
- The case for discharging can be obtained by similar analysis
- Empirical formula of $R_{TG}$ with $(W/L)_n = (W/L)_p$ for certain CMOS technologies is

$$R_{TG} = \frac{12.5}{(W/L)_n}(k\Omega)$$

## Calculation of Propagation Delay in the Signal Path

- The signal path containing multiple transmission gates can be modeled by resistors and capacitors

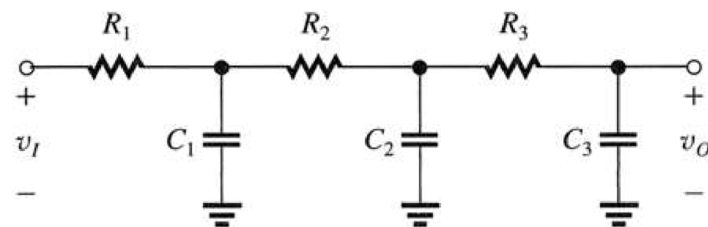



- The model is in a form of an *RC* ladder network
- The propagation delay is given by Elmore delay formula as

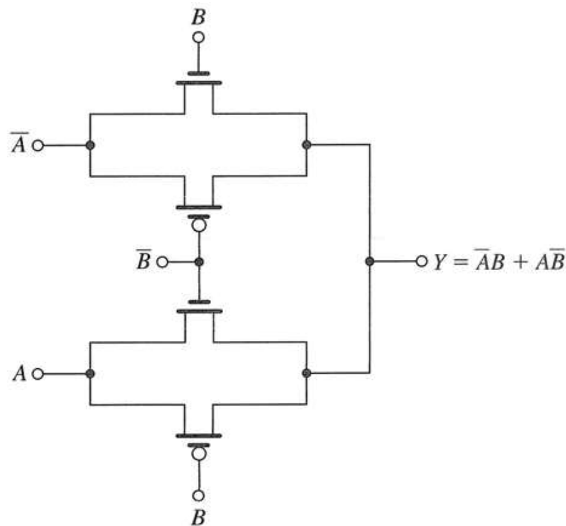
$$t_P = 0.69[(C_{out1} + C_{TG1})R_{P1} + (C_{TG2} + C_{in2})(R_{P1} + R_{TG})]$$

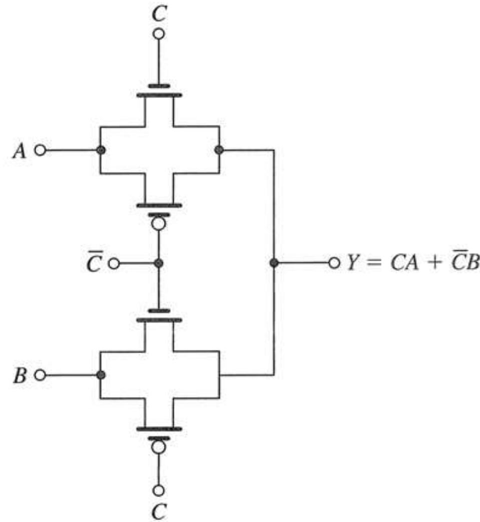
- The factor 0.69 is dropped for estimation as the input is not a step function
- *Elmore delay formula is given by

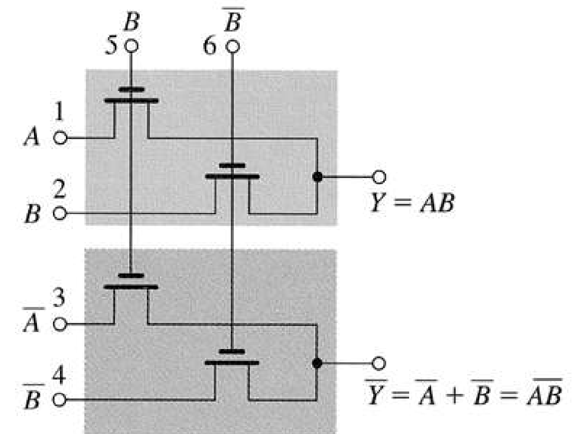
$$t_P = 0.69[C_1 R_1 + C_2(R_1 + R_2) + C_3(R_1 + R_2 + R_3) + \ldots]$$



## Pass-Transistor Logic Circuit Examples




## Final Remarks

- Advantages of CMOS transmission gate over pass-transistor logic with NMOS devices
  - Logic level: good "1" and "0"
  - No level restoring technique needed
- Disadvantages of CMOS transmission gate over pass-transistor logic with NMOS devices
  - Silicon area and complexity: an additional input requires one NMOS and one PMOS devices
  - Complementary control signal required
  - Propagation delay: more capacitive loading from the MOSFETs

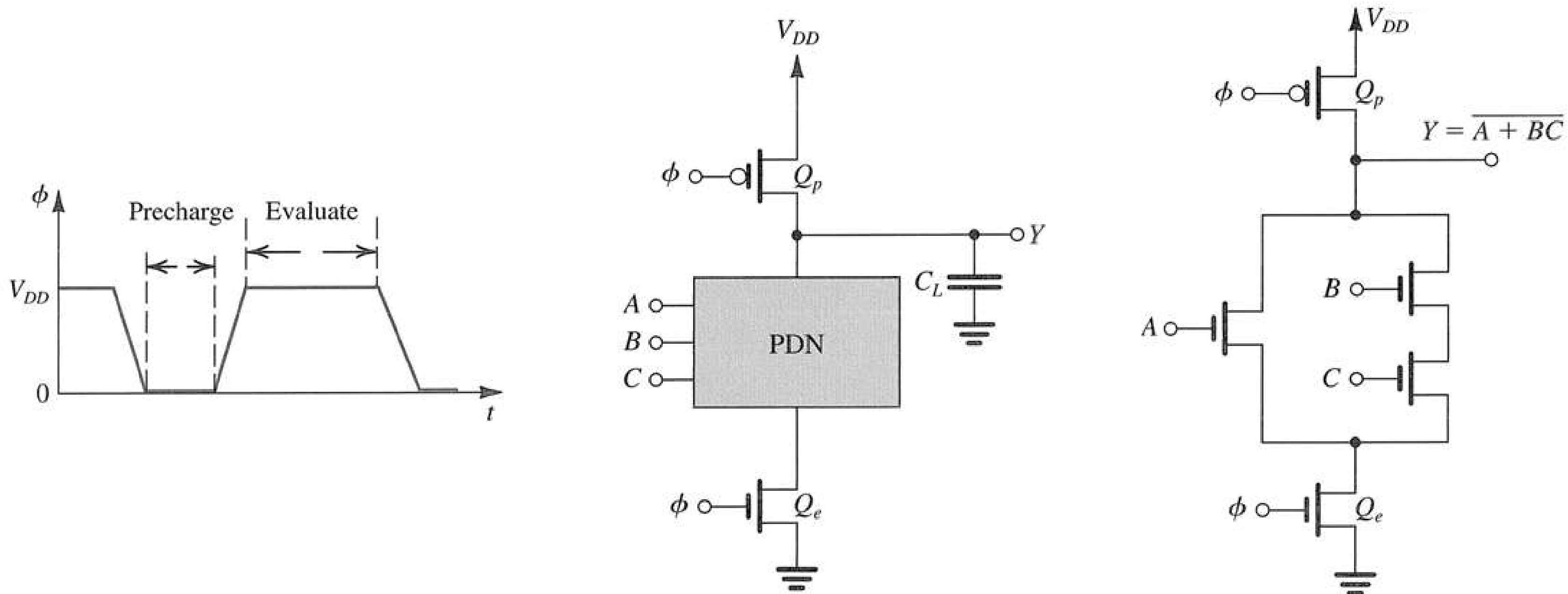
# 16.5 Dynamic MOS Logic Circuits

## Principle of Dynamic Logic Circuits

- Rely on the storage of signal voltage on parasitic capacitances at certain circuit nodes
- The circuits need to be periodically refreshed
- Maintain the low device count of pseudo-NMOS with zero static power dissipation

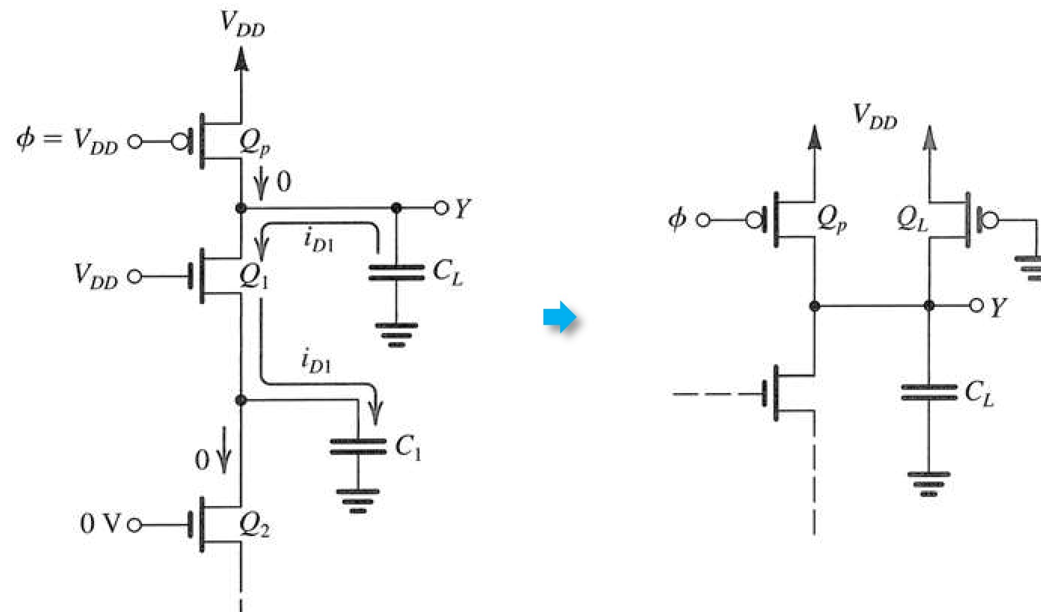
## Operation of Dynamic Logic Circuits

- Precharge phase: $Q_p$ on and $Q_e$ off $\rightarrow$ charge the output node to $V_{DD}$
- Evaluation phase: $Q_p$ off and $Q_e$ on $\rightarrow$ selectively discharge the output node through PDN



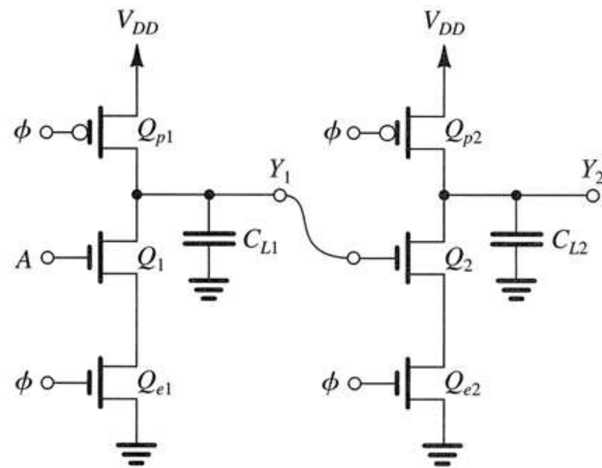
## Nonideal Effects

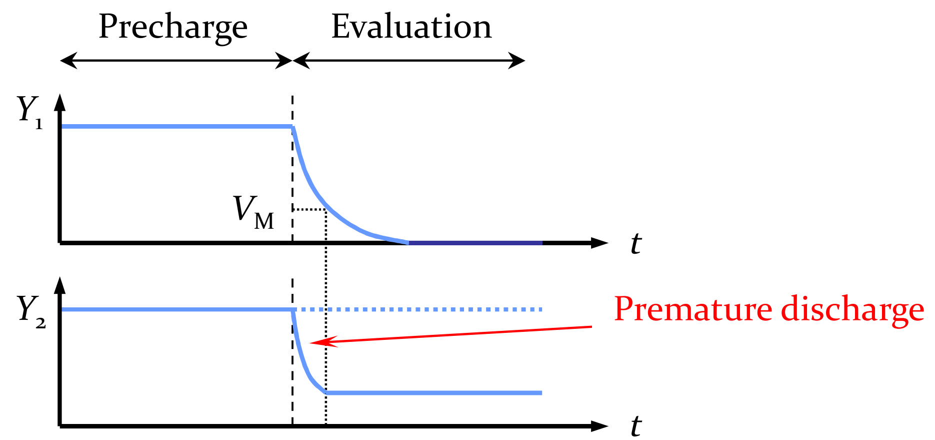
- Noise margin:
  - Since $V_{IL} \approx V_{IH} \approx V_{tn}$ , the resulting noise margins are $NM_L \approx V_{tn}$ and $NM_H \approx V_{DD} - V_{tn}$
  - Asymmetric noise immunity (poor $NM_L$)
- Output voltage decay due to leakage effects:
  - When PDN is off, leakage current will slowly discharge the output node
  - The leakage is from the reversed-biased junctions and possibly the subthreshold conduction
- Charge sharing:
  - Some of the internal nodes in PDN will share the charge in $C_L$ even the PDN path is off
  - Can be solved by adding a permanently turn-on transistor $Q_L$ at the cost of static power dissipation



# Domino CMOS Logic

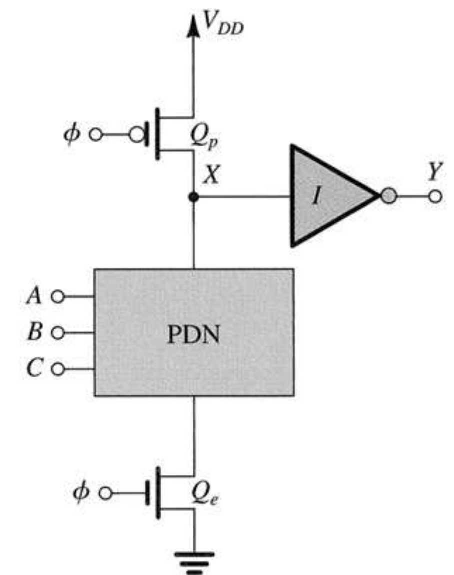
❑ Problem with cascading dynamic logic gates: errors caused by undesirable premature discharge



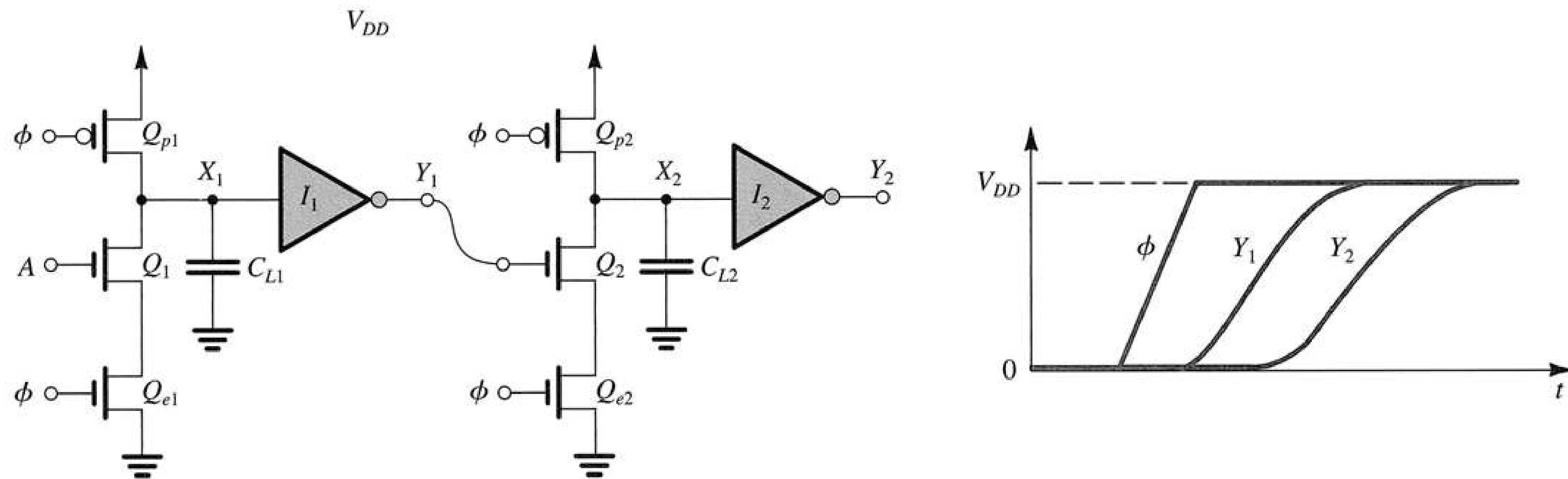




❑ Domino CMOS logic:

- A dynamic logic with a static CMOS inverter connected to its output
- The output to the following stages is 0 during the precharge phase
- Can alleviate the premature discharge problem



- A cascade of Domino CMOS logic:
  - Each stage has to wait for the rising edge from the preceding stage
  - The rising edge propagates through a cascade of gates




## Concluding Remarks

- Advantages of Domino logic: small area, high-speed operation, and zero static power dissipation
- Disadvantages of Domino logic:
  - Asymmetric noise margin
  - Leakage issue
  - Charge sharing
  - Dead time: unavailability of output during precharge phase