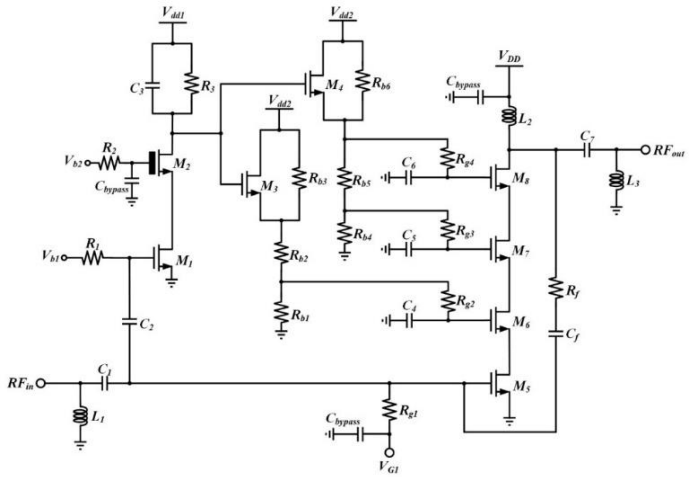
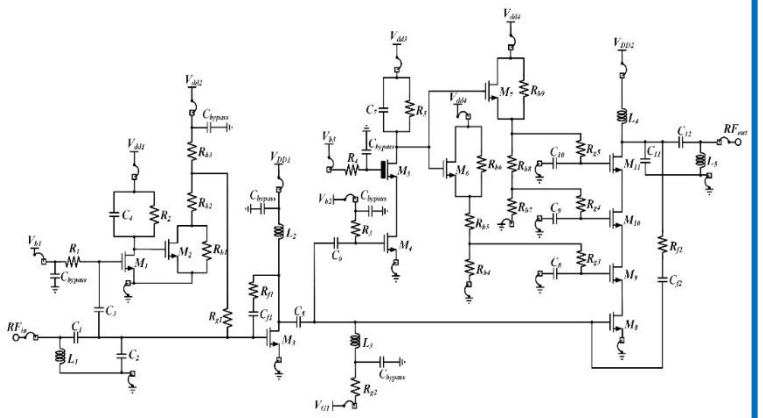
CMOS RF Power Amplifier with Adaptive Bias Linearization Technology

Schematic

First Work

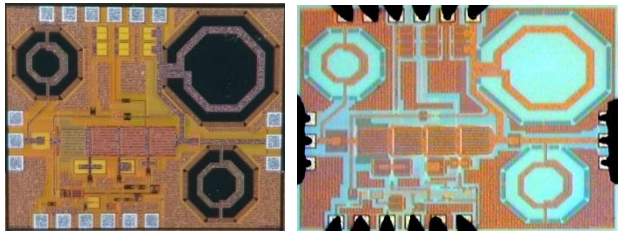


Second Work

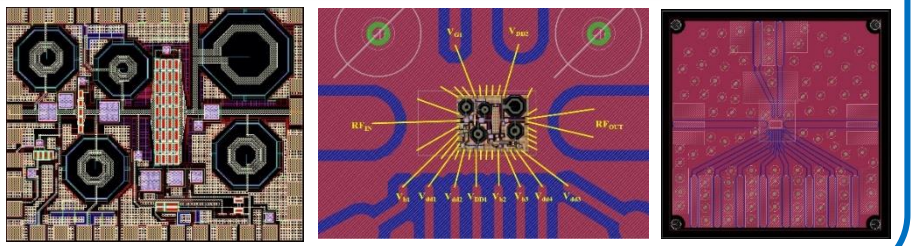


Chip & PCB

First Work

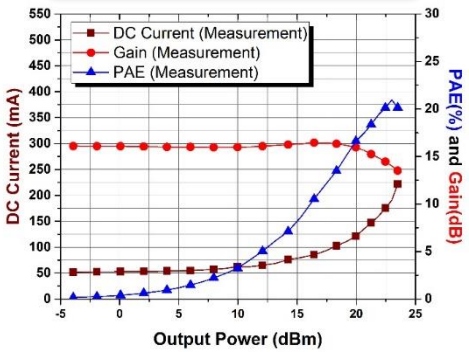


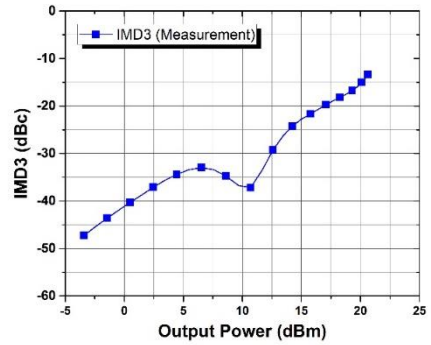
Second Work



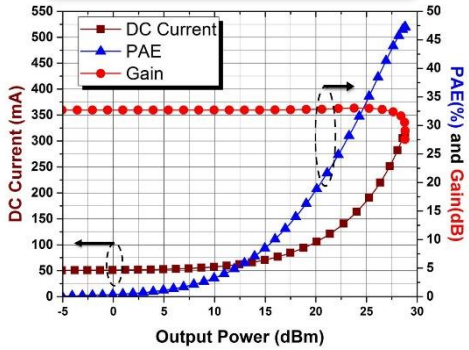
Measurement and Simulation Result

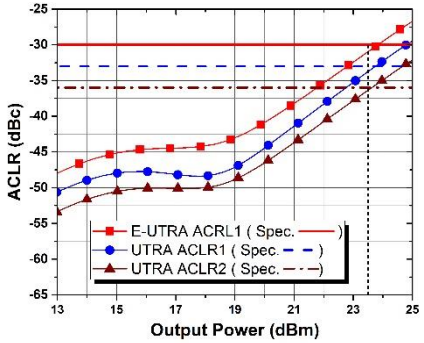
First Work





Second Work





	First Work	Second Work (Simulation)
Technology	0.13 μm	0.13 μm
V_{DD} (V)	4.8	4.8
Frequency(GHz)	1.95	1.95
Gain (dBm)	16.09	32.69
CW P_{1dB} (dBm)	21.87	28.41
CW P_{SAT} (dBm)	23	29.08
CW PAE@P_{1dB} (%)	19.41	46.37
CW PAE@P_{SAT} (%)	20.96	47.92
Modulated Signal	-	LTE 16 QAM 20 MHz
P_{avg} (dBm)	-	23.7
Modulated PAE (%)	-	28.4
E-$UTRA_{ACLR1}$ (dBc)	-	-30.61
Chip Size (mm^2)	1.21	1.24
Output Matching	on-chip	on-chip