High resolution Centered Digital Pulse Width Modulator

2013/12/31

Presenter : Jing-Hsien Fu

Advisor : Y-J Emery Chen

Graduate Institute of Electronics Engineering and
Department of Electrical Engineering,
National Taiwan University, Taipei, Taiwan

Summary

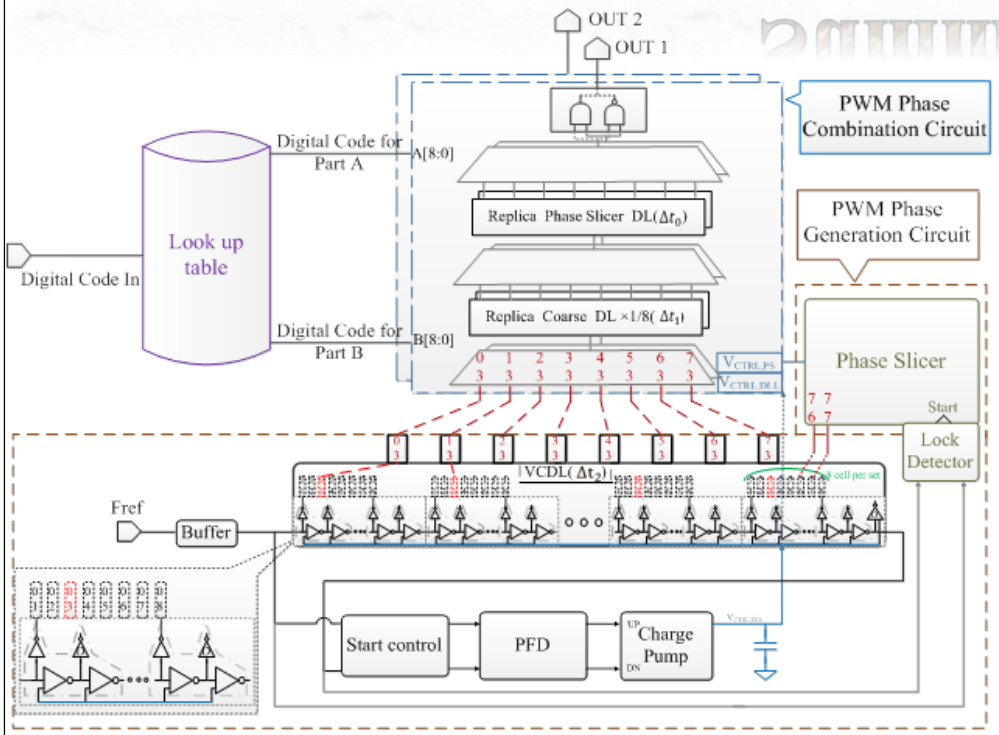

Table I
DPWM PERFORMANCE COMPARISON

	Simulation result	Measurement	[1]	[2]	[3]
Architecture	Centered DPWM with DLL&PS		Non-Centered Segmented Delay Line DPWM	Non-Centered Hybrid DPWM	Non-Centered Pulse Shrinking Mechanism DPWM
Type	Centered		Non-Centered	Non-Centered	Non-Centered
Process	90nm CMOS		0.6-µm CMOS	0.6-µm CMOS	0.35-µm CMOS
Supply Voltage	1.2V	1.0V	3.3 V	1.2 V	3.3 V
F_{ref}	30MHz		1MHz	1.8-7.4MHz	0.5-17MHz
Resolution	9-bit	n/a	6-bit	9-bit	8-bit
W_{LSB} ***	65.1ps		1560 ps	336 ps	229 ps
INL	0.4 LSB	0.43*	n/a	3.61	0.45/-0,6
DNL	0.41 LSB	0.45*	n/a	n/a	n/a
Power	24.6mW @30MHz	n/a	0.555 mW @1MHz	5 mW @7.4MHz	0.741 mW @1MHz
FOM**	1.6	n/a	8.7	1.31	2.89

*Between 45% & 55% **FOM= $\frac{power}{2^N \cdot sampling\ rate}$(pJ/bit) ***$W_{LSB}$= width per LSB