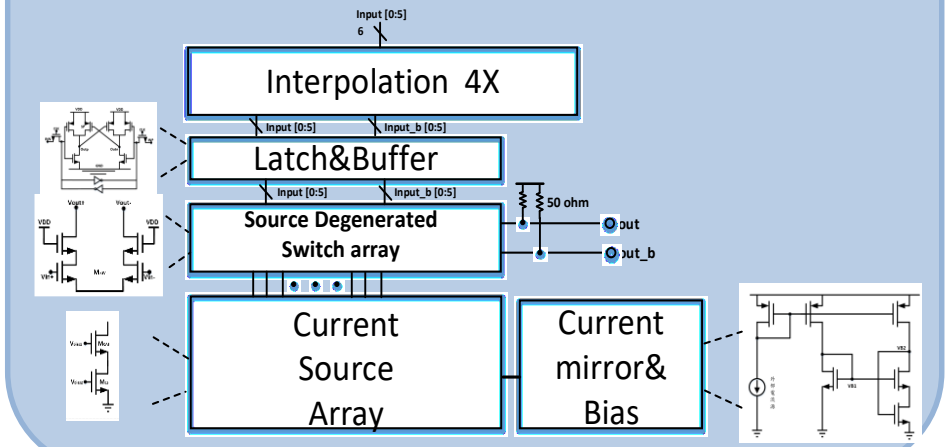
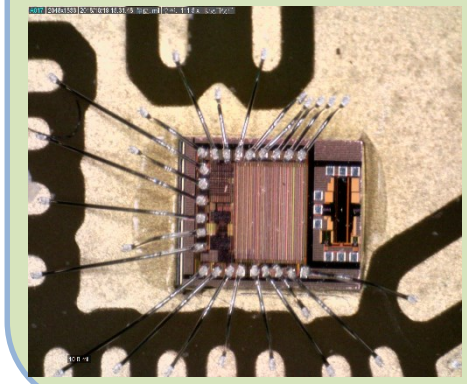
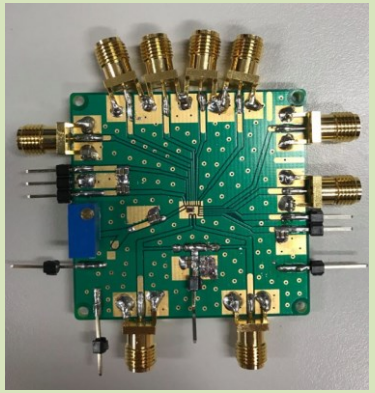
0.13μm CMOS Digital to Analog Converter with Upsampling Interpolation Technique

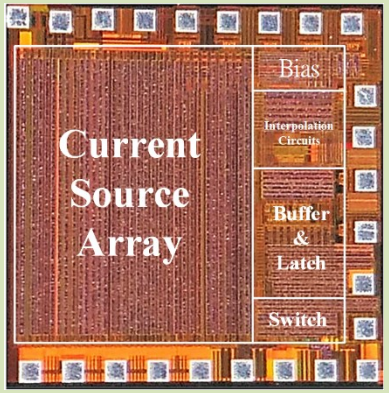
Architecture

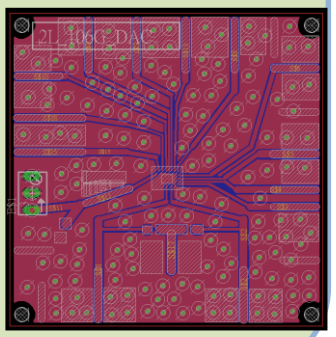


PCB & Chip

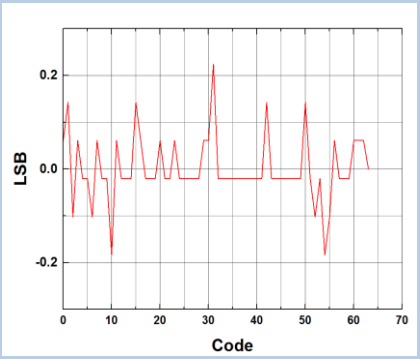


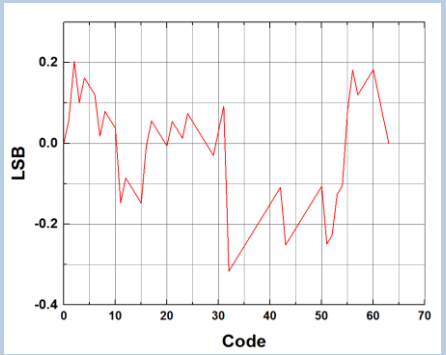




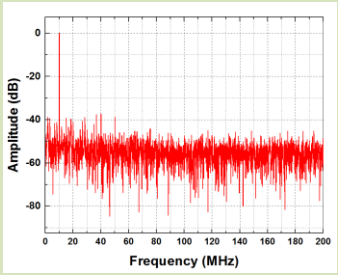


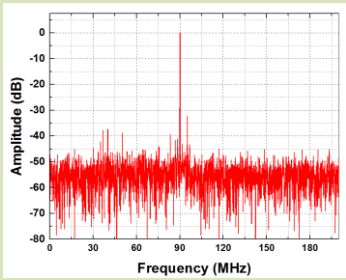
DNL / INL Measurement

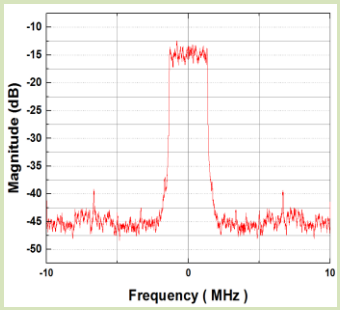


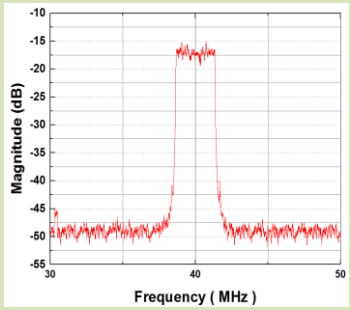


Measurement Result









Technology	0.13μm CMOS
Supply Voltage	1.2V
Resolution	6 bit
Sampling rate	200MHz upsampling to 800 MHz
Full swing scale	0.8 Vp-p
DNL	0.22 LSB
INL	0.316 LSB
SFDR	38dB @ Fin=10 MHz
Area	0.9× 0.9 mm^2
Power	23 mW
ACLR	-29.2 dBc @ Baseband -28.9 dBc @ Fc=40 MHz