Design Examples
Outlines

• Power Integrity Overview
• PI-induced EMI effect
• PI for LPDDR4 in InFO
Power Integrity Overview
Power Delivery Network

- High-f Caps
- Mid-f Caps
- Motherboard
- VRM
- Interconnects
- DeCap’s on PCB & package
Hierarchical Power Delivery Network

Multiple power/ground planes as PDN
Challenges in Power Delivery System

• With clock speeds increasing, supply voltages decreasing and the number of device on a chip increasing, the SSN is getting seriously.

• SSN is one of the major concerns for designing high speed circuit.

\[ \Delta V = N \cdot L \frac{di}{dt} \]

- Change of current ↑
- Number of device ↑
- Noise voltage ↑
- Effective inductance of PDN
- Rise/Fall time ↓
Target Impedance

- Target impedance states that voltage to current ratio has to equal the impedance in the network.

- If exceeds it at any freq., resultant power supply noise will exceeds 5% of Vdd

\[ Z_{Target} = \frac{V_{dd} \cdot \text{Ripple}}{I_{MAX}} \quad (\Omega) \]
Power Noise Signature

Ultra-High Frequency (not shown) ~ 10-100 GHz
Source: Die L, C

High Frequency ~100-1000 MHz
Source: Die/Package L, C

Mid Frequency ~1-10 Mhz
Source: Package/Socket/ Motherboard L, C

Low Frequency ~1-100 kHz
Source: Motherboard/ Voltage Regulator L, C

Localized Droops - may impact local circuit paths

Droops observed across the die - will impact all circuit paths
PI-Induced EMI
Overview – Ground Bounce Induced EMI

- Induced from ground bounce or other mechanisms.
- Fringing field and radiation.
- Interfere other devices.
- Signal-noise fluctuation, system crash.
20-H Rule vs. Edge Radiation

- 20-H rule – Back the edge of the power plane away from the edge of the board by a distance equal to 20 times the separation distance between the planes.
- Ground plane acts as a reflector.
- Maximum 6dB incremental in field strength ideally.

Cross View and Radiation
De-Caps vs. Edge Radiation

- On the whole board
- Shift the resonances
- Work at lower frequency (depends on the resonance of de-cap)

With capacitors 10nF/1nH/1mOhm
## 20-H Rule vs. Edge Radiation

<table>
<thead>
<tr>
<th>Resonance Mode</th>
<th>Frequency (MHz)</th>
<th>Radiated E-Field (0H)</th>
<th>Radiated E-Field (20H)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TM(_{01})</td>
<td>940</td>
<td>102.7dB</td>
<td>108.1dB</td>
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<tr>
<td>TM(_{10})</td>
<td>1490</td>
<td>110.9dB</td>
<td>115.9dB</td>
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<tr>
<td>TM(_{02})</td>
<td>1640</td>
<td>101.2dB</td>
<td>103.6dB</td>
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<td>TM(_{11})</td>
<td>1840</td>
<td>107.6dB</td>
<td>113.1dB</td>
</tr>
</tbody>
</table>

Without capacitors (only 20-H rule)

Key Parameters of Edge Radiation

- **Cavity Model**

\[
Z_{ij} = j \omega \mu h \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \chi_{mn} \cos(k_{xm} x_i) \cos(k_{yn} y_i) \cos(k_{xm} x_j) \cos(k_{yn} y_j)
\]

\[
\times \frac{1}{ab} \frac{\cos(k_{xm} \Delta x_i/2\pi) \cos(k_{yn} \Delta y_i/2\pi)}{(k_{xm}^2 + k_{yn}^2 + \gamma^2)}
\]

\[
\times \frac{1}{\varepsilon} \frac{\cos(k_{xm} \Delta x_j/2\pi) \cos(k_{yn} \Delta y_j/2\pi)}{(k_{xm}^2 + k_{yn}^2 + \gamma^2)}
\]

\[
\propto h
\]

\[
\propto f
\]

- **Radiation field**

\[
\vec{E}_{rad} = -\frac{1}{\varepsilon} \nabla \times \vec{F} = -\frac{1}{\varepsilon} \nabla \times \left( \frac{\mu h}{4\pi} \int_C \left( -n \times \frac{1}{h} Z_{ij} \cdot I_0(x',y') \right) e^{-j\omega R} ds' \right)
\]

\[
\propto h
\]

\[
\propto f^2
\]
Radiation Model of Three-Layer Structure

- Mode decomposition – even- and odd-mode.
- Array factor.

\[
AF = \begin{cases} 
    jk_0 h \cos \theta, & \text{for even mode} \\
    2, & \text{for odd mode}
\end{cases}
\]
Even- and Odd-Mode Radiation and Attenuation Factor

- With sufficient shorting vias, odd-mode excitation can be greatly reduced.

- Ratio of even-mode and odd-mode radiation is given by an attenuation factor:

- For example, EMI suppression of 20dB from dc to 3GHz $\Rightarrow$ layer height $h < 3.1$mm so that $A < 0.1$ for all $\theta$.

$$A = \left| \frac{E_{\text{rad, even}}}{E_{\text{rad, odd}}} \right| = A_{\text{ideal}} \cos \theta; \quad A_{\text{ideal}} = \frac{1}{2} k_0 h$$
Simplification of GPG Structure with Shorting Vias

- Via stitched three-layer structure with odd-mode excitation can be simplified to a two-layer structure with shorting vias.

Even Mode Excitation

 Canonical problem

Source

Shorting vias

$E_{\text{inc}}$

$P$

$D$

$PMC$

$h$

$z$

$y$

$P$

$D$

$PMC$

$h$

$D$

$y$

$z$

$V$

$E_{\text{inc}}$

$T$

$E_{\text{inc}}$

$M$
Scattering Field Analysis in Canonical Problem

- Incident wave is from the left side of canonical problem

\[ E_z^+ = -j\omega \mu I_{via} \cdot \frac{1}{4j} H_0^{(2)}(k\rho) \]

- Boundary condition: total E-field should be zero at the via

\[ E_z^{tot}(x, y) = E_{inc} e^{-j k x} + E_{inc} e^{j k x} + E_z^s(x, y) \]

\[ = 2E_{inc} \cos kx - j\omega \mu I_{via} \cdot \left[ g(x + D, y) + g(x - D, y) \right] \]

- The odd-mode suppression factor \( A_{\text{odd}} \):

\[ A_{\text{odd}} \equiv \frac{E_{z,\text{max}}^{\text{total}}(0, y)}{E_{z,\text{max}}^{\text{total}}(0, 0)} = \frac{E_z^{\text{total}}(0, 0)}{E_{inc}} \]

\[ = 2 - 2 \cos(kD - kr) \cdot \left( \frac{2g(D, 0)}{g(r, \frac{p}{2}) + g(2D - r, \frac{p}{2})} \right) \]

Design Procedure for Shorting Vias

- Weighting: \( kP > kD \approx kr \) (\( kD < \pi/2 \))
- Design from low importance to high importance
- Choose 1mm for example

- Step 1: Determine the distance \( D \) from edge to shorting via
  - Maximum E-field suppression when \( kD = 0.15 \sim 0.6 \)
  - Choose \( kD = 0.15 \), \( D \approx 1.138 \text{mm} @ 3\text{GHz} \)

- Step 3: Determine radius “\( r \)”
  - \( kr \) given by PCB factory
  - Suppose \( kr = 0.02 \), \( r \approx 151.7 \text{um} @ 3\text{GHz} \)

- Step 4: Choose the via pitch \( P \) by \( A_{odd} \)
  - Use the design chart
  - Find corresponding \( kP = 0.287 \)
  - For 3GHz, \( P \approx 2.178 \text{mm} \)
**Measurement Environment**

- GTEM cell (GHz Transverse Electromagnetic Cell)
- Function generator—SG-hp83650B (10MHz-50GHz)
- Spectrum analyzer—R&S FSP (9kHz-40GHz)
Measurement Results with Shorting Vias

Three-Layer Radiation with Vias Comparison

Simulation Data (HFSS)
Measurement Data
(P = 2.178mm, D = 1.138mm, r = 6mil)
Simulation Data (without vias))

\[ P_{inc} = P_{meas} \times \frac{|Z_0 + Z_{11}|^2}{8Z_0} \cdot \frac{|I_{inc}|^2}{P_{in}} \]

h = 1mm
\( \varepsilon_r = 4.4 \)
(70,70)

Cross View

Top View
Applications to Next Generation DRAM @ 3DIC
Chip and Package Stacking

Wirebonded Stacking (ChipPac, 2002)

Flip-chip Stacking (Amkor)

Embedded IC Stacking (IMEC & Fujitsu, 2001)

Package-On-Package (POP)

Package-In-Package (PIP)

Folded Stackable Chip Scale Package (FSCSP)

PoP

Vertical 3D-IC

Single-die Flip-chip

Flip-chip MCM

Interposer

Fan-In WLP

Fan-Out WLP
Next Generation DRAM

- Wide IO II / LPDDR4
- High-bandwidth and low-power DRAM
- Thin and compact: 3D integration
- Wafer level packaging (WLP) 3D-IC
  - Integrated Fan-Out in TSMC.
  - Cost-effective technique for 3D-IC.
  - Vertical interconnect of through InFO via between stacked chips.
  - Thinner
  - Lower loss on molding compound and routing area but longer interconnect.
  - Better thermal.

<table>
<thead>
<tr>
<th></th>
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<tbody>
<tr>
<td>LPDDR2 1.2V/1.2V</td>
<td></td>
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<tr>
<td>LPDDR3 1.2V/1.2V</td>
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<tr>
<td>LPDDR4</td>
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<tr>
<td>Wide-IO and Wide-IO 2</td>
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<tr>
<th>Speed</th>
<th>2010</th>
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<th>2014</th>
<th>2015</th>
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<tr>
<td>6.4GB/s</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>8.5GB/s</td>
<td></td>
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<tr>
<td>12.8GB/s</td>
<td></td>
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<tr>
<td>Up to 68GB/s</td>
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<tbody>
<tr>
<td>2Gb</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>4Gb</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>8Gb</td>
<td></td>
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<thead>
<tr>
<th>PKG</th>
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<th></th>
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<tbody>
<tr>
<td>Up to 4 die stacks : 1.0mm -&gt; 0.9mm and below</td>
<td></td>
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<td></td>
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<td></td>
</tr>
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</table>
**Bandwidth of Mobile DRAM**

- Bandwidth per die for LPDDR4: \(3.2\text{Gbps} \times 32 \frac{\text{IO}}{\text{die}} \times \frac{1 \text{Byte}}{8 \text{bits}} = 12.8\text{GBps}\)
- \(68\text{GBps} \rightarrow 4\) stacked dies with 4266Mbps/IO

<table>
<thead>
<tr>
<th></th>
<th>LPDDR3 &amp; LPDDR3E</th>
<th>LPDDR4</th>
<th>Wide IO2</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Die Organization</strong></td>
<td>1ch X 8 banks X 32 IO</td>
<td>2ch X 8 banks X 16 IO</td>
<td>4ch X 8 banks X 64 IO</td>
</tr>
<tr>
<td><strong>Channel #</strong></td>
<td>1</td>
<td>2</td>
<td>4 &amp; 8</td>
</tr>
<tr>
<td><strong>Bank #</strong></td>
<td>8</td>
<td>8 per channel (16 per die)</td>
<td>32 per die</td>
</tr>
<tr>
<td><strong>Density</strong></td>
<td>4Gb – 32Gb</td>
<td>4Gb – 32Gb</td>
<td>8Gb – 32Gb</td>
</tr>
<tr>
<td><strong>Page Size</strong></td>
<td>4KByte</td>
<td>2KByte</td>
<td>4KByte (4ch die), 2K (8ch die)</td>
</tr>
<tr>
<td><strong>Max BW per die</strong></td>
<td>6.4GB/s, 8.5GB/s (overclocking)</td>
<td>12.8GB/s, 17GB/s (overclocking)</td>
<td>25.6GB/s &amp; 51.2GB/s</td>
</tr>
<tr>
<td><strong>Max IO Speed</strong></td>
<td>2133Mbps</td>
<td>4266Mbps</td>
<td>1066Mbps</td>
</tr>
<tr>
<td><strong>Signal Pin #</strong></td>
<td>62 per die</td>
<td>66 per die</td>
<td>~430 per die (4ch die), ~850 per die (8ch die)</td>
</tr>
<tr>
<td><strong>Package</strong></td>
<td>POP, MCP</td>
<td>POP, MCP</td>
<td>KGD,</td>
</tr>
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</table>
# Next Generation Mobile DRAM Using 3DIC

<table>
<thead>
<tr>
<th>Type</th>
<th>Wide IO II</th>
<th>LPDDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip photo</td>
<td><img src="image" alt="Chip photo" /></td>
<td><img src="image" alt="Chip photo" /></td>
</tr>
<tr>
<td>Pin amounts</td>
<td>~430 per die (4ch die)</td>
<td>66 per die</td>
</tr>
<tr>
<td>Signaling speed</td>
<td>Max. 1066 Mpbs</td>
<td>Max. 4266 Mpbs</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>Up to 68 GBps</td>
<td>Up to 34 GBps</td>
</tr>
<tr>
<td>Package</td>
<td>TSV-based 3DIC</td>
<td>Various, WLP or PoP</td>
</tr>
<tr>
<td>Cost</td>
<td>Higher</td>
<td>Lower</td>
</tr>
<tr>
<td>Energy per Byte</td>
<td>~40mW $^{26}$</td>
<td>~60mW</td>
</tr>
</tbody>
</table>
Who Uses LPDDR4?

- Samsung galaxy S6/S6 Edge
  - Exynos 7 (Samsung 14nm FinFET) + LPDDR4
  - ePoP (embedded package on package)
  - 15mm × 15mm with 1.4mm thickness
- HTC M9
  - Qualcomm Snapdragon 810 (TSMC 20nm) + LPDDR4
  - PoP (overheat)
- Apple iPhone
  - A9 (TSMC 16nm FinFET/ Samsung 14nm FinFET) + LPDDR4
  - InFO

👍 👎
Signal/Power Integrity in 3D Packaging

- **Signal integrity**: providing the solution space and guideline for RDL routing design on InFO to meet LPDDR4 specification.
- **Power integrity**: developing and designing the decoupling capacitor for InFO power integrity.
Electrical Definition of Eye for LPDDR4

- Set the right and left bound from the requirement of Spec.
- Acquire the maximum eye width

- Set the upper and lower bound from the requirement of Spec.
- Acquire the maximum eye height

- Clear eye mask in JEDEC definition.
- Rectangular eye mask.

Bottleneck of Signal Integrity in InFO

LPDDR4 Substrate
RDL Wire-bonding 100 μm 50 μm

Micro bump TIV
Molding compound 300 μm ~ 8000 μm
RDL (Re-distribution layer)
Upper Stacked-die (LPDDR4)
Molding compound
Substrate
RDL
Lower die (AP)
Solder ball
PCB (Printed circuit board)

DK = 4, Df = 0.01
Ground
Signal 5 μm
Silicon Chip
Power

DK = 3.1, Df = 0.017
Ground
Signal 5 μm
Silicon Chip
Power

@ 2400Mbps
140mV 0.22UI

@ 3200Mbps
140mV 0.25UI

@ 4266Mbps
120mV 0.25UI
Model Construction for Lower RDL and TIV

Through InFO Via (TIV) Model

Lower RDL (AP) Model

VRM

PCB (Printed circuit board)

Model Construction for Lower RDL and TIV

Through InFO Via (TIV) Model

Lower RDL (AP) Model
Model Construction for Upper RDL and PCB

Upper RDL (DRAM) Model

- VDDQ (Power)
- DQ8_A
- DQ9_A
- DQ10_A
- DQ11_A
- VSSQ (Ground)

- 6 VSSQ
- 7 DQ8_A
- 8 VDDQ
- 9 DQ9_A
- 10 VSSQ
- 11 DQ10_A
- 12 VDDQ
- 13 DQ11_A
- 14 VSSQ

TIV

DRAM Die

PCB Power/Ground Model

- VDDQ (Power)
- VSSQ (Ground)

- 50mm
- 4 mil

PCB Power plane

InFO VRM

Ground plane

50mm

VRM

Ground plane

50mm

4 mil

PCB

Power plane
Model Connection

- $V_{\text{vic}}$ (victim) and $V_{\text{agg}}$ (aggressor) are different patterns to excite maximum crosstalk condition.
- Voltage probes are at victim (DQ10_A) and btw power/ground nets on IOs.
- Only on-chip and on-package decaps are in simulation.
Signal Integrity by Lower RTL Design

- GSSPSSG @ 2400Mbps
- GSSPSSG @ 3200Mbps
- GSSPSSG @ 4266Mbps

- GS SPS SG @ 2400Mbps
- GS SPS SG @ 3200Mbps
- GS SPS SG @ 4266Mbps

- GSPSGSPSG @ 2400Mbps
- GSPSGSPSG @ 3200Mbps
- GSPSGSPSG @ 4266Mbps

- Silicon Chip
- Ground
- Power DK = 3.1, Df = 0.017
Solution Space for DQ (GSPSGSPSG)

- Dominant factor: InFO RDL length
- Bi-directional transmission.
- Under requirement of Spec.
**Power Distribution System for InFO**

- **Power Distribution System**
  - LPDDR4 to AP
  - AP to LPDDR4
- **Improve power integrity**
  - Change layout of power bus
  - Add decoupling capacitors
- **Decoupling capacitors**
  - On-chip capacitance: without parasitic effect but small capacitance
  - Off-chip capacitance
    - On package de-cap: close to IO but small area and choice for de-cap
    - On board de-cap: the most flexible but far away from IO
**Single Node Analysis for De-caps Design**

- Impedance can be analyzed in local region.
- Two different types of parallel capacitors cause anti-resonance, ⇒ exceed the target impedance.
- At anti-resonance, series $C_1 (n_i C_i$ and $n_j C_j)$ and series $L (L_i/n_i$ and $L_j/n_j)$

$$X_i = \omega L_i - \frac{1}{\omega C_i} \rightarrow Z_i = R_i + jX_i$$
$$X_j = \omega L_j - \frac{1}{\omega C_j} \rightarrow Z_j = R_j + jX_j$$

$$f_{anti} = \frac{1}{2\pi} \sqrt{\frac{1}{\frac{C_i C_j}{C_i + C_j}(L_i + L_j)}} = \frac{1}{2\pi} \sqrt{\frac{C_i + C_j}{C_i C_j(L_j + L_i)}}$$

$$Z_{in} = \frac{1}{Z_i} + \frac{1}{Z_j} = \frac{(R_i + jX_i) \times (R_j + jX_j)}{R_i + R_j + j(X_i + X_j)}$$
De-cap Design Example

- Current drawing per IO: ~10mA
- 10% tolerance of power noise (0.44V): 0.44 x 10%
- Number of switching IO: 4
- Target impedance: 1 Ohm

① 5 various de-caps: type 3 4 6 7 10
② 2 identical de-caps: 47p + 47p
③ 2 identical de-caps: 100p + 100p
④ 1 de-cap: 100p
⑤ 1 de-cap: 4.7n
Comparison of Power Noise Signature

- As design for target impedance, the 5 de-caps case satisfies the 10% noise requirement.

![Graphs showing power noise signature comparison](image)

- **Only 1pF on-chip capacitance**
  - 210mV
- **4.7n decap**
  - 53mV
- **100p decap**
  - 48mV

- **47p + 47p decaps**
  - 31mV
- **100p + 100p decaps**
  - 33mV

\[ L_{P1} = 2.03nH, C_{P1} = 0.35pF \]

*for 8mm power line*
DQ Eye-Diagram Comparison @ 4266MHz

<table>
<thead>
<tr>
<th></th>
<th>EW</th>
<th>EH</th>
</tr>
</thead>
<tbody>
<tr>
<td>Only on-chip cap</td>
<td>Out of Spec.</td>
<td></td>
</tr>
<tr>
<td>4.7n</td>
<td>0.34UI</td>
<td>192mV</td>
</tr>
<tr>
<td>100p</td>
<td>0.34UI</td>
<td>193mV</td>
</tr>
<tr>
<td>47p + 47p</td>
<td>0.35UI</td>
<td>208mV</td>
</tr>
<tr>
<td>100p + 100p</td>
<td>0.35UI</td>
<td>208mV</td>
</tr>
</tbody>
</table>
DQ Eye-Diagram Comparison @ 4266MHz
Using 100pF Decap and Different ESL

Ideal power

Only on-chip capacitance

1nH ESL (0.667nH total)

0.4nH ESL (0.333nH total)

$L_{P1} = 2.03\, nH, \ C_{P1} = 1.05\, pF$
for 8mm power line

<table>
<thead>
<tr>
<th></th>
<th>EW</th>
<th>EH</th>
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<tbody>
<tr>
<td>Only on-chip cap</td>
<td>Out of Spec.</td>
<td></td>
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<tr>
<td>Ideal power</td>
<td>0.54UI</td>
<td>289mV</td>
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<tr>
<td>100pF+1nF ESL</td>
<td>0.40UI</td>
<td>238mV</td>
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<tr>
<td>100pF+0.4nF ESL</td>
<td>0.45UI</td>
<td>261mV</td>
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</tbody>
</table>
**PI Design by Meshed Ground/Power**

$L_{P1} = 2.03nH, C_{P1} = 1.05pF$

for 8mm power line

EW: 0.49UI
EH: 276mV
Conclusions

• Solution space is proposed and the pin assignment can meet the specification up to 4266 Mbps.
• One 100p de-cap can meet the PI requirement at 4266 Mbps. However, the large power noise will be induced when the resonant frequency is excited at IO.
• For 8mm GSPSGSPSG routing, one 100p decap with smaller than 2.1nH ESL can meet design requirement.
• Using meshed ground/power, InFO without on-package decap but with improved performance deserves further study.