Design of a RISC Processor Compatible with ARM Instructions

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OUTLINE

- Motivation
- Development of the chip
- Architecture
- Synthesis & Optimization
- Place & Route
- Simulation Results
- Conclusion

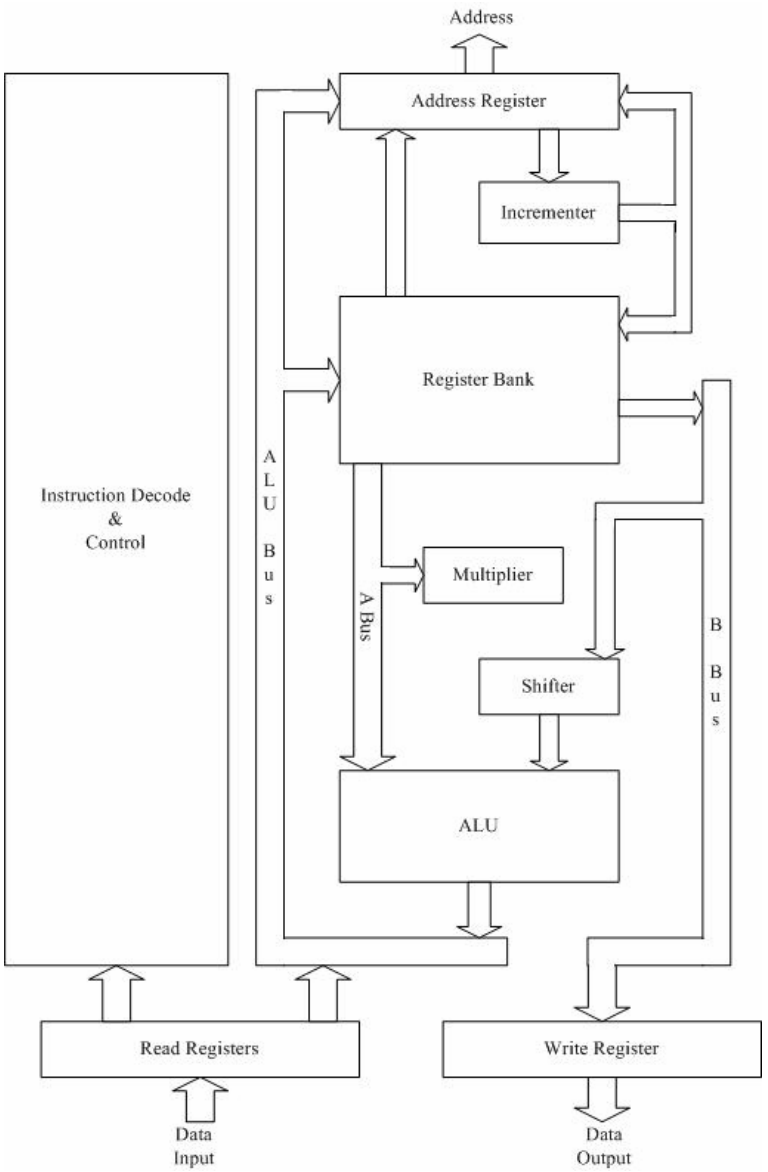
MOTIVATION

- ARM processors are frequently used in application specific integrated circuits (ASICs).
- Major applications:
  Telecommunication
  Data communication
  Portable Computing
  Automotive
  Information Systems
  Imaging

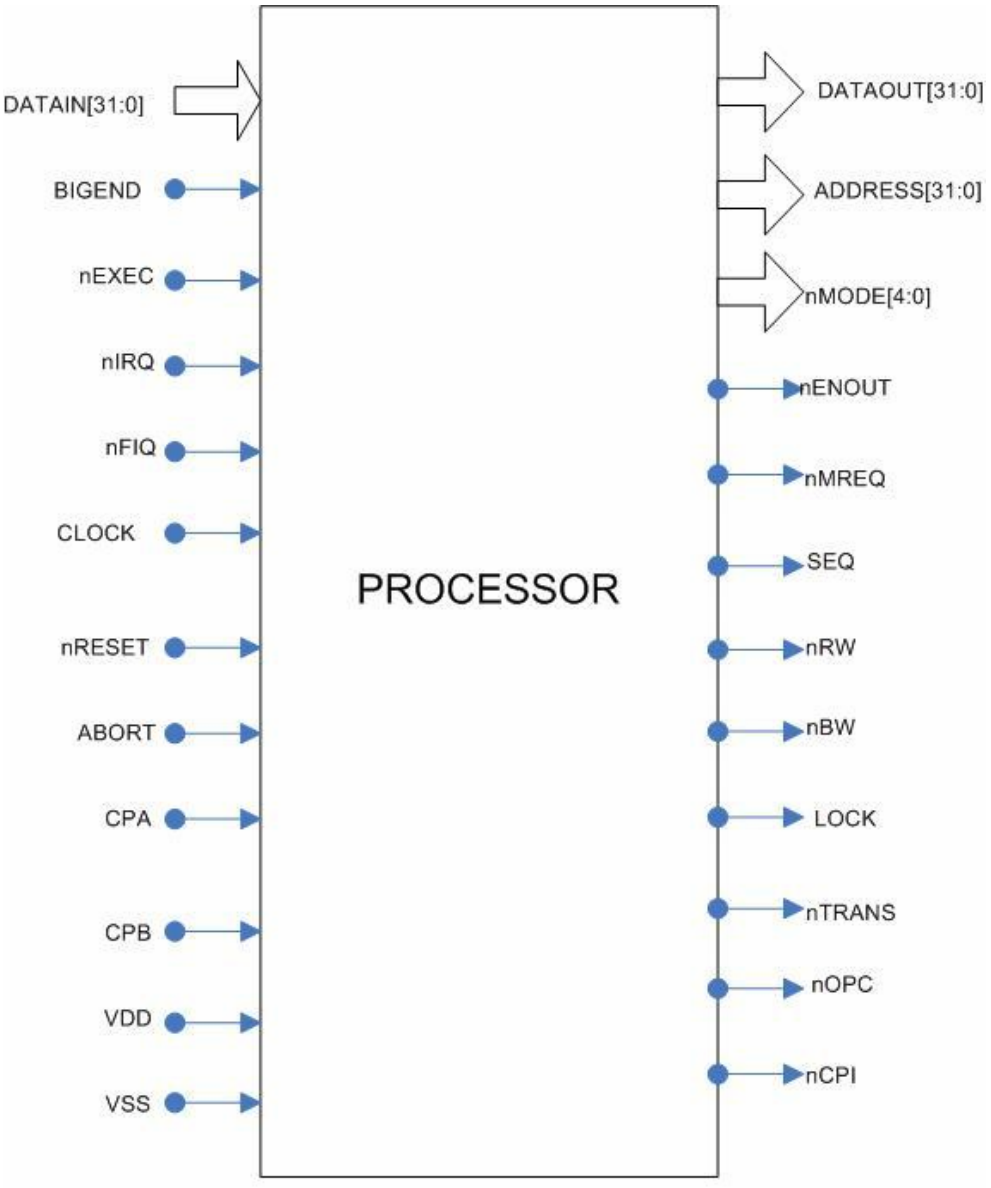
DEVELOPMENT OF THE CHIP

- Research on ARM processors
- Coding the architecture (Verilog)
- Synthesis with scan chain (Synopsys DC)
- Test pattern generation (Tetramax)
- Place & Route (Astro)
- Post layout verification (Verilog)
- DRC & LVS verification (Calibre)

ARCHITECTURE



IO Signals


DATAIN[31:0]
BIGEND
nEXEC
nIRQ
nFIQ
CLOCK
nRESET
ABORT
CPA
CPB
VDD
VSS
PROCESSOR
DATAOUT[31:0]
ADDRESS[31:0]
nMODE[4:0]
nENOUT
nMREQ
SEQ
nRW
nBW
LOCK
nTRANS
nOPC
nCPI

INSTRUCTION SET

Instruction Set is consisted of 34 instructions which can be divided into 12 groups:

- 1. Data processing
- 2. PSR (Program Status Register) transfer
- 3. Multiply
- 4. Single data swap
- 5. Single data transfer
- 6. Undefined Instruction
- 7. Block data transfer
- 8. Branch
- 9. Coprocessor data transfer
- 10. Coprocessor data operation
- 11. Coprocessor register transfer
- 12. Software interrupt

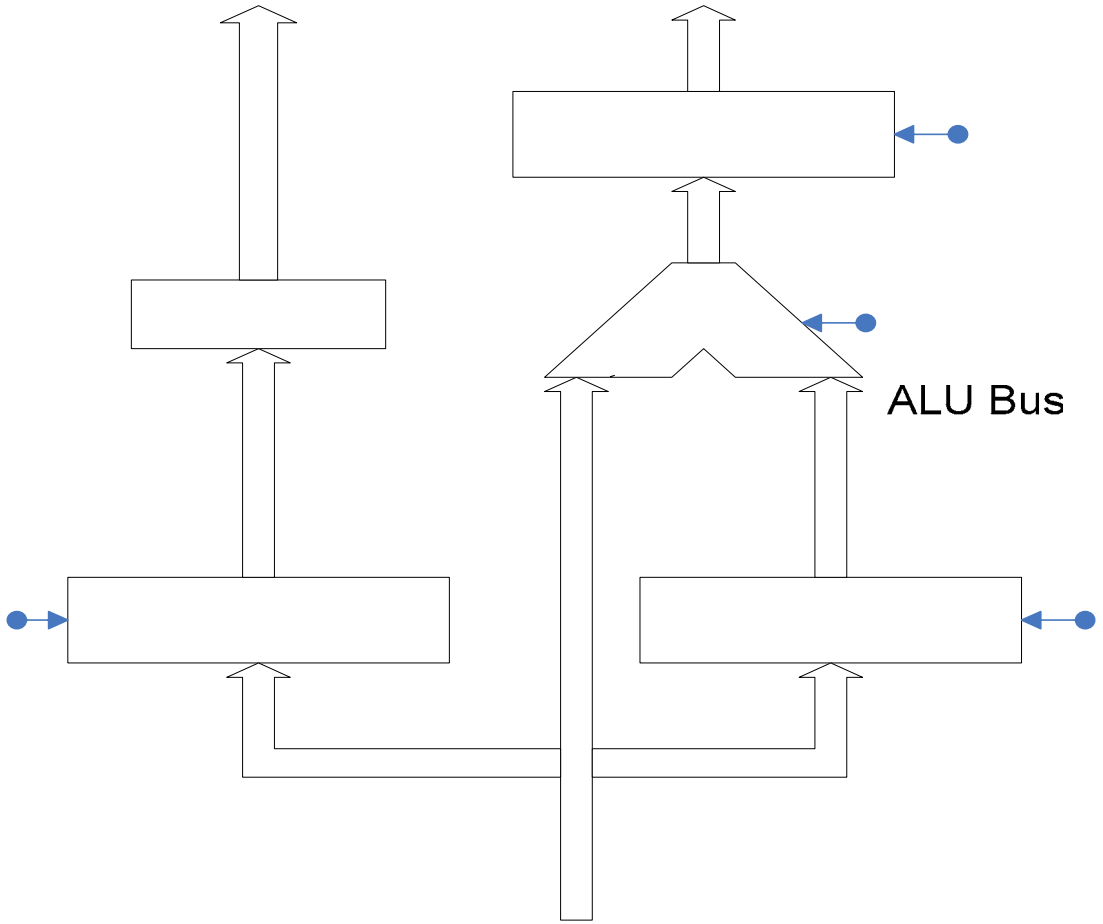
Conditional Execution

Condition Code	Mnemonic Extension	Interpretation	Needed flag state for execution
0000	EQ	Equal / equals zero	Z set
0001	NE	Not equal	Z clear
0010	CS/HS	Carry set / unsigned higher or same	C set
0011	CC/LO	Carry clear / unsigned lower	C clear
0100	MI	Minus / negative	N set
0101	PL	Plus / positive	N clear
0110	VS	Overflow	V set
0111	VC	No overflow	V clear
1000	HI	Unsigned higher	C set and Z clear
1001	LS	Unsigned lower or same	C clear or Z set
1010	GE	Signed greater than or equal	N equals V
1011	LT	Signed less than	N is not equal to V
1100	GT	Signed greater than	Z clear and N equals V
1101	LE	Signed less than or equal	Z set or N isn't equal to V
1110	AL	Always	Any
1111	NV	Never	None

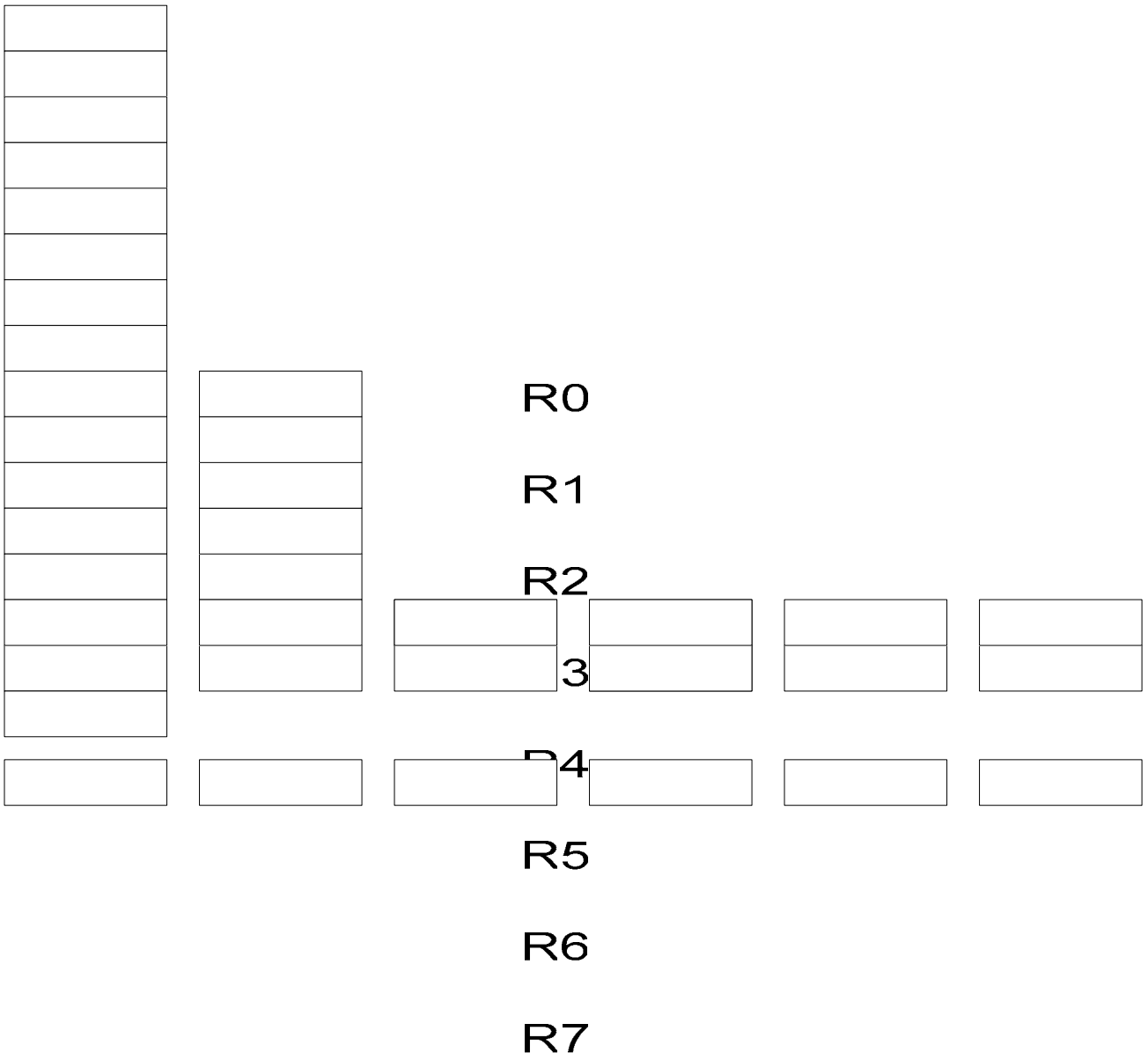
Components of the Processor

- Read registers
- Write register
- Address register
- Incrementer
- Register bank
- Multiplier
- Shifter
- ALU
- Controller

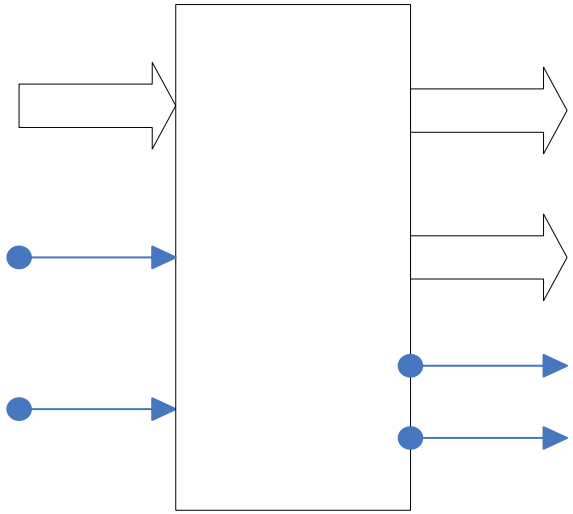
Read Registers



Register Bank



Multiplier

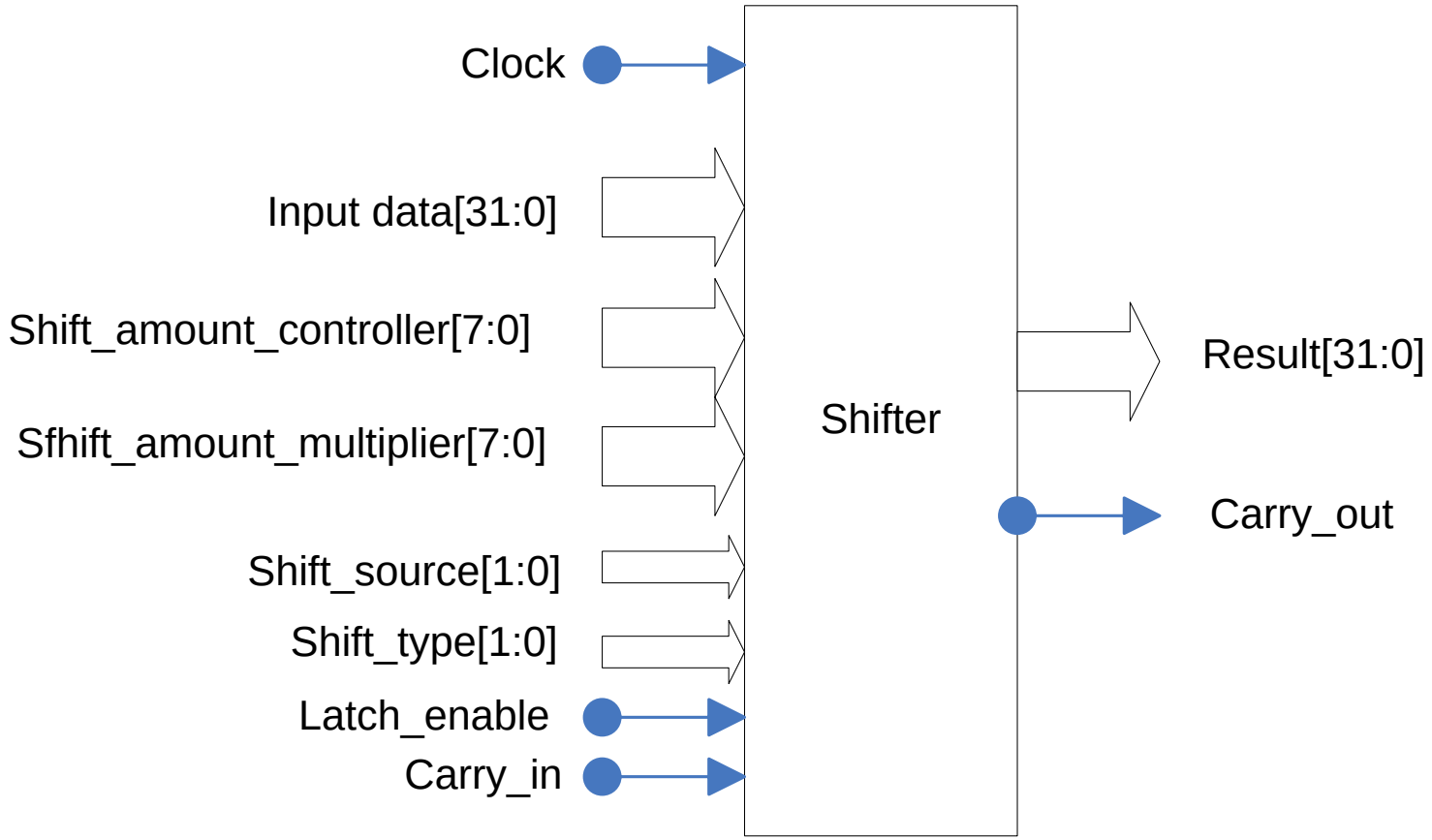


Carry In	Multiplier	Shift	ALU	Carry Out
0	0	LSL(2N)	A+0	0
0	1	LSL(2N)	A+B	0
0	2	LSL(2N+1)	A-B	1
0	3	LSL(2N)	A-B	1
1	0	LSL(2N)	A+B	0
1	1	LSL(2N+1)	A+B	0
1	2	LSL(2N)	A-B	1
1	3	LSL(2N)	A+0	1

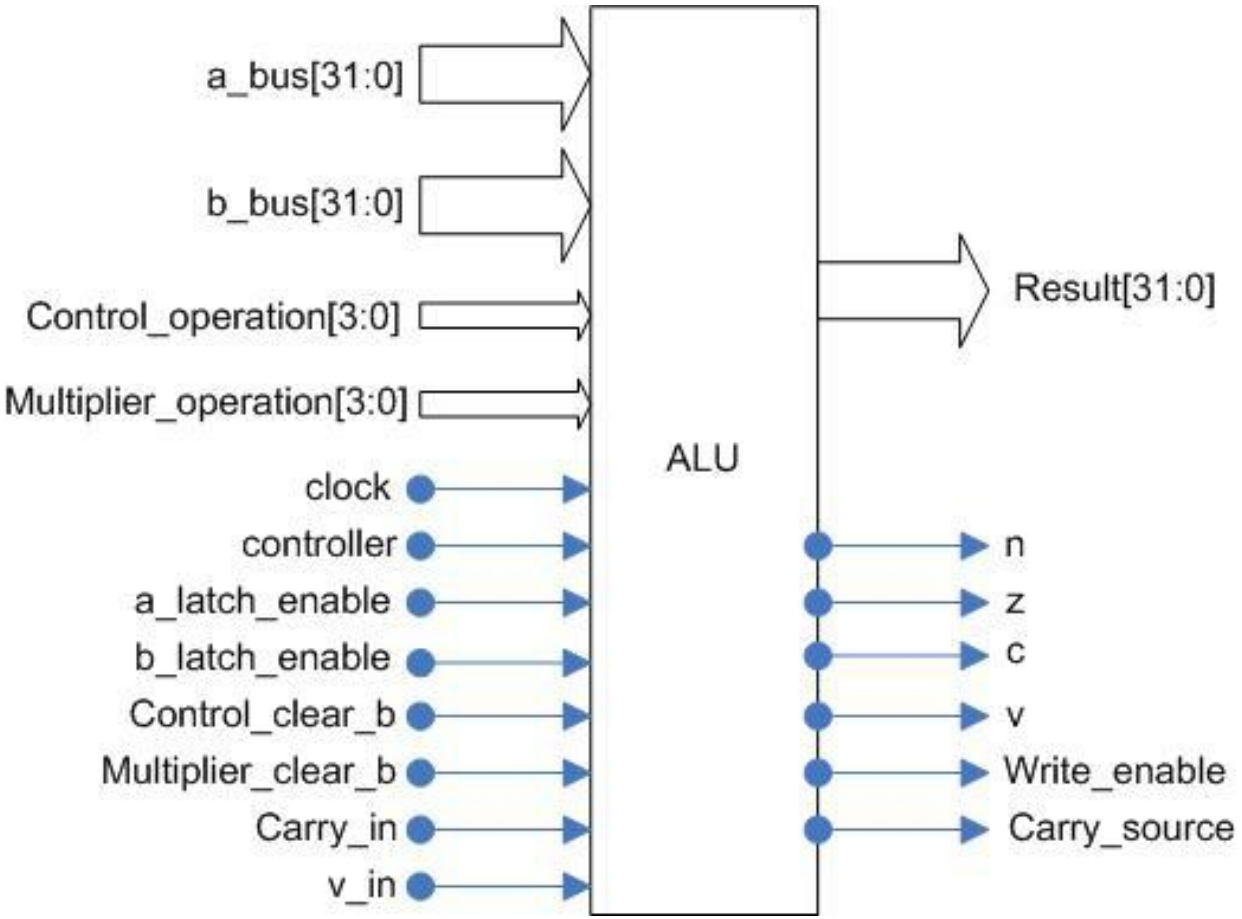
Multip

Latch_a_bus

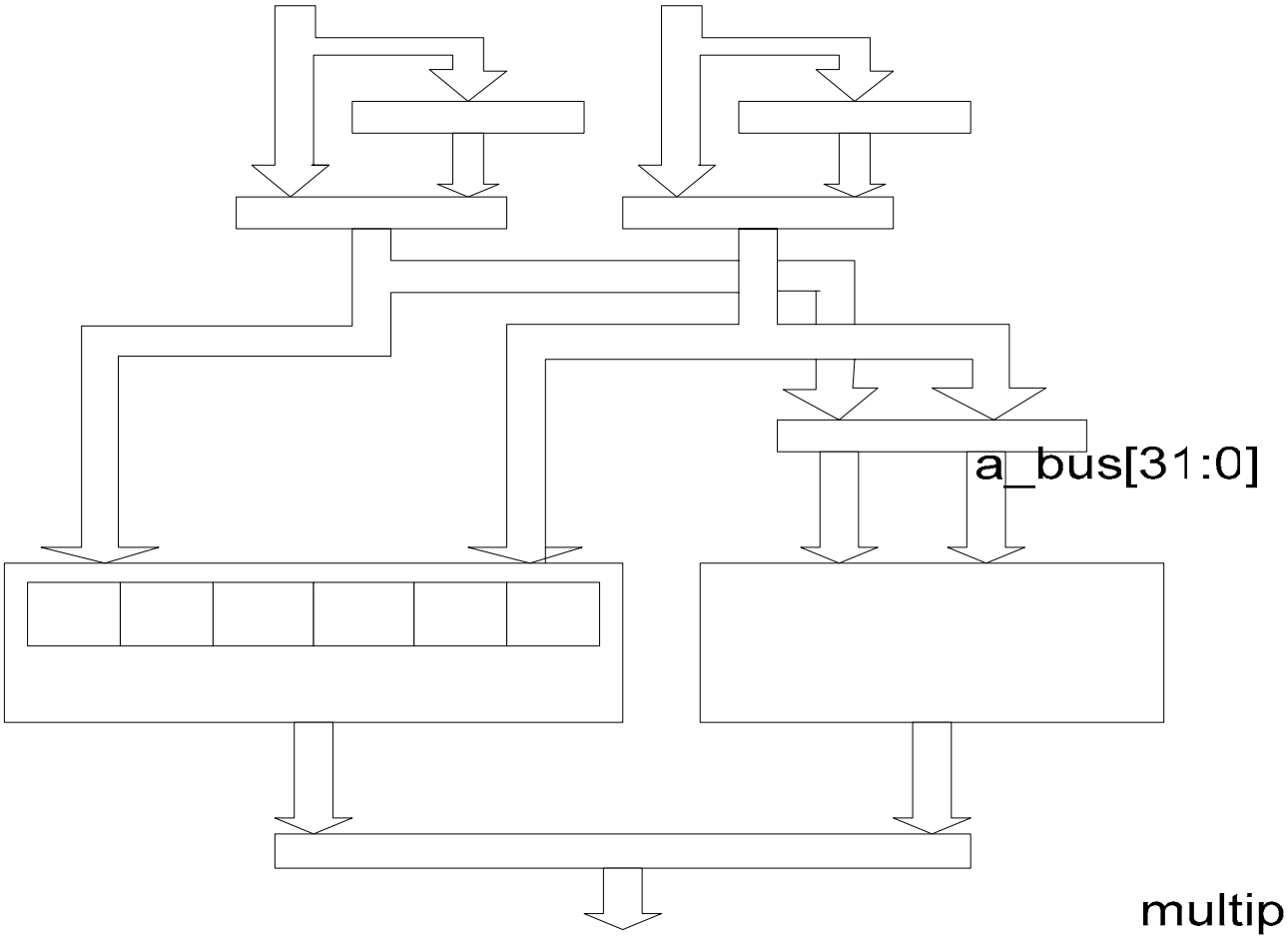
Shifter


Clock
Input data[31:0]
Shift_amount_controller[7:0]
Sfhift_amount_multiplier[7:0]
Shift_source[1:0]
Shift_type[1:0]
Latch_enable
Carry_in
Shifter
Result[31:0]
Carry_out

ALU


a_bus[31:0]
b_bus[31:0]
Control_operation[3:0]
Multiplier_operation[3:0]
clock
controller
a_latch_enable
b_latch_enable
Control_clear_b
Multiplier_clear_b
Carry_in
v_in
ALU
Result[31:0]
n
z
c
v
Write_enable
Carry_source

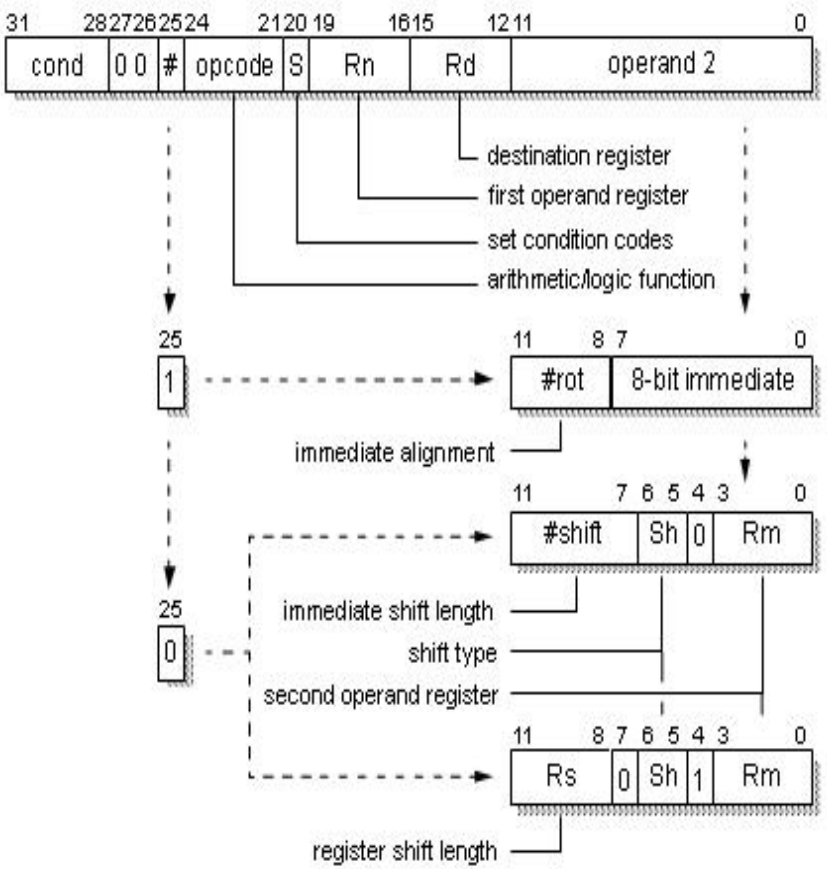
Architecture of the ALU

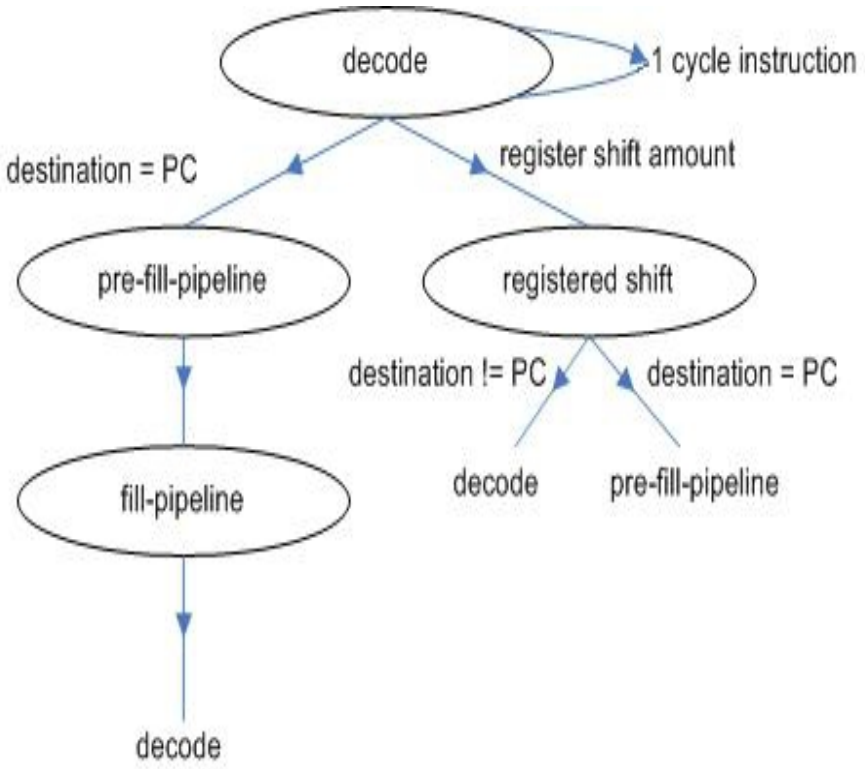


Controller

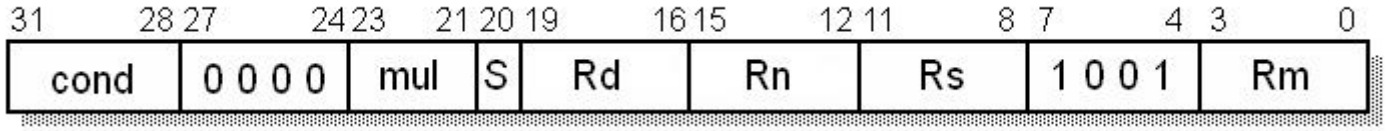
- Instruction decoding
- FSM
- Interrupt handler
- Pipeline Registers

FSM - Data Processing

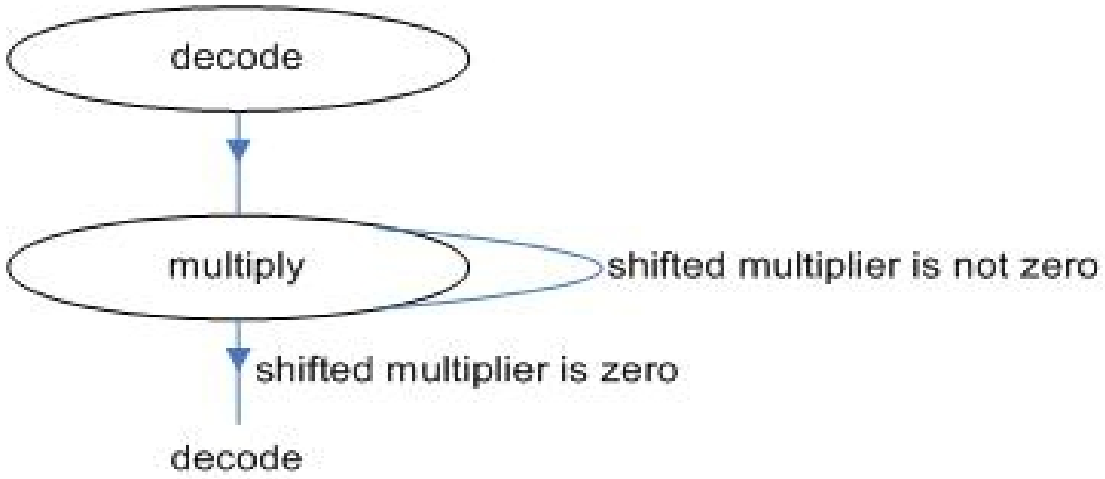




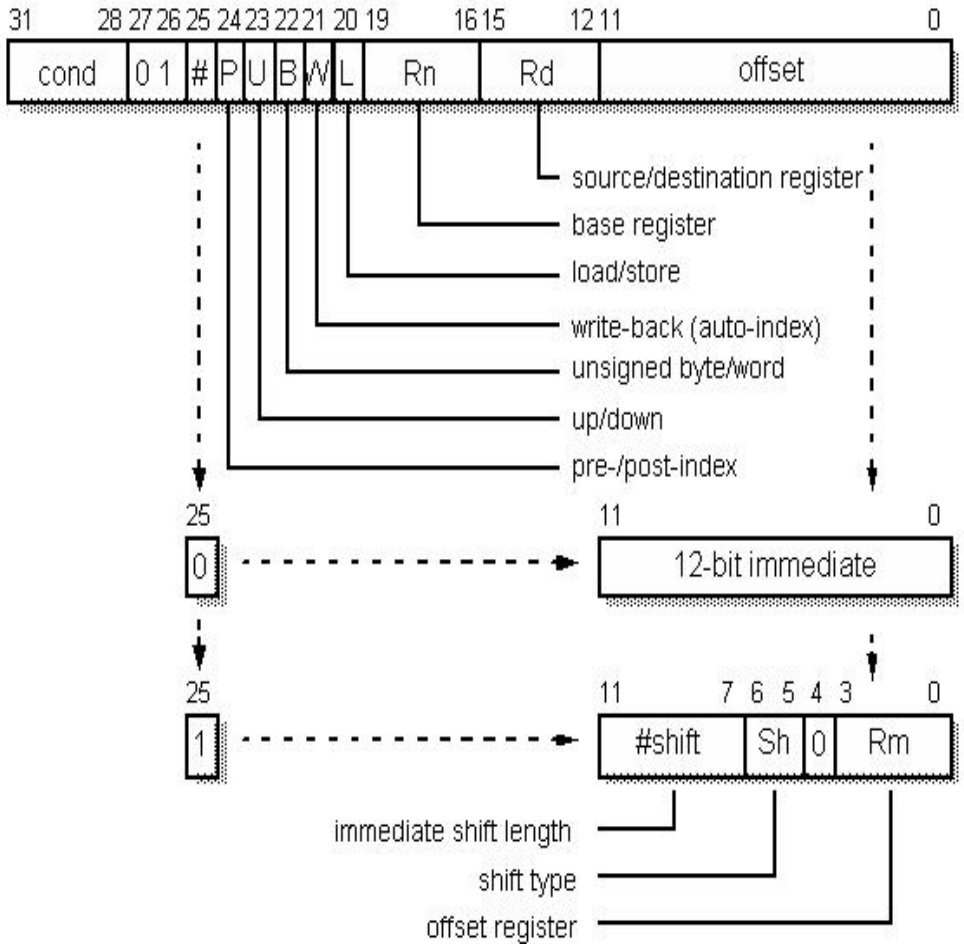
FSM - Multiply

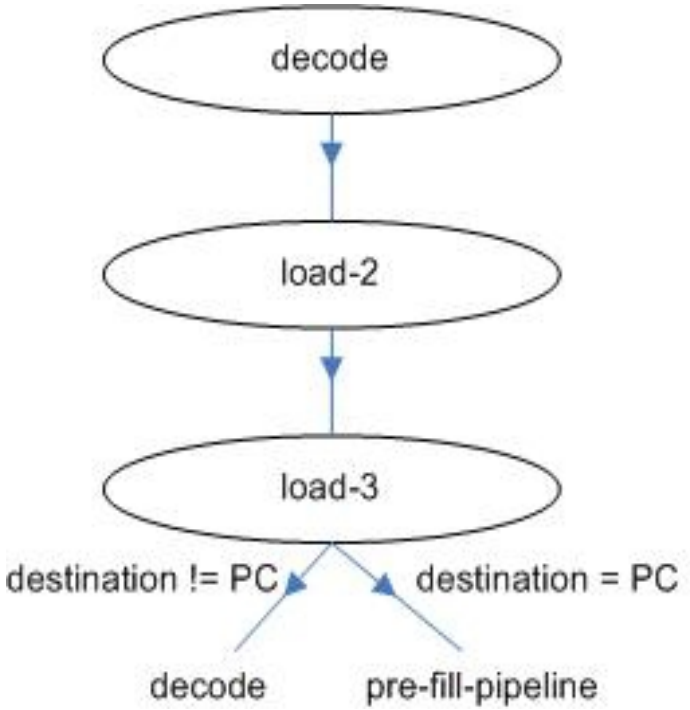


mul = 000; Rd = Rm x Rs
mul = 001; Rd = Rm x Rs + Rn

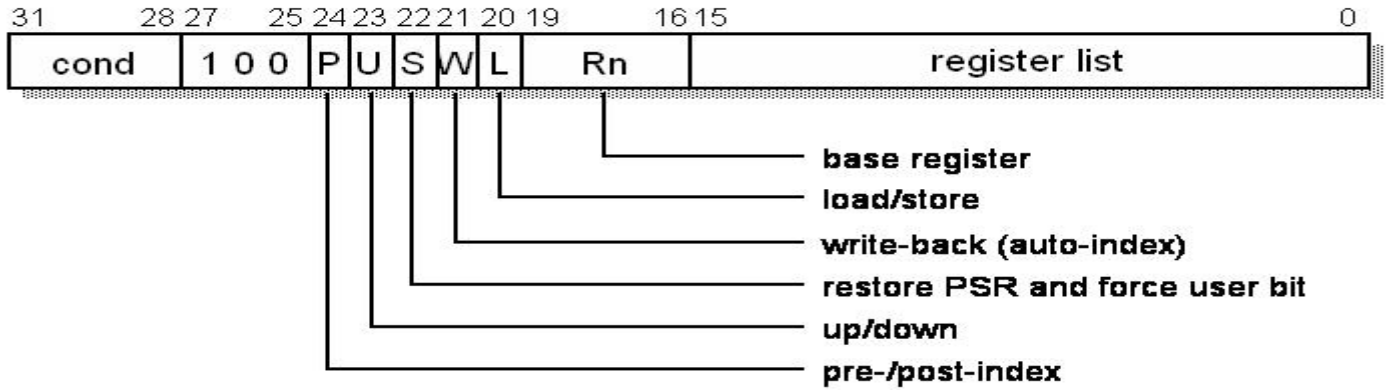


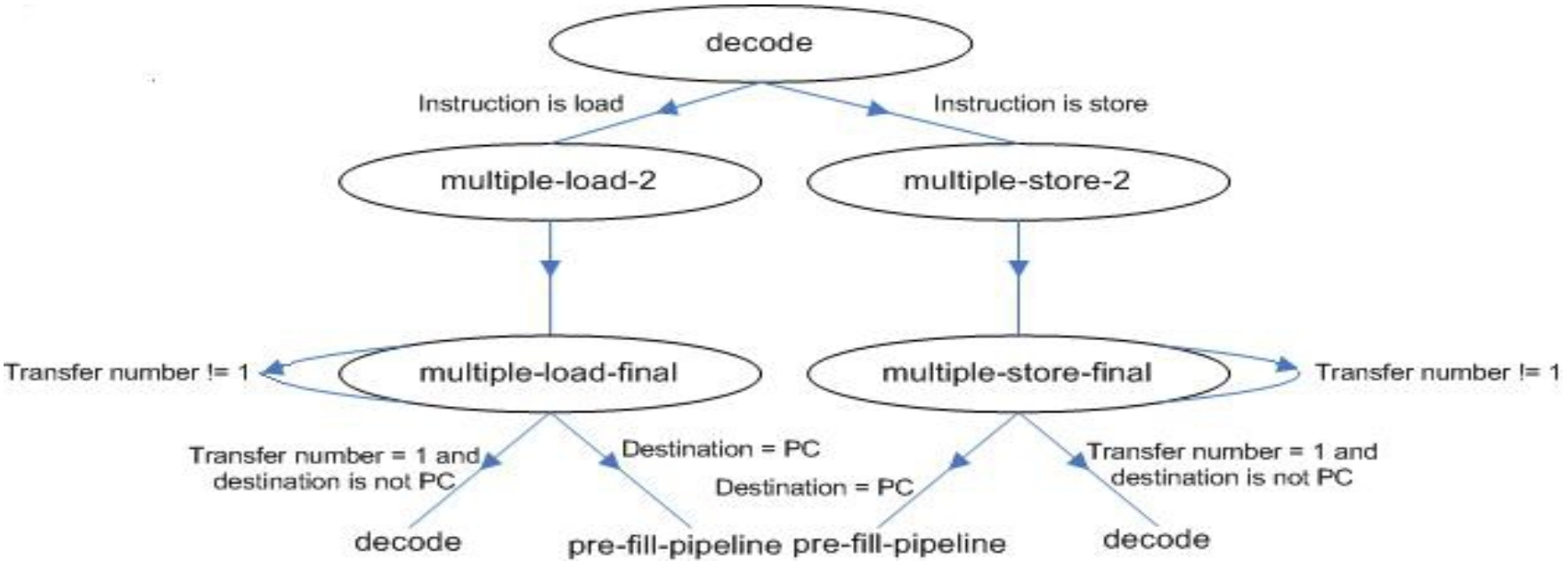
FSM – Single Load



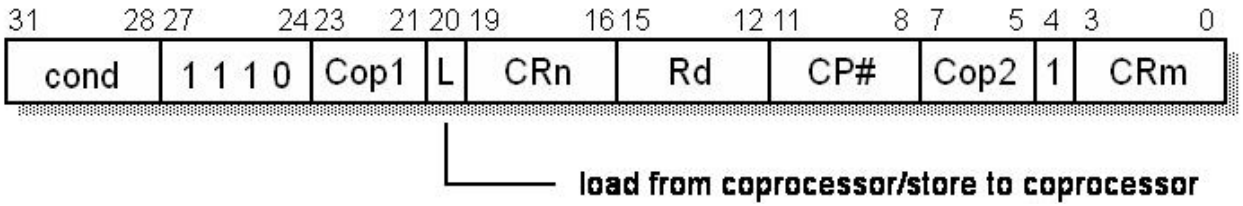


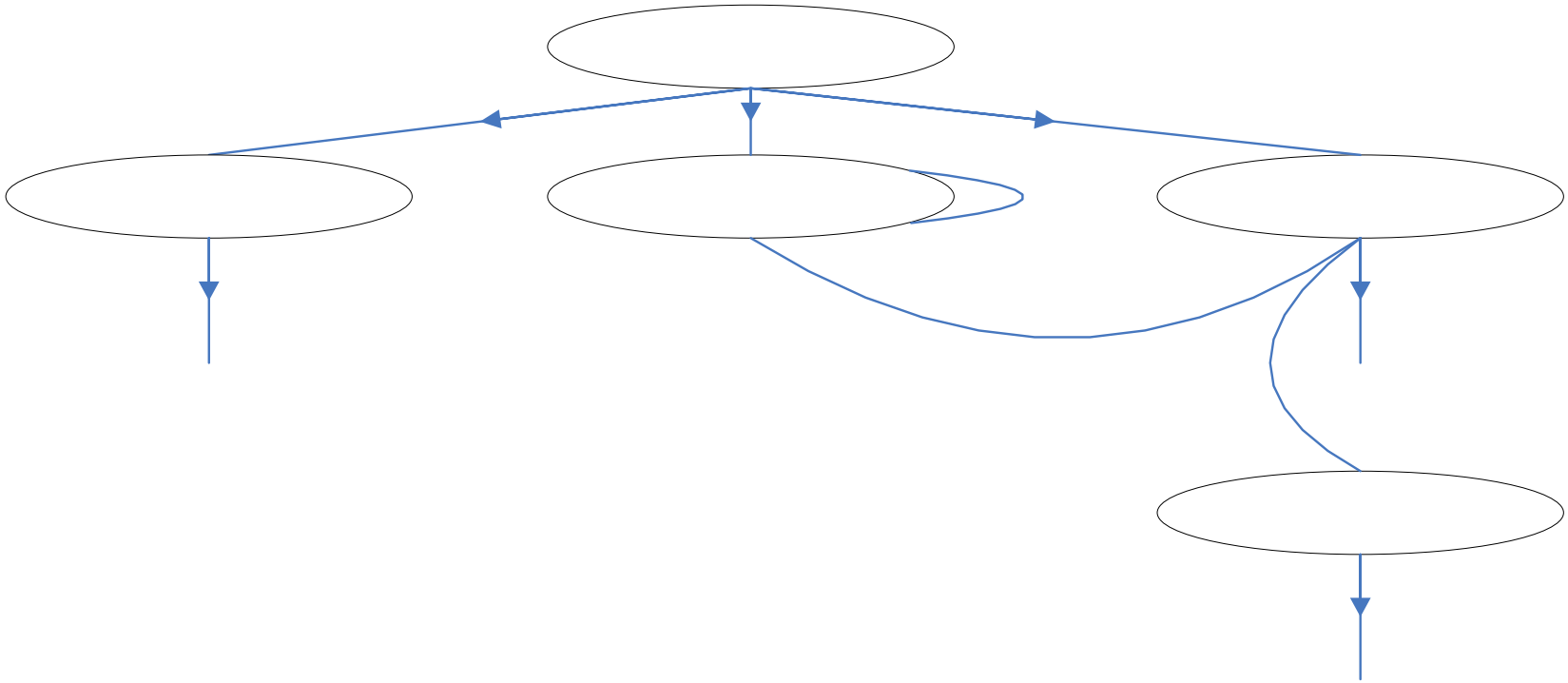
FSM – Multiple Transfer





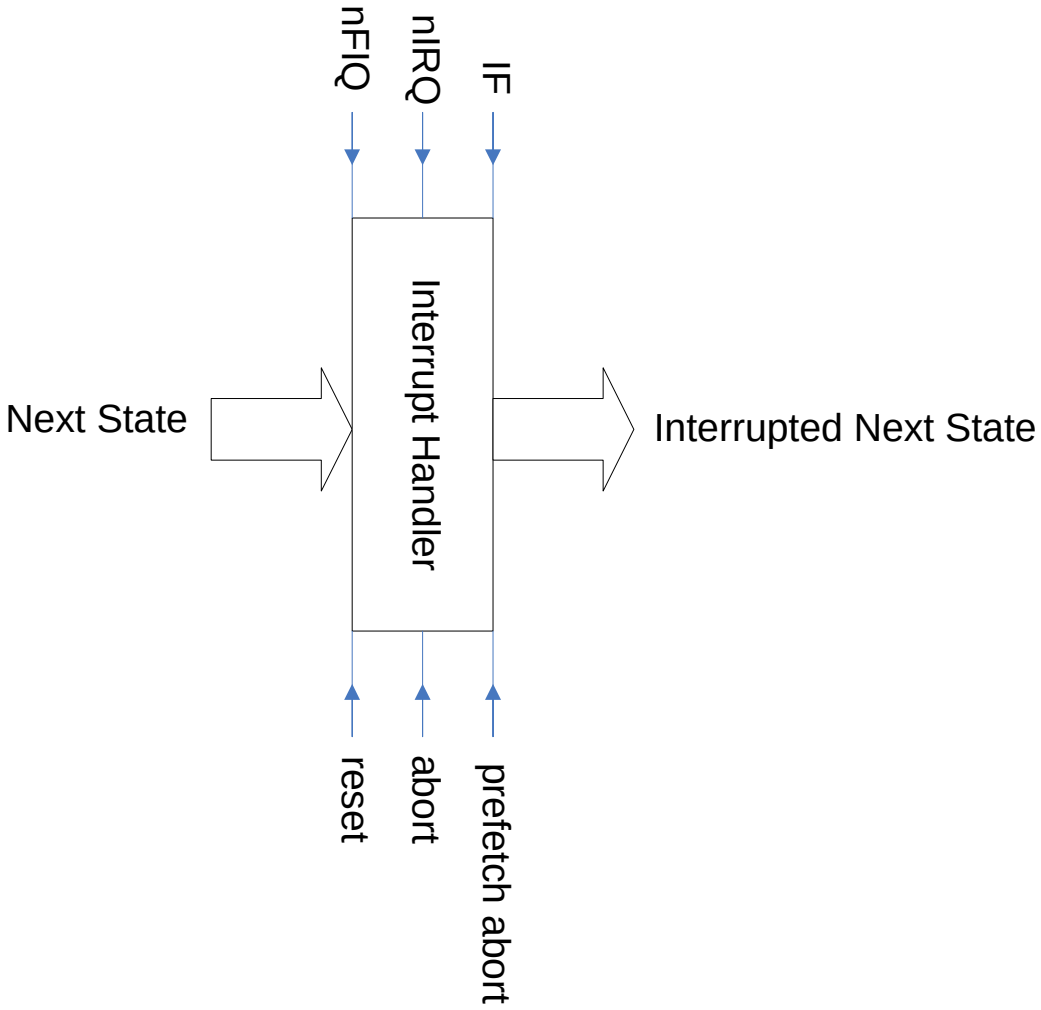
Coprocessor Register Transfer





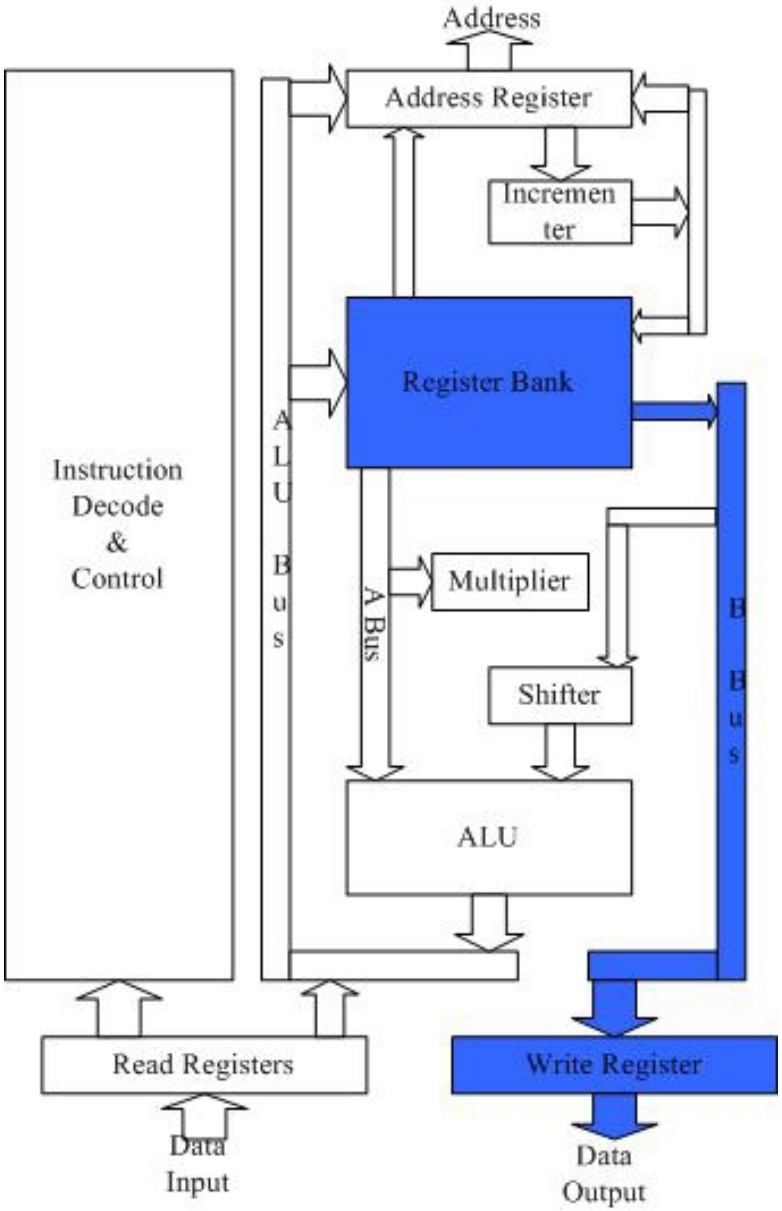
decoc

Interrupt Handler

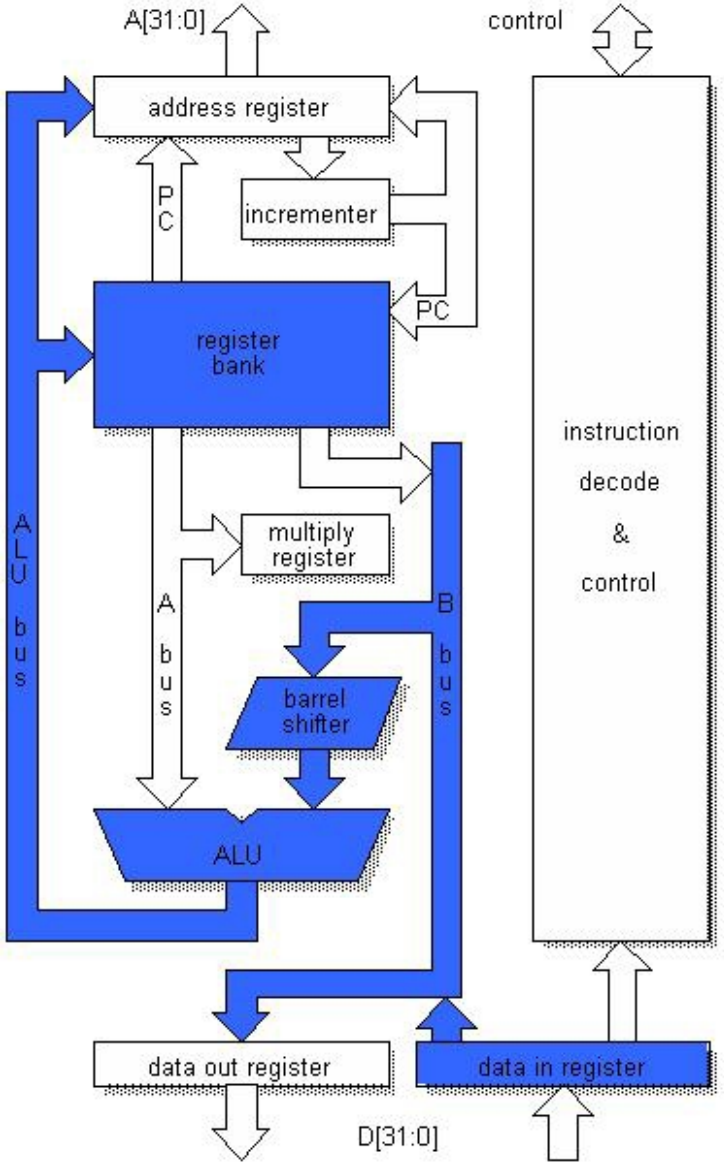


SYNTHESIS

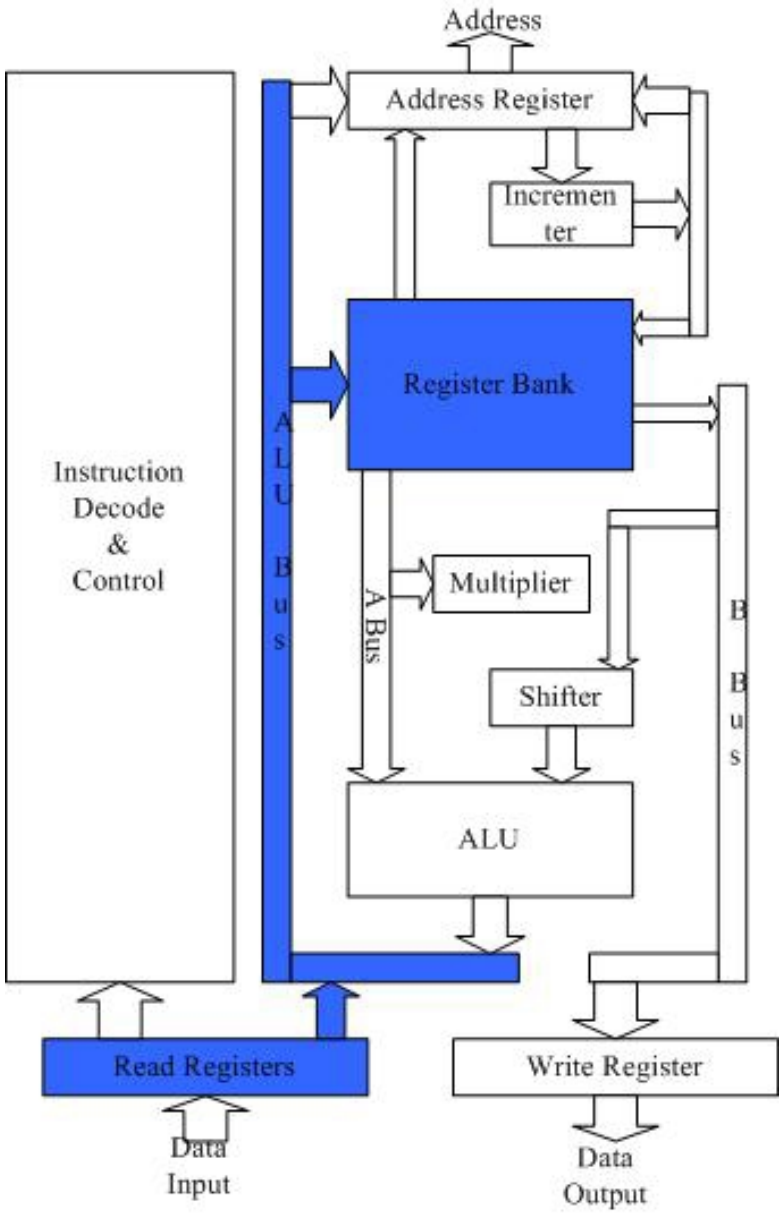
Optimization



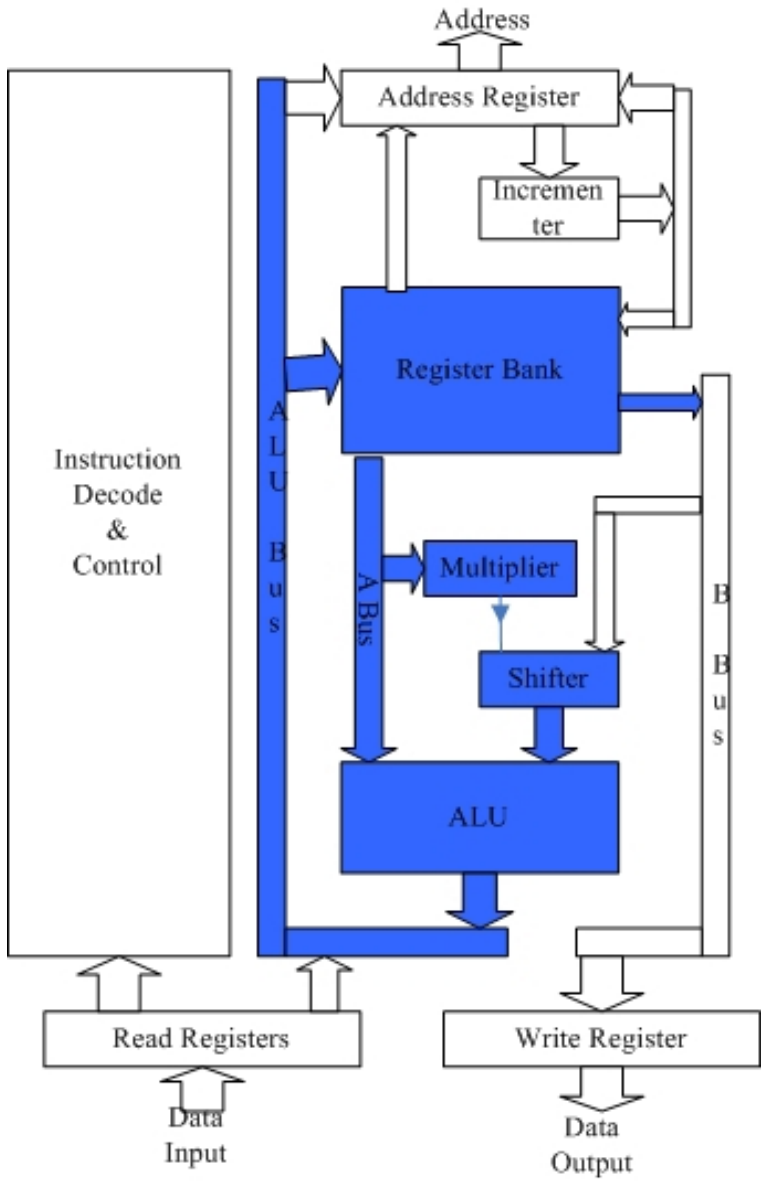
Optimization



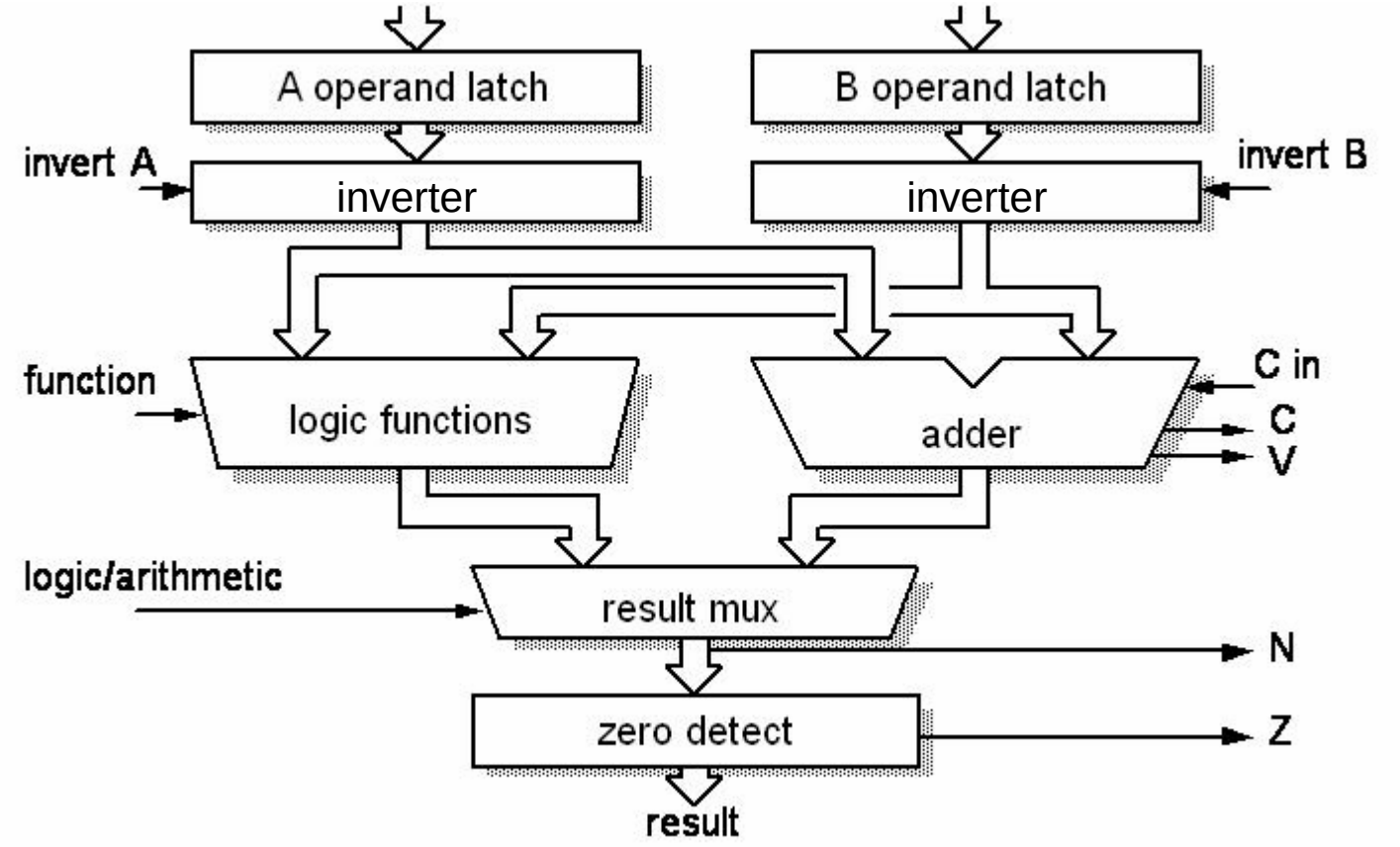
Optimization



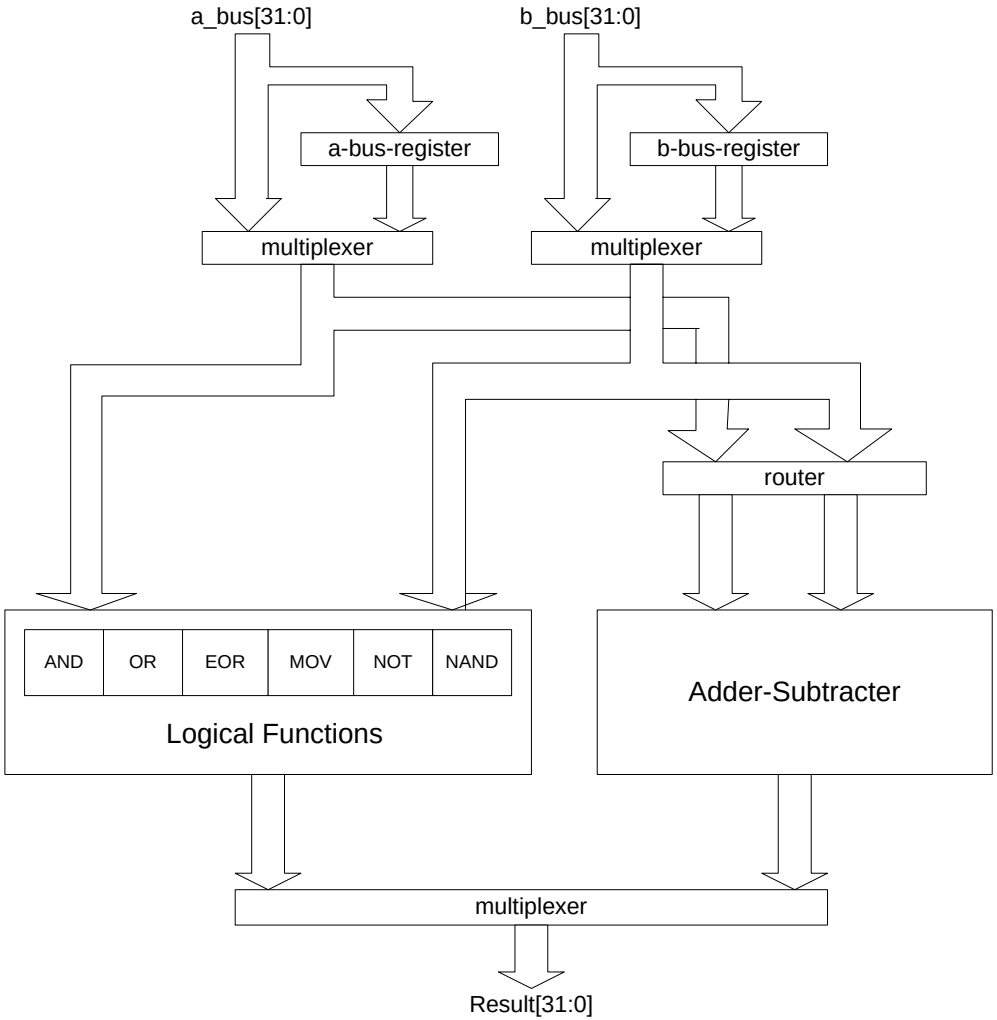
Optimization



ALU before being modified



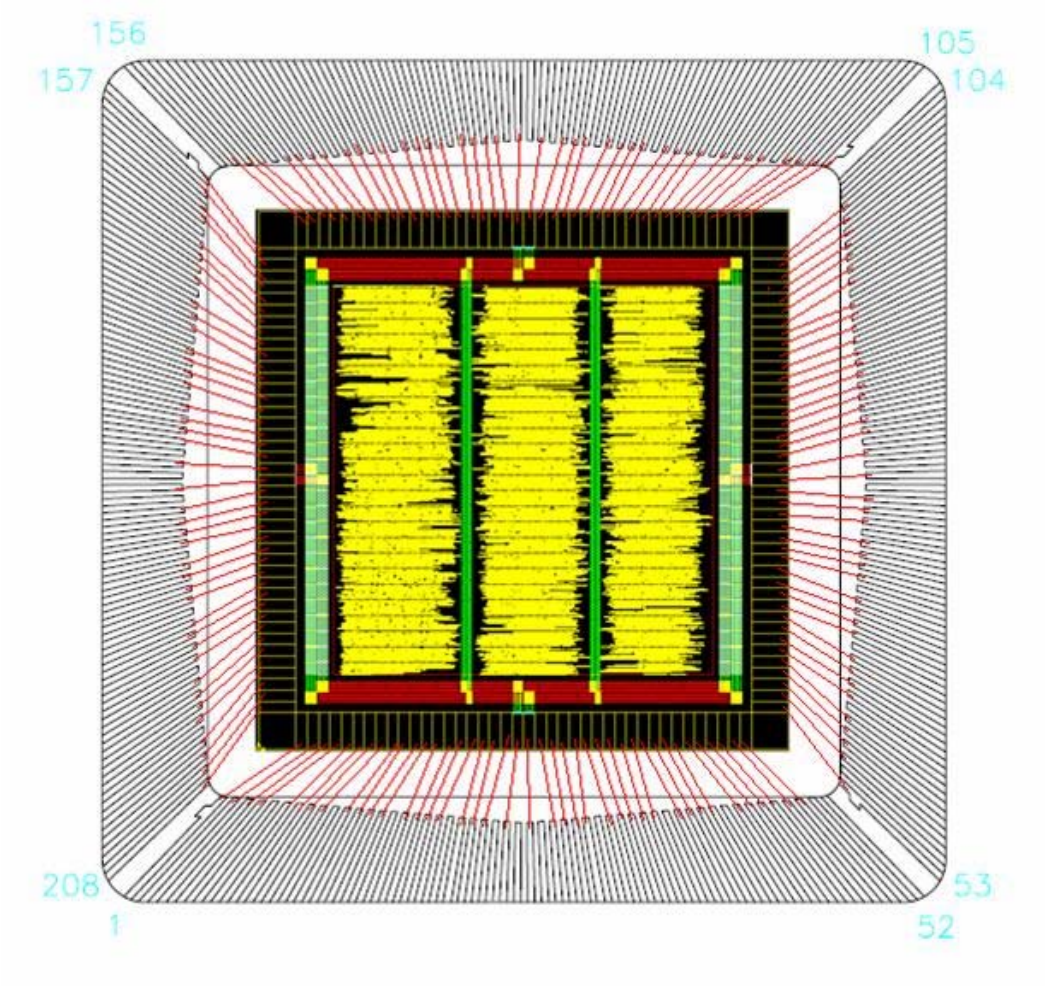
ALU after being modified



PLACE & ROUTE

- DRC has 0 error count.
- LVS check has passed.
- Post layout simulation has no timing violations.

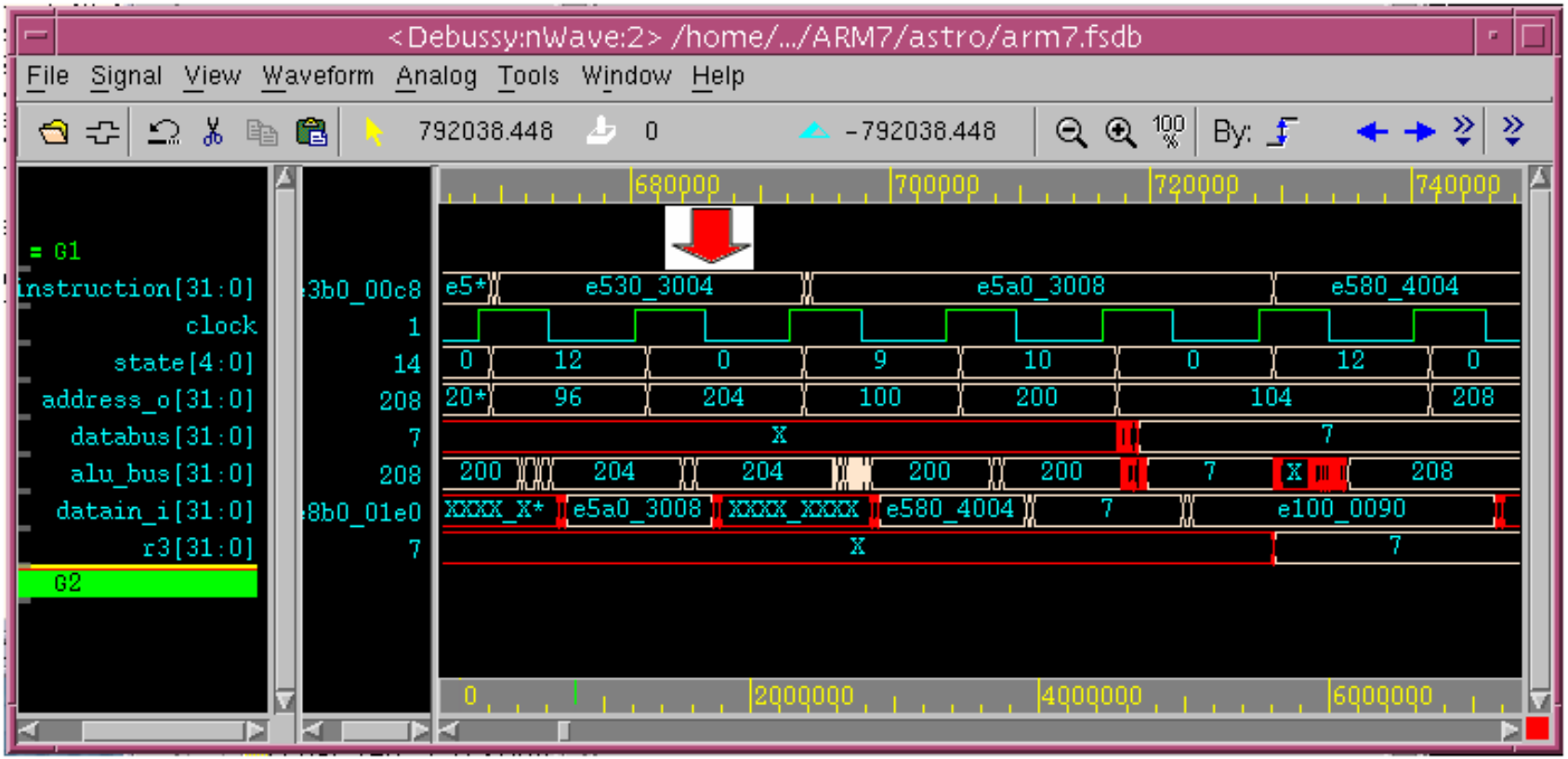
Layout with Bonding Diagram



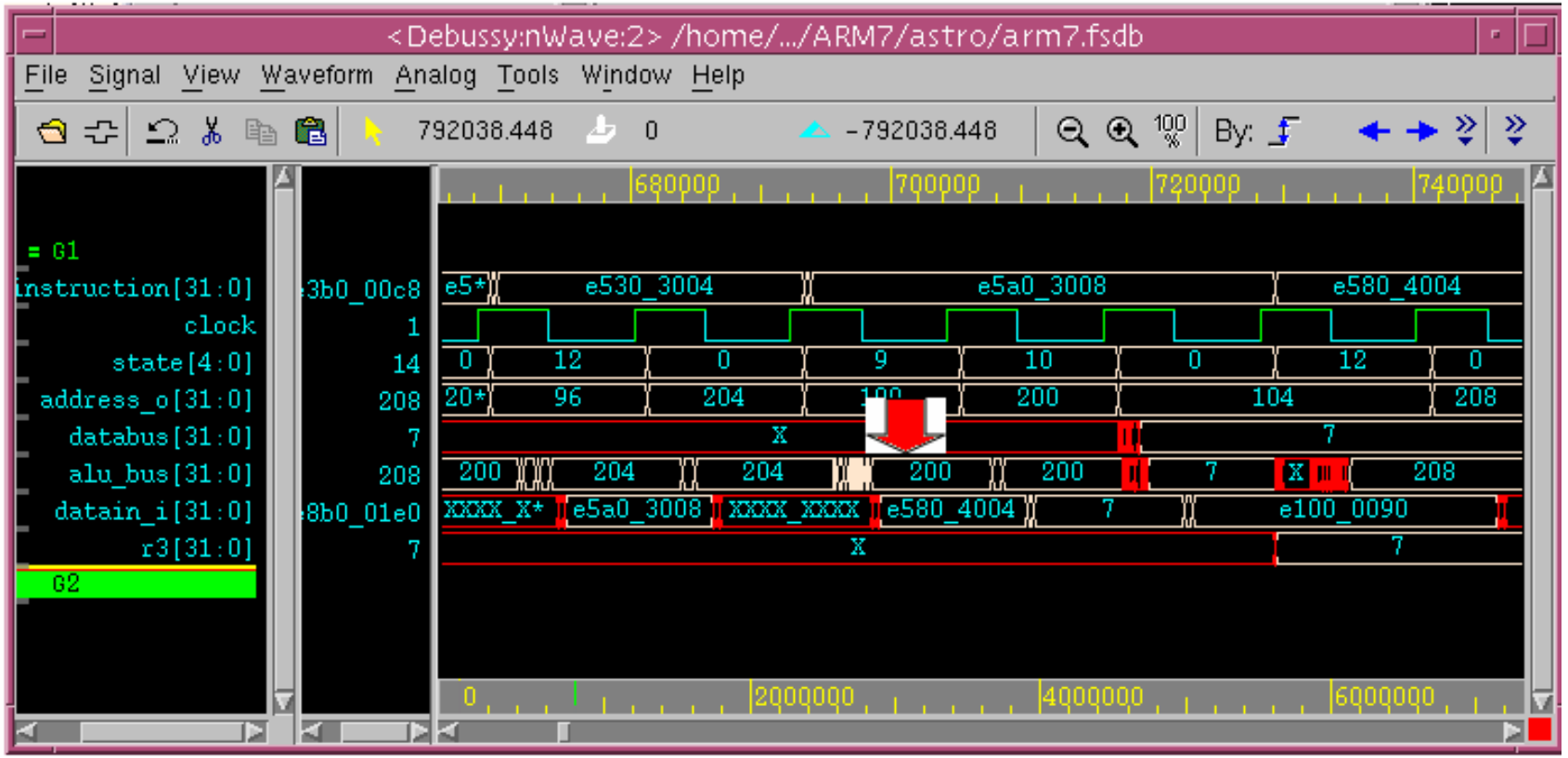
SIMULATION RESULTS

- Load Instruction
- Multiply Instruction

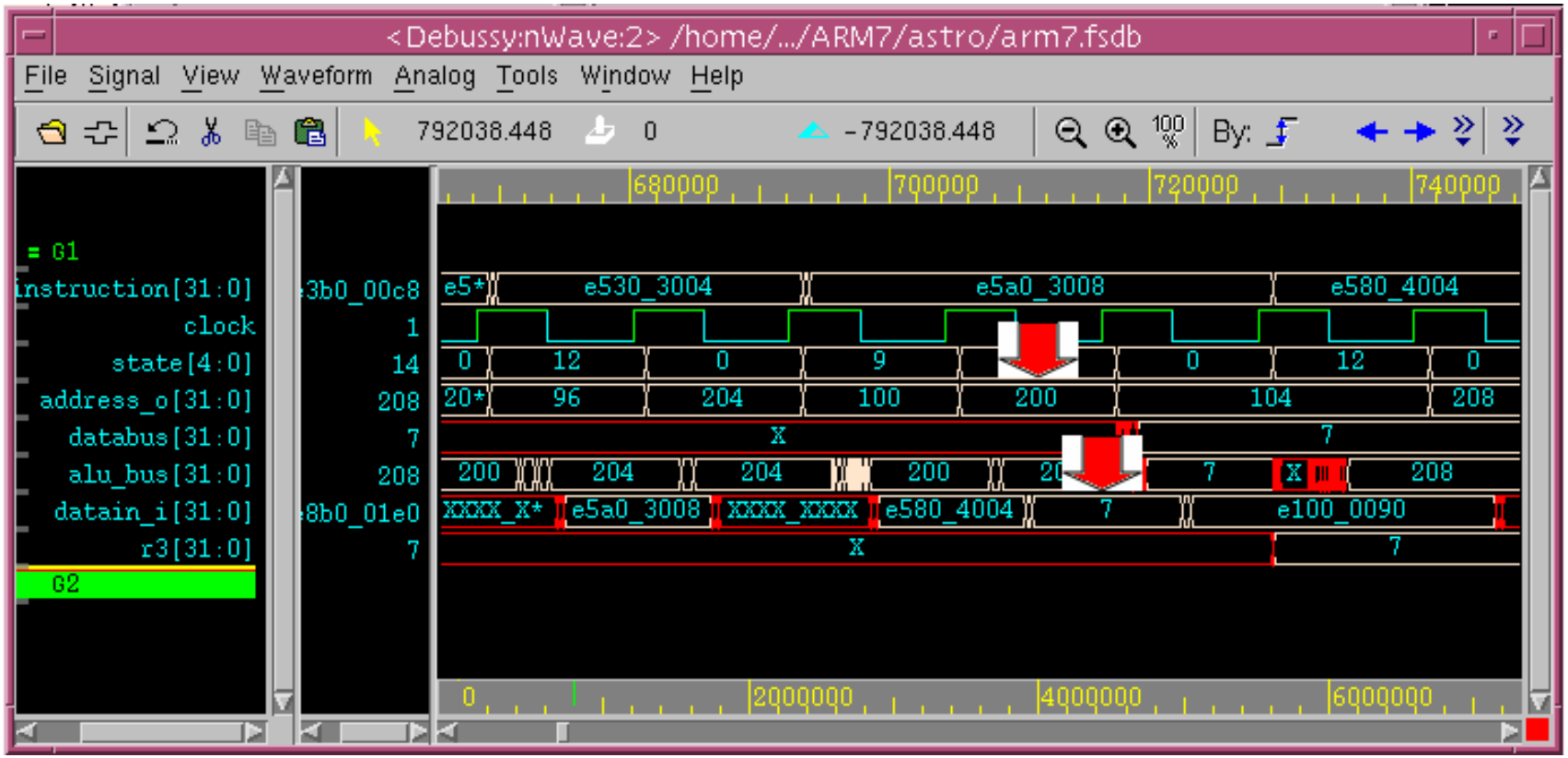
Load – Instruction decoding



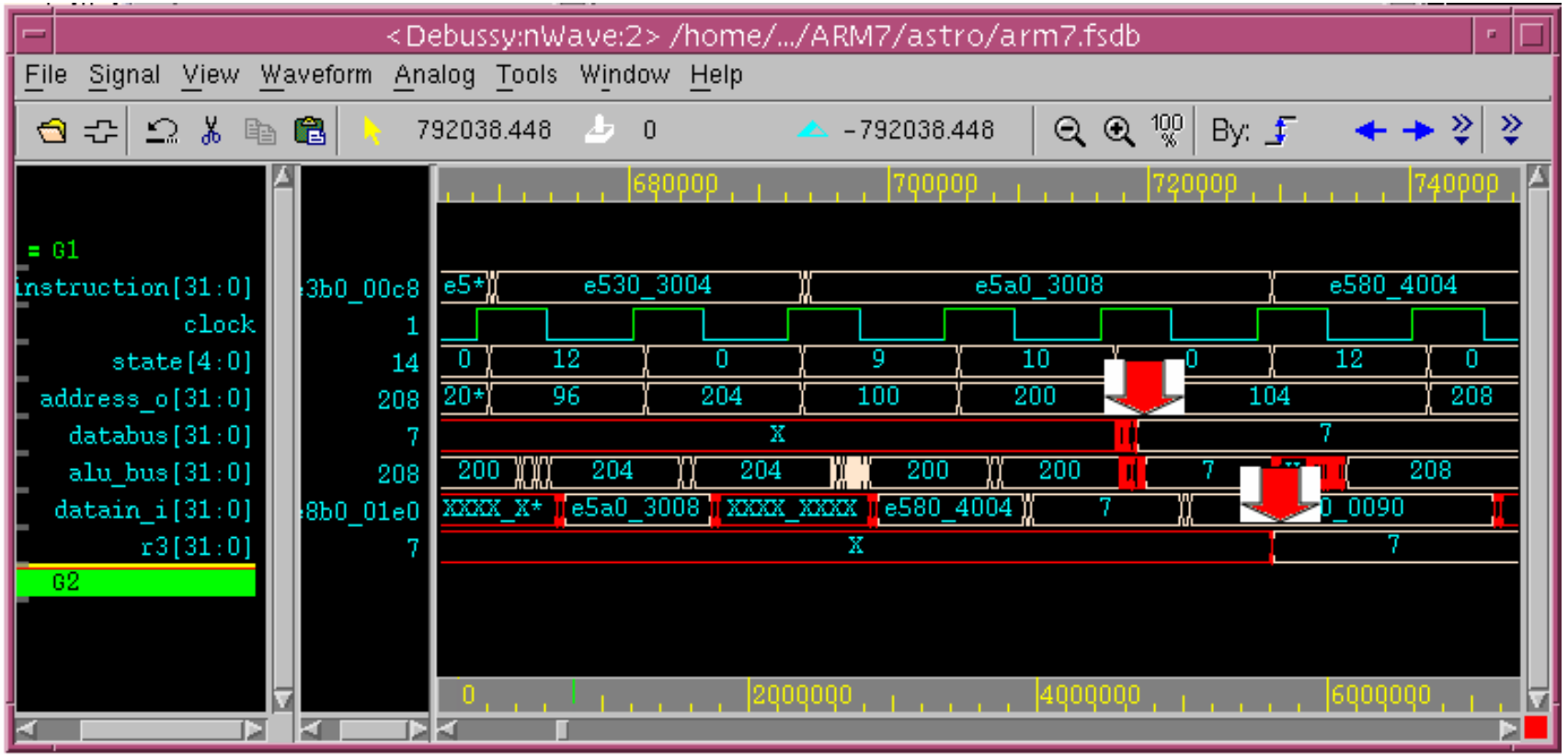
Load – Cycle 1


<Debussy:nWave:2> /home/.../ARM7/astro/arm7.fsdb
File Signal View Waveform Analog Tools Window Help
792038.448
0
-792038.448
By:
680000
700000
720000
740000
= G1
instruction[31:0]
clock
state[4:0]
address_o[31:0]
databus[31:0]
alu_bus[31:0]
datain_i[31:0]
r3[31:0]
G2
3b0_00c8
1
14
208
7
208
8b0_01e0
7
e5*
e530_3004
e5a0_3008
e580_4004
0
12
0
9
10
0
12
0
20*
96
204
200
104
208
X
7
200
204
204
200
200
7
X
208
xxxx_X*
e5a0_3008
xxxx_xxxx
e580_4004
7
e100_0090
X
7
0
2000000
4000000
6000000

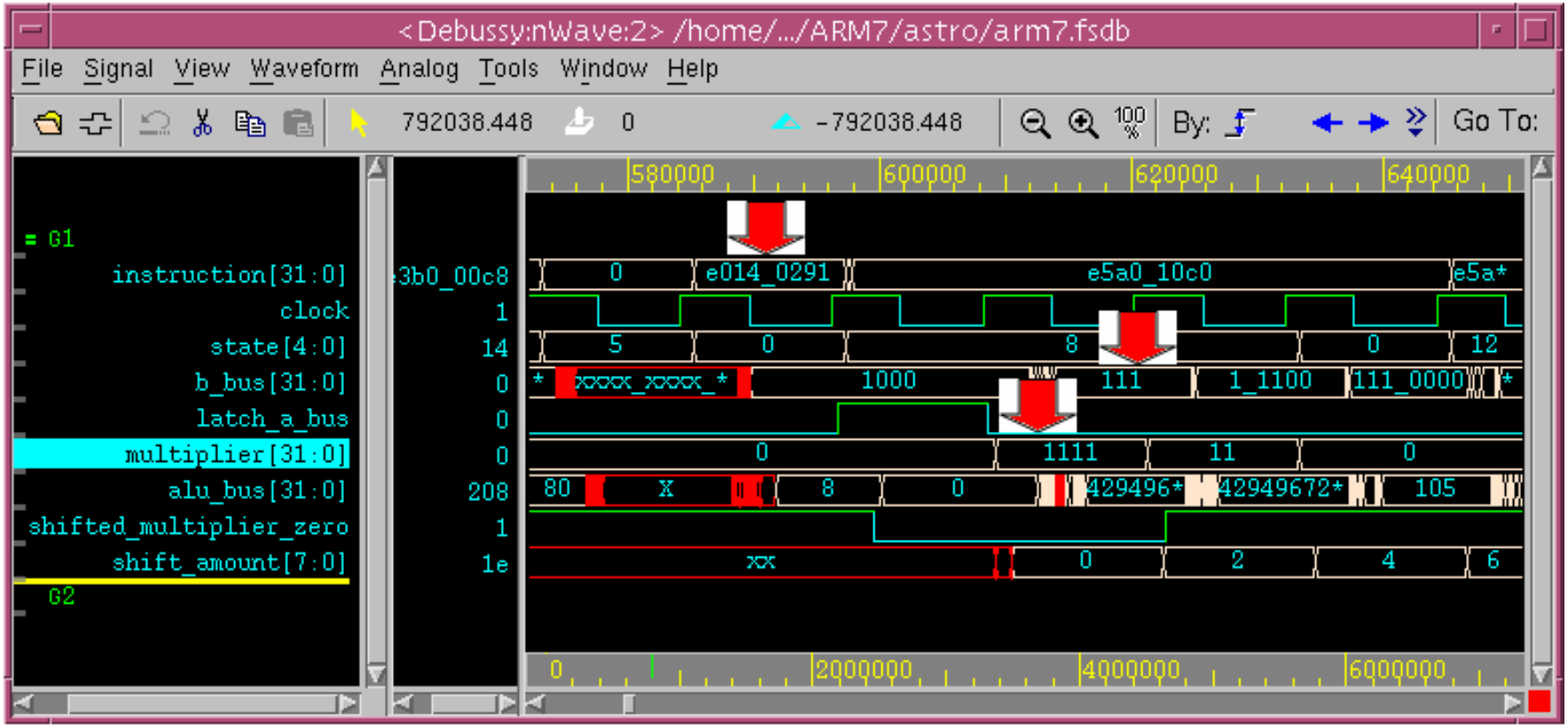
Load – Cycle 2


<Debussy:nWave:2> /home/.../ARM7/astro/arm7.fsdb
File Signal View Waveform Analog Tools Window Help
792038.448
0
-792038.448
By:
680000
700000
720000
740000
= G1
instruction[31:0]
clock
state[4:0]
address_o[31:0]
databus[31:0]
alu_bus[31:0]
datain_i[31:0]
r3[31:0]
G2
3b0_00c8
1
14
208
7
208
8b0_01e0
7
e5*
e530_3004
e5a0_3008
e580_4004
0
12
0
9
0
12
0
20*
96
204
100
200
104
208
X
7
200
204
204
200
7
X
208
XXXX_X*
e5a0_3008
XXXX_XXXX
e580_4004
7
e100_0090
X
7
0
2000000
4000000
6000000

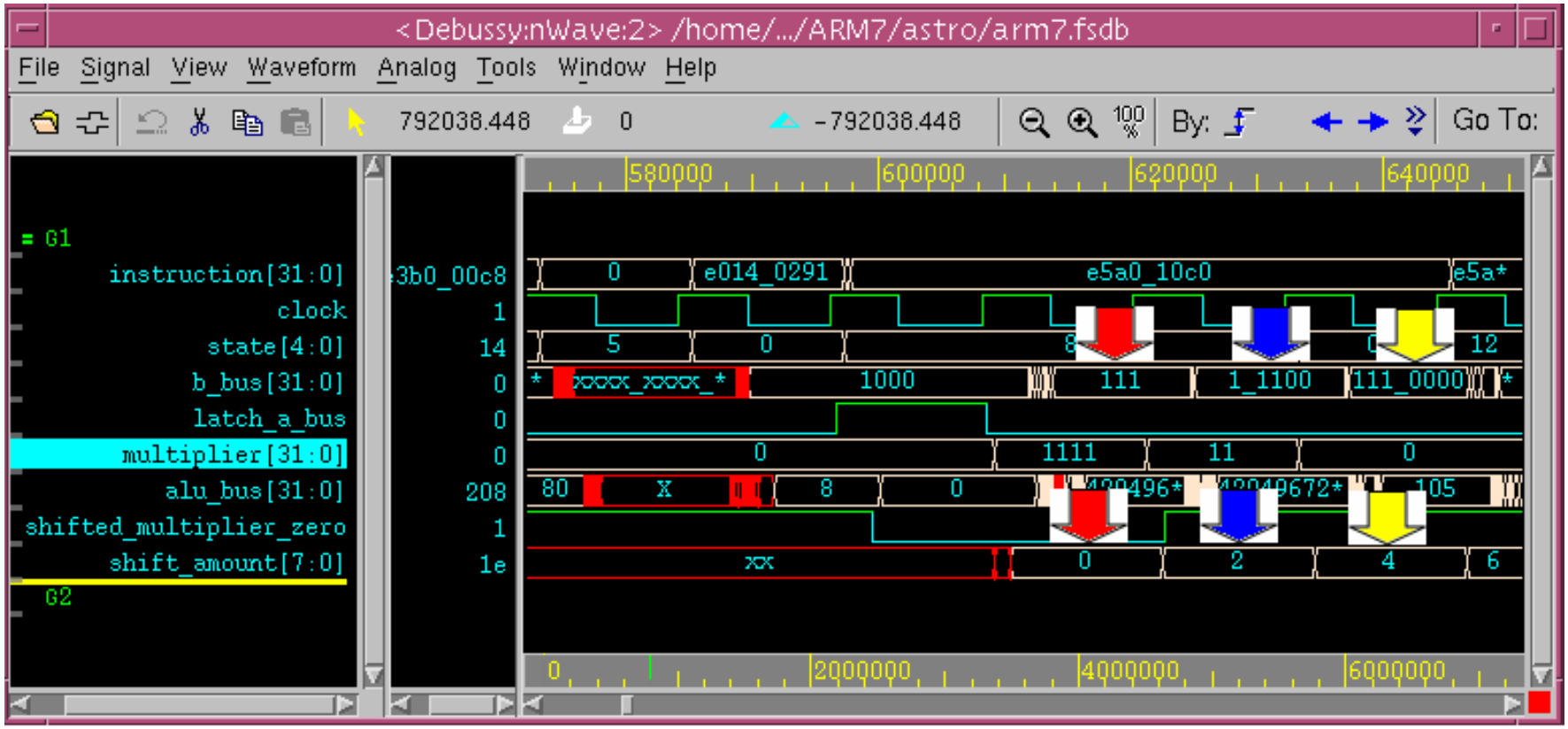
Load – Cycle 3


<Debussy:nWave:2> /home/.../ARM7/astro/arm7.fsdb
File Signal View Waveform Analog Tools Window Help
792038.448
0
-792038.448
By:
680000
700000
720000
740000
= G1
instruction[31:0]
clock
state[4:0]
address_o[31:0]
databus[31:0]
alu_bus[31:0]
datain_i[31:0]
r3[31:0]
G2
3b0_00c8
1
14
208
7
208
8b0_01e0
7
e5*
e530_3004
e5a0_3008
e580_4004
0
12
0
9
10
0
12
0
20*
96
204
100
200
104
208
X
7
200
204
204
200
200
7
208
XXXX_X*
e5a0_3008
XXXX_XXXX
e580_4004
7
0_0090
X
7
0
2000000
4000000
6000000

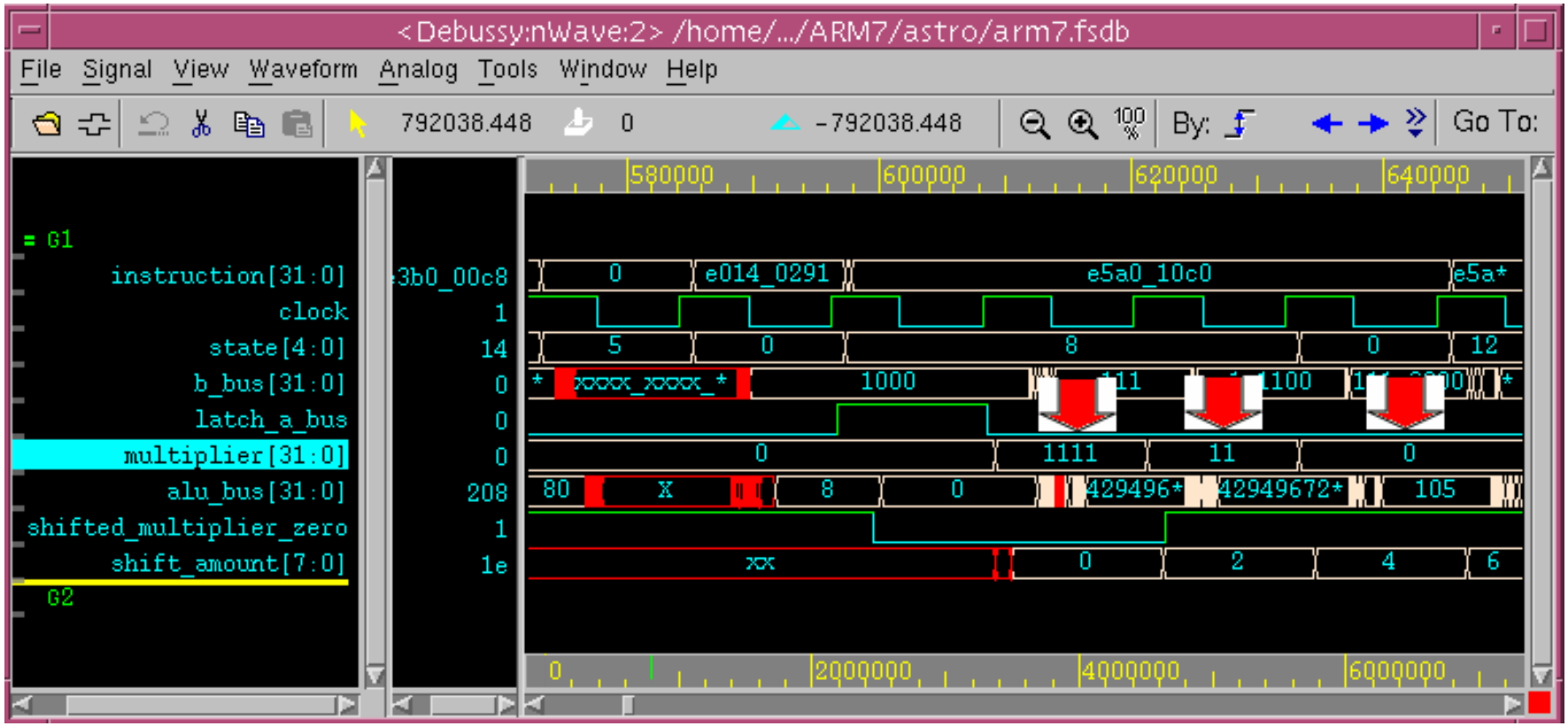
Multiply – Decoding, Multiplier, Multiplicand



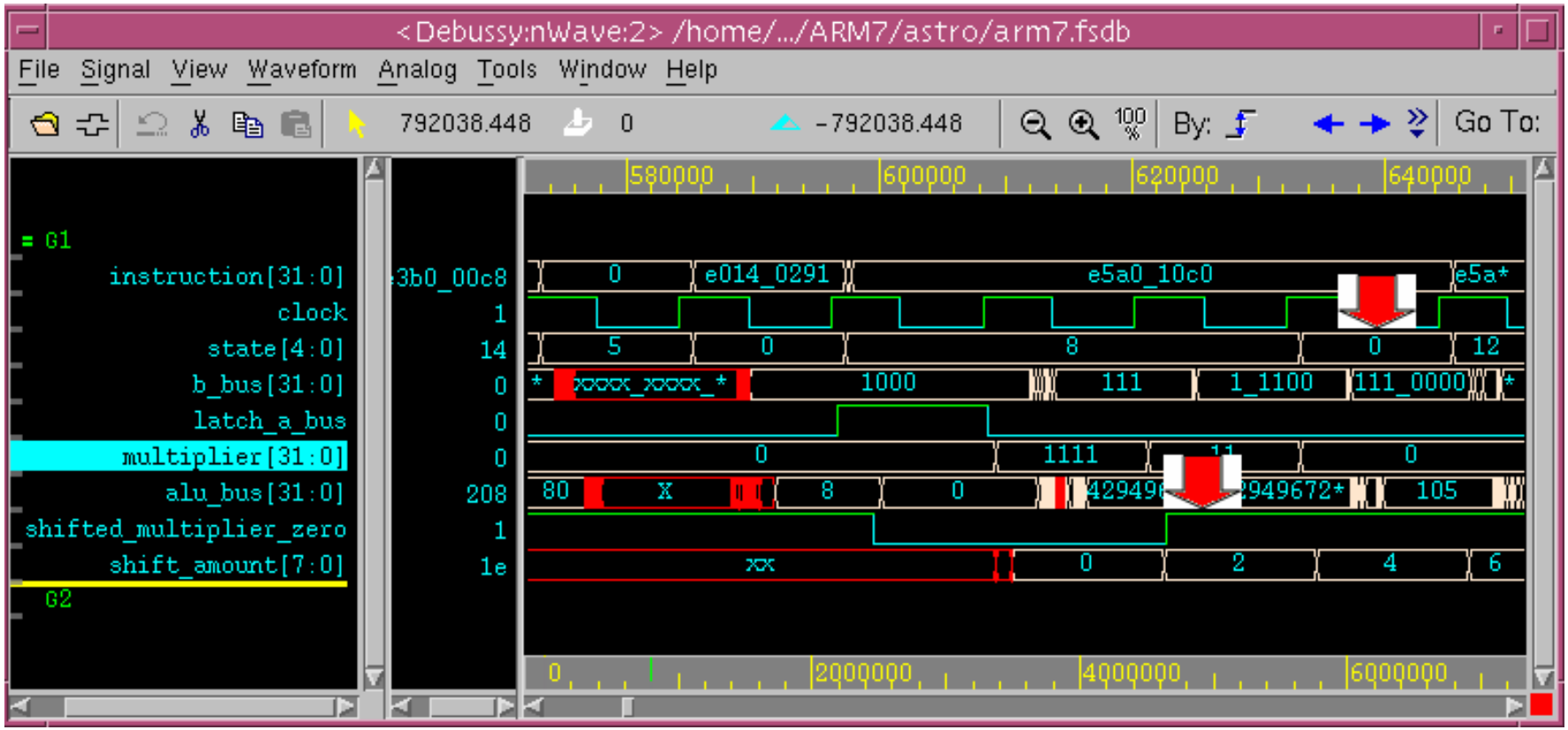
Multiply – Multiplicand is shifted left in each cycle according to Booth's algorithm



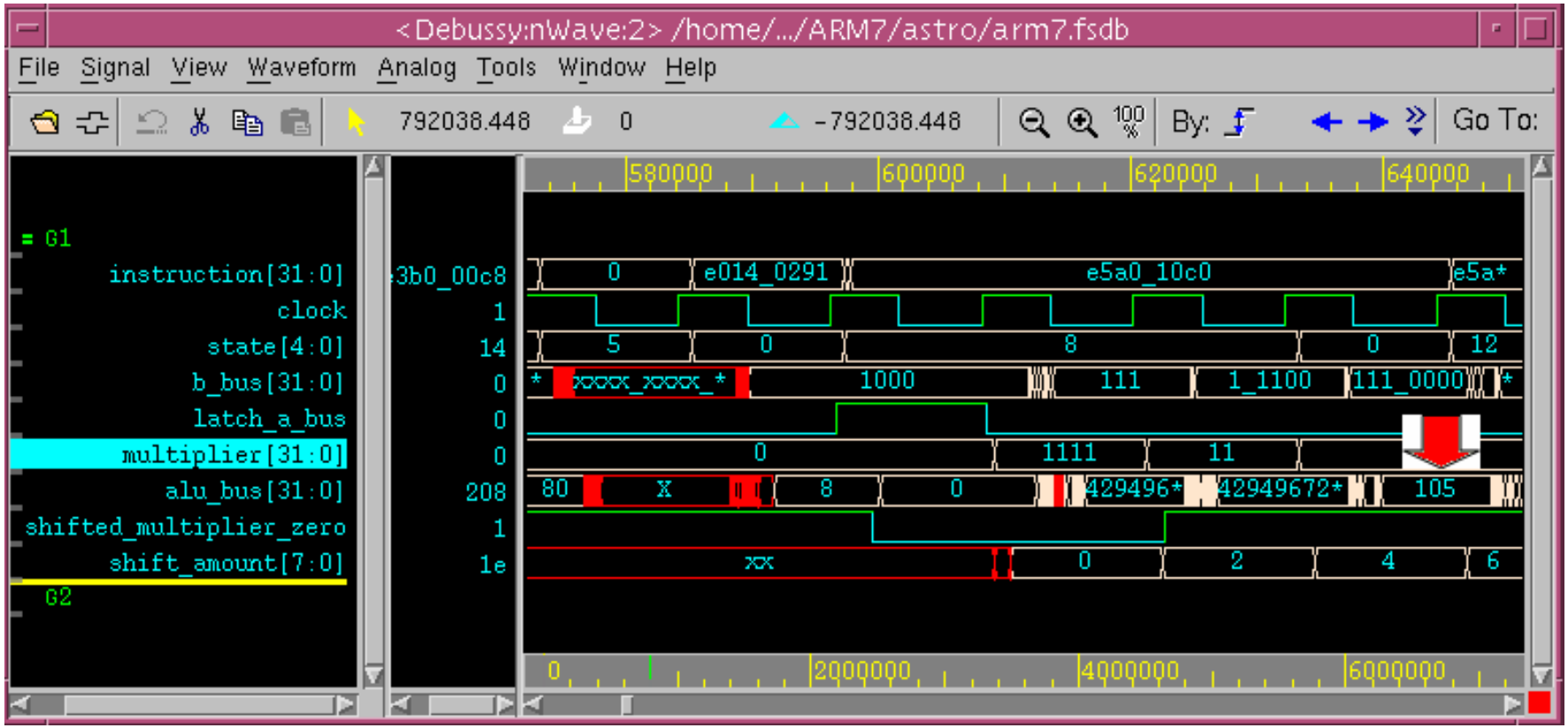
Multiply – Multiplier is shifted right 2 bits in each cycle



Multiply – The instruction completes when the shifted multiplier becomes zero



Multiply – The result is on ALU bus



CONCLUSION

(Max frequency before optimizations: 70Mhz)

Specifications	
Maximum operating frequency	90 MHz
Test frequency	10 MHz
Power supply voltage	1.8V
Power	30.9 mW
Gate count	286547
Area	7.97
Instruction count	34
Datapath width	32 bits

THANK YOU