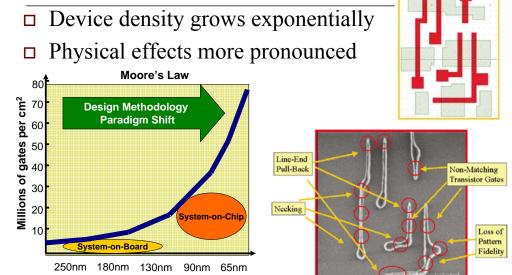
High-performance Routing at the Nanometer Scale

Igor Markov University of Michigan



Technology Trends and Challenges



Process Technology Node

Key Physical Effects



- □ 180nm wire delay comparable to gate delay
- □ 130nm noise due to crosstalk
- □ 90nm
 - Difficulty in printing features
 - Numerous design rules introduced in routing
 - □ Time consuming optical proximity correction (OPC)
 - Across the die variability
 - Significant delay due to coupling capacitance
 - Leakage power
- □ 65nm and beyond
 - CMP : uneven wire density leads to dishing, erosion
 - Random defects, yield issues
 - Power variability









Erosion

Problems with Traditional Flow

- Point tools
 - Little or no interaction
 - Oversimplified objectives
 - Poorly estimate real objectives
- Delayed yield optimization
 - Consensus: yield <u>should</u> be optimized by *routers*
 - Cadence: *entire PD flow* must account for yield
- Numerous design iterations
 - Greater time to market \Rightarrow revenue loss

In the Eye of the DFM/DFY Storm We Haven't Survived 85 nm - We're Just in the Eye of the Storm Mitch Heins, Pyxis Technology

Mitch Heins, Pyxis Technology
Page 1 of 2

"Summary: The Solution is in the Routing"

The phrase "eye of the storm" refers to the relatively calm center of a hurricane, where winds are light and the skies are only slightly cloudy, or even clear. If the eye of the hurricane passes over during the daytime, one might see sunny skies and even enjoy a rise in temperature. Observers sometimes

Our Strategy



5

7

- Identify simple but effective algorithms for routing
 - Start with global routing (easier)
- Develop flexible open-source infrastructure that will support algorithm extensions
- Identify DFM-related objectives & constraints relevant to global and detail routing
- □ Incorporate DFM concerns into routing

Our Contributions So Far



6

- □ FGR "Fairly Good Router" (ICCAD `07)
 - Routing based on Lagrange Multipliers
 - Extend A*-search to reshape net topology
- Best known results on ISPD'98 & ISPD'07 routing benchmark suites
- □ Extended empirical evaluation
 - Steiner trees vs. MSTs for net decomposition
 - Layer assignment for multi-layer routing

Review: Lagrange Relaxation

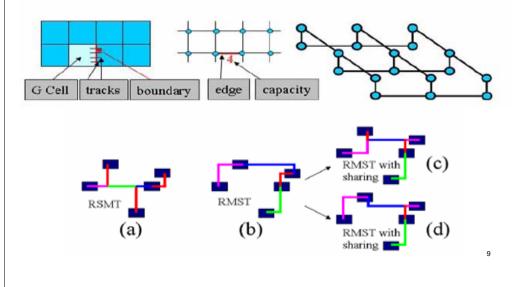
- □ Start with: *optimization problem with constraints*
- Convert constraints to penalties
- □ <u>Add penalties to original objective</u>
 - New variable for each penalty: *Lagrange multiplier*
- Optimizing new objective solves original problem
 - New problem is easier to solve
 - Continuous case
 - □ Solve with Newton's method, steepest decent, etc.
 - Discrete case
 - □ Iterative techniques such as RRR

Analogy

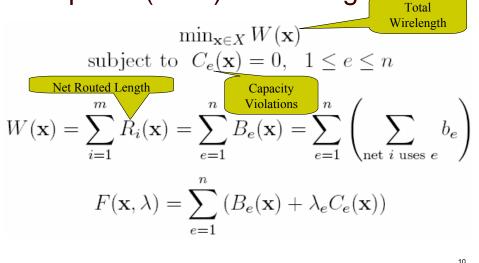
- □ Land prices in downtown
 - Many businesses want offices in downtown (competition)
 - Some businesses could move further
- □ Solution: auction
 - Start with initial price & solicit bids
 - Increase price until only one bidder remains
- □ Rationale: encourage efficient use of land



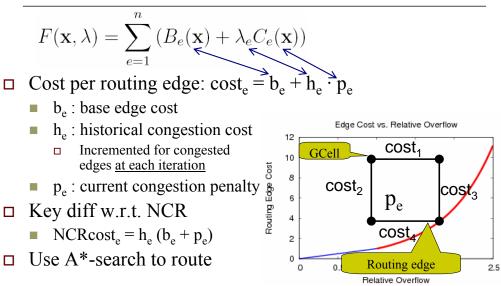
Review of Global Routing



Discrete Lagrange Multipliers (DLM) in Routing



DLM Formulation

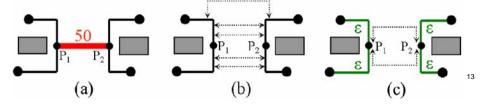


Multi-pin Nets

- □ Maze search connects pin pairs
 - Nets with 3 or more pins must be decomposed
- □ Standard decomposition methods
 - Steiner tree
 - □ If optimal, shortest possible wirelength
 - Minimum spanning tree
 - □ Up to 50% more wirelength than Steiner
 - □ Simple construction: easy to consider congestion
- \square We compare both options
 - Steiner trees lead to fewer routing segments, more vias

Topology Restructuring in Maze Search

- □ Static decompositions cannot react to congestion
 - Steiner points may become congested
- □ We reshape the tree during rerouting
 - Steiner points will change
 - Initial MSTs will become Steiner trees
- □ Modify routing edge weights in A*
 - Previously-used segments cost ε, a small value



2-d vs. Multi-layer Routing

- □ Maze routing can handle arbitrary grids
 - No theoretical limits on number of layers
 - Practically, only 2 layers are needed: H & V
- \Box To route multi-layer as 2-d:
 - Combine H & V capacities for each GCell
 - Route along the induced 2-d grid
 - Convert the 2-d soln. by layer assignment
- 2-d routing + layer assignment faster, more successful
 - When multi-layer succeeds, better soln. quality

Summary of Empirical Results

ISPD'98 benchmarks (no vias)

- 12k 64k nets, 64x64 256x64 GCells, 1 layer
- Violation free (unmatched in literature)
- 2.7% better WL than FastRoute
- 3.6% better WL than BoxRouter, 35% less runtime

□ ISPD'07 contest benchmarks

- 220k 860k nets, 324x324 973x1256 GCells
- 2-d : 2 layers, 3-d : 6 layers
- 8.4% better WL than MaizeRouter (1st 3-d, 2nd 2-d)
- 9.9% better WL than BoxRouter (2nd 3-d, 3rd 2-d)¹⁵

Results for ISPD'98 benchmarks

- Comparison to published results for BoxRouter and FastRoute 2.0
- □ FGR is 35% faster than BoxRouter

Bench-	BoxRouter		FastRoute 2.0		FGR		vs. Box-	vs. Fast-
$_{mark}$	ovfl	WL	ovfl	WL	ovfl	WL	Router	Route 2.0
ibm01	102	65588	31	68489	0	63332	-3.44%	-7.53%
ibm02	33	178759	0	178868	0	168918	-5.51%	-5.56%
ibm03	0	151299	0	150393	0	146412	-3.23%	-2.65%
ibm04	309	173289	64	175037	0	167101	-3.57%	-4.53%
ibm05	0	409747	-	-	0	409739	-0.00%	_
ibm06	0	282325	0	284935	0	277608	-1.67%	-2.57%
ibm07	53	378876	0	375185	0	366180	-3.35%	-2.40%
ibm08	0	415025	0	411703	0	404714	-2.48%	-1.70%
ibm09	0	418615	3	424949	0	413053	-1.33%	-2.80%
ibm10	0	593186	0	595622	0	578795	-2.43%	-2.83%
Average							-2.71%	-3.64%

16

14

ISPD'07 Contest Benchmarks

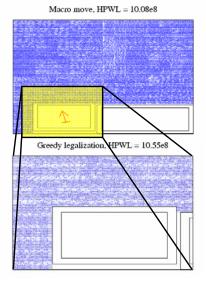
□ Best competition: BoxRouter & MaizeRouter

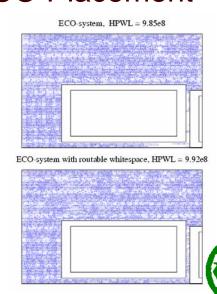
Bench- mark		Best of	BoxRou	ter and l	MaizeRouter	FGR			
		Overflow		Cost		Overflow		Cost	vs.
		total max		(e5) Router		total	max	(e5)	Best
adaptec	#1 2-d	0	0	58.84	Box	0	0	54.44	-7.48%
	#1 3-d	0	0	99.61	Maize	0	0	88.45	-11.20%
	#2 2-d	0	0	55.69	Box	0	0	52.30	-6.09%
	#2 3-d	0	0	98.12	Maize	0	0	89.89	-8.39%
	#3 2-d	0	0	137.75	Maize	0	0	130.89	-4.98%
	#3 3-d	0	0	214.08	Maize	0	0	199.66	-6.74%
	#4 2-d	0	0	128.45	Maize	0	0	125.00	-2.69%
	#4 3-d	0	0	194.38	Maize	0	0	179.36*	-7.73%
	#5 2-d	0	0	164.32	Box	0	0	152.13	-7.42%
	#5 3-d	0	0	298.08	Box	0	0	259.98	-12.78%
newblue	#1 2-d	400	2	51.13	Box	526	4	47.42	-7.26%
	#1 3-d	400	2	101.83	Box	514	2	94.26	-7.43%
	#2 2-d	0	0	79.64	Maize	0	0	76.51	-3.93%
	#2 3-d	0	0	139.66	Maize	0	0	129.40*	-7.35%
	#3 2-d	32588	1236	114.63	Maize	39908	1120	109.23	-4.71%
	#3 3-d	32840	1058	184.40	Maize	39828	374	173.71	-5.80%
A	verage								-7.03%

Applications of Our Algorithms & SW

- □ Incremental routing
- Detail routing
- Integrated place-and-route
- DFM-aware global and detail routing
- An open-source RTL-to-GDSII tool-chain

Illustration: ECO Placement



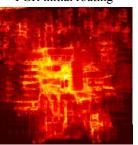


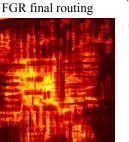
17

Integrated Place-and-Route

- □ FGR initial routing
 - Many times faster than full routing
 - Congestion and WL very similar to final solution
- □ Use these maps in **ROOSTER** (our placer)



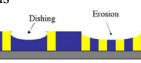




18

Yield- and Manufacturability-driven Routing

- Model-based routing
- Minimization of vias
 - Major source of timing, variability problems
 - Doubling often needed to improve yield
- □ Density constraints
 - Affect capacitance, crosstalk, CMP





- □ From CANDE 2005 predictions for 2010
 - An open-source RTL-to-GDSII tool-chain will be available
- □ Currently available tools
 - Synthesis & technology mapping (ABC, OAGear)
 - Verification (MiniSAT, CUDD, OAGear)
 - ATPG (ATALANTA)
 - Partitioning, floorplanning & placement (UMPack)

□ Missing

- Full-chip routing
- Clock-tree synthesis

Summary

- □ Routing is key to DFM
 - Must be flexible to accommodate DFM concerns
 - Must use simple algorithms
- \square FGR framework Lagrange multipliers \mathcal{F}
 - Unmatched solution quality
 - Extensions for yield and manufacturability \check{R}
- □ Integrated P&R
- □ DFM-aware routing
- □ Open source tools FGR release @ICCAD` 07_{π}

References

- □ J. A. Roy and I. L. Markov, "High-performance Routing at the Nanometer Scale", ICCAD 2007
- FGR

22

- J. A. Roy and I. L. Markov, "ECO-system: Embracing the Change in Placement", to appear in *IEEE Trans. on CAD*, 2008
- J. A. Roy and I. L. Markov,
 "Seeing the Forest and the Trees: Steiner Wirelength Optimization in Placement", *IEEE Trans. on CAD*, vol. 26 no. 4, pp. 632-644, April 2007

