Topic I

Class Introduction

系統晶片驗證

SoC Verification

Sep, 2004

Class Information

- Class website:
  http://cc.ee.ntu.edu.tw/~ric/teaching/SoC_Verification/F04/
- My office:
  - EE building 444
  - (Tel) 2363-5251 ext 444
  - (e-mail) ric@cc.ee.ntu.edu.tw
  - Office hour: stop by or by e-mail appointment
- Class TA

Class Information (2)

- References
  - Class handouts/slides
  - *"System-on-a-Chip Verification - Methodology and Techniques"*, Prakash Rashinkar, Peter Paterson, and Leena Singh, Kluwer Academic Publishers.
  - *"Assertion-Based Design"*, Harry Foster, Adam Krolnik, and David Lacey, Kluwer Academic Publishers.
  - *"Writing Testbenches: Functional Verification of HDL Models"*, Janick Bergeron, Kluwer Academic Publishers.

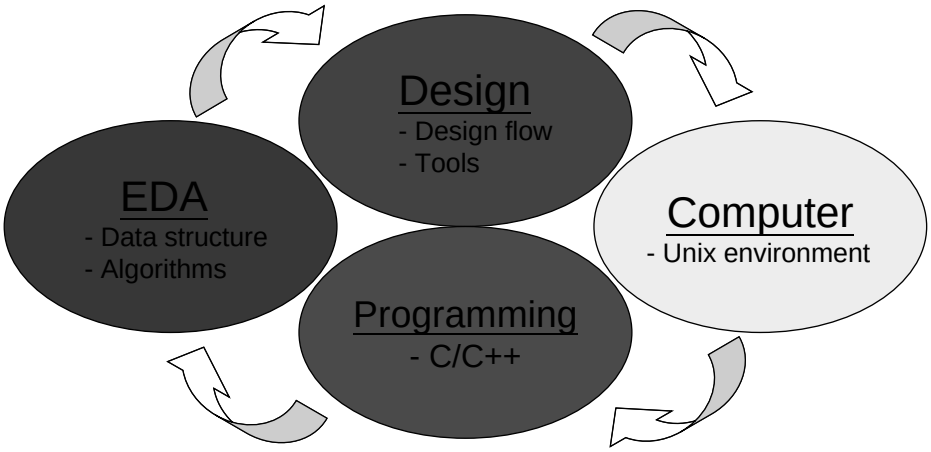
Grading

- Homework 30%
- Midterm exam 30%
- Final exam or project 40%
- Bonus TBD

The final grade will be linearly adjusted.

Instructor will determine the average and standard deviation

Background Requirements



If you are short of any of the above, please try to make up ASAP

Class Objectives

What do you expect to learn from this class?

Why do you take this course?

Class Objectives

1. Learn the different verification options
   - Trade-offs between techniques
   - Make up your best verification plan
   - Improve your verification / design quality
   - New verification languages
2. Understand the principles of verification algorithms
   - Set the right expectation / attitude
   - State-of-the-art verification techniques
   - Software training
3. Get a sense about the EDA business

Class Topics

1. Class Overview
   - Administrative information
2. SoC Design Overview
   - Opportunities and challenges
   - IP-based design
3. Verification Techniques Overview (I)
   - Simulation
   - Emulation
   - Formal verification
4. Verification Techniques Overview (II)
   - Static analysis
   - Physical verification
   - Testing

Class Topics

5. System-Level Design and Verification
   - Verification planning
   - Electronic System Level (ESL) languages
   - HW/SW co-design/co-verification
   - Assertion-based verification
6. Simulation-based Verification
   - Simulator techniques
   - Error diagnosis and debugging
   - Testbench authoring
7. Emulation-based verification
   - Emulation
   - Hardware accelation
   - Rapid prototyping

Class Topics

8. Mid term exam

9. Formal Verification Techniques (I)
   - Property Specification Languages (PSL)
   - Constraint Satisfaction Problem (CSP)
   - Boolean techniques
     - BDD, SAT, ATPG
10. Formal Verification Techniques (II)
   - Unbounded proof techniques
   - Advance formal techniques
   - Semi-formal verification
   - Formal verification tools

Class Topics

11. Static Analysis
    - Linting tools
    - Clock domain check
    - Static timing analysis
12. Physical Verification
    - Design rule checking
    - Signal integrity
    - Design for Manufacturing (DfM) issues
13. Special Topics
    - CPU verification
    - Memory verification
    - Managing the verification work
14. **Final exam**