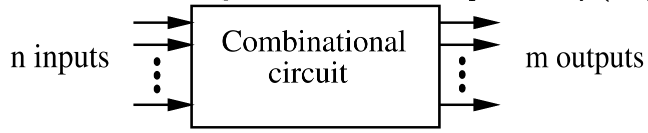
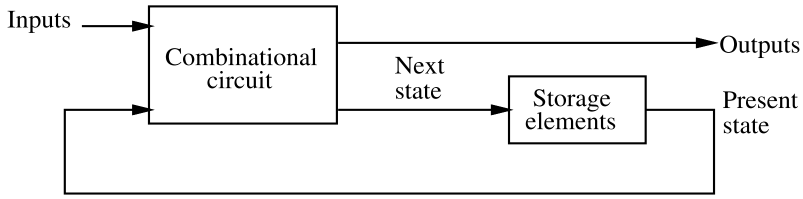
Sequential Systems

- **No state:** Combinational logic system: $Output := f(Inputs)$.

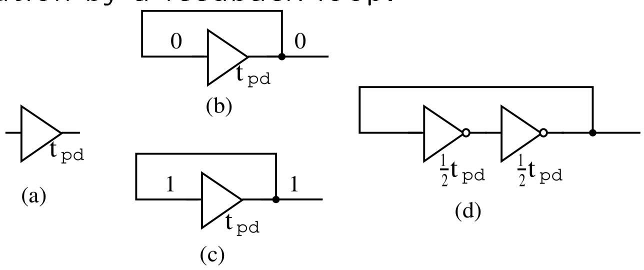


- **State present:** Sequential logic system: $Output := f(Inputs, State)$.
  - **Synchronous** sequential system: State updated at **discrete time**.
  - **Asynchronous** sequential system: State updated at **any time**.
  - Consists of two components: **combinational circuit** and **storage elements**.
  - Signals: inputs, outputs, **state**.

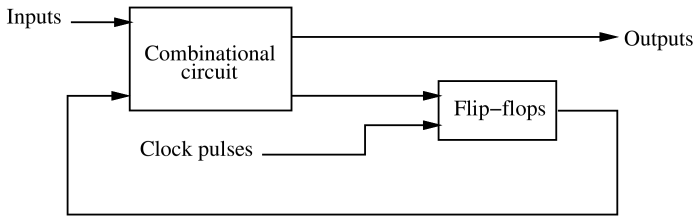


Sequential Circuits

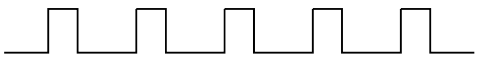
- Storing information by a feedback loop:



- **Synchronous clocked sequential circuit:** Use clock pluses as inputs to storage elements.



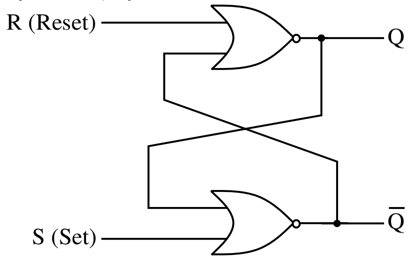
(a) Block diagram



(b) Timing diagram of clock pulses

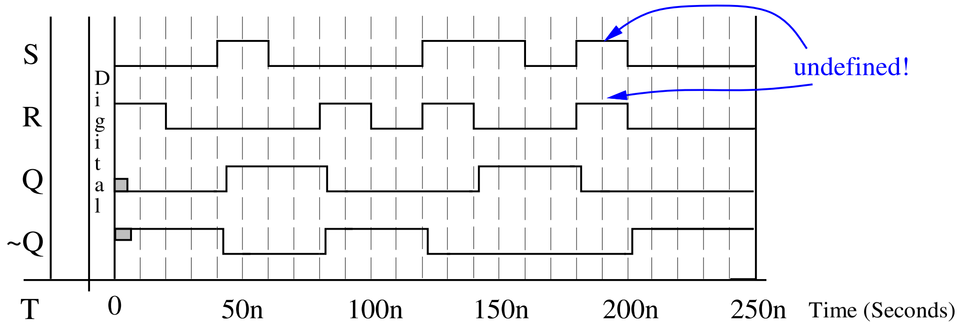
SR Latch

- **Set state:** $Q = 1, \overline{Q} = 0$; **Reset state:** $Q = 0, \overline{Q} = 1$.



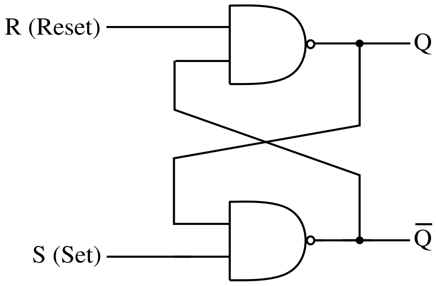
S	R	Q	$\overline{Q}$	
1	0	1	0	Set State
0	0	1	0	
0	1	0	1	Reset State
0	0	0	1	
1	1	0	0	Undefined

- Timing simulation: Propagation delay of the NOR gate: 2 ns; inputs changed every 20 ns.



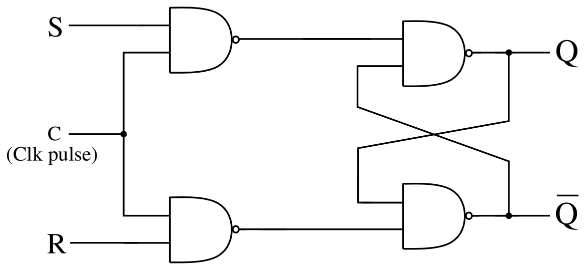
$\bar{S}\bar{R}$ and SR Latches

- $\bar{S}\bar{R}$ latch with NAND gates:



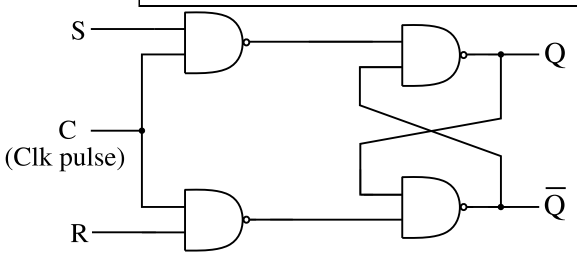
S	R	Q	$\overline{Q}$	
0	1	1	0	Set State
1	1	1	0	
1	0	0	1	Reset State
1	1	0	1	
0	0	1	1	Undefined

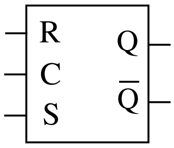
- SR latch with clock pulse: R and S are only observed when the input line C (clock pulse) is **high**.



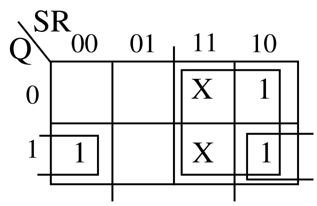
C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q=0 ; Reset state
1	1	0	Q=1 ; Set state
1	1	1	Undefined

SR Latch with Clock Input





Q	S	R	Q(t+1)	Comment
0	0	0	0	No change
0	0	1	0	Clear Q
0	1	0	1	Set Q
0	1	1	??	Undefined
1	0	0	1	No change
1	0	1	0	Clear Q
1	1	0	1	Set Q
1	1	1	??	Undefined

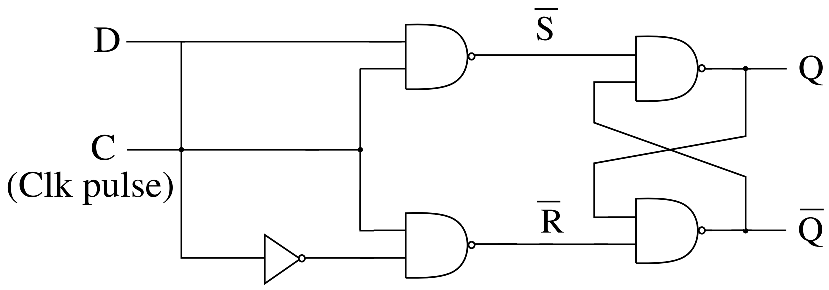


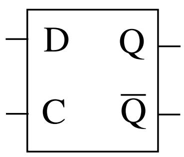
Q(t+1) = S + $\overline{\text{R}}$ Q,
where SR = 0.

- **Characteristic equation** for SR Flip Flop: $Q(t+1) = S + \overline{R}Q$, where $SR = 0$.

D Latch

- Characteristic equation for D latch: $Q(t+1) = D$.



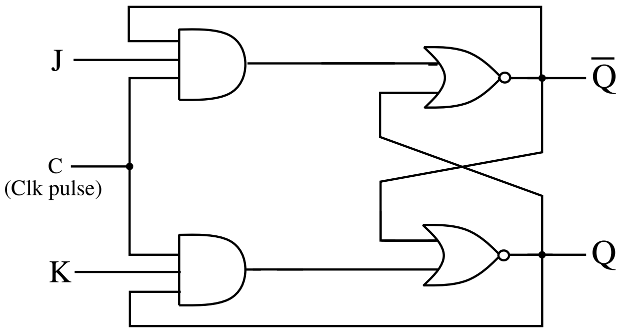


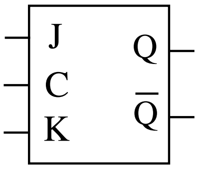
C	D	Next state of Q
0	X	No change
1	0	Q=0 ; Reset state
1	1	Q=1 ; Set state

Q	D	Q(t+1)	Comment
0	0	0	No change
0	1	1	Set Q
1	0	0	Clear Q
1	1	1	Set Q

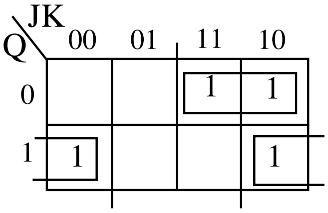
JK Latch

- Characteristic equation for JK latch: $Q(t+1) = J\overline{Q} + \overline{K}Q$.





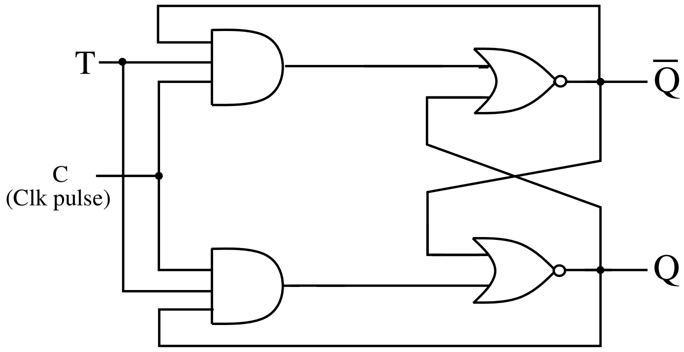
Q	J	K	Q(t+1)	Comment
0	0	0	0	No change
0	0	1	0	Clear Q
0	1	0	1	Set Q
0	1	1	1	Toggle Q
1	0	0	1	No change
1	0	1	0	Clear Q
1	1	0	1	Set Q
1	1	1	0	Toggle Q

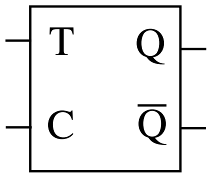


$Q(t+1) = J\overline{Q} + \overline{K}\,Q,$

T Flip Flop

- Characteristic equation for T latch: $Q(t+1) = T \oplus Q = T\overline{Q} + \overline{T}Q$.





Q	T	Q(t+1)	Comment
0	0	0	No change
0	1	1	Toggle Q
1	0	1	No change
1	1	0	Toggle Q