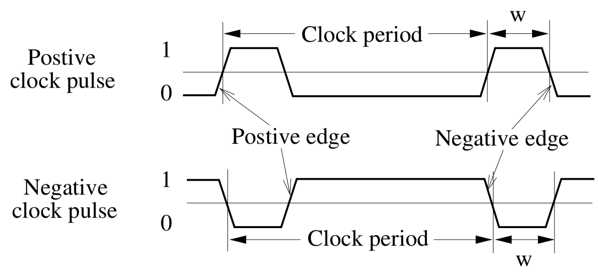
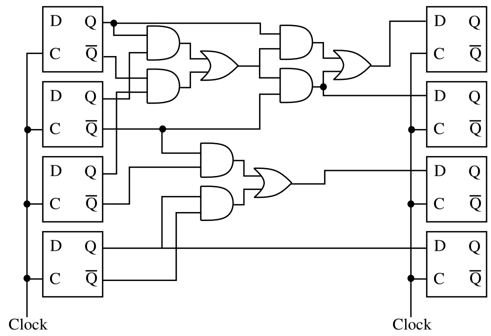
Clocking Concepts

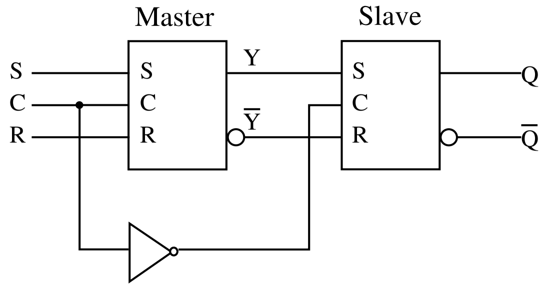


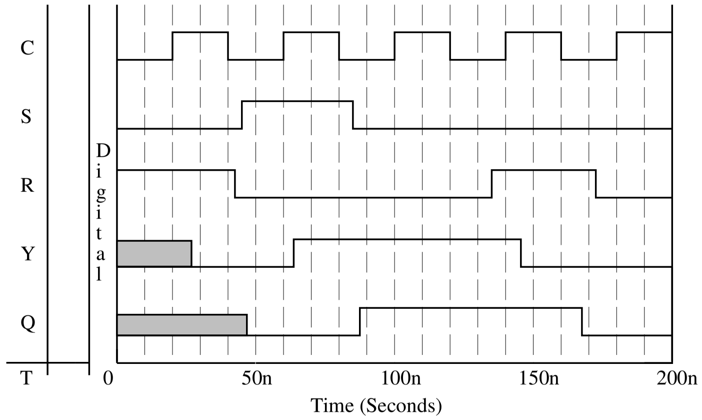
- If the clock **period** is **too short**, some data changes will not propagate through the circuit.
- If the clock **pulse width** is **too long**, some data will propagate through the second rank of flip-flops.
- Solutions to the clocking problem? **Master-slave flip-flop, edge triggering.**



SR Master-Slave Flip-Flop

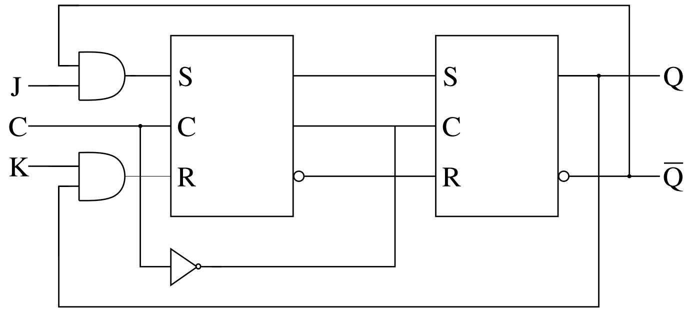
- $C = 1$: The master latch is enabled, and S and R ($SR = 0$) control the value Y. (The slave latch is disabled.)
- $C = 0$: The slave latch is enabled, and $Q = Y$. (The master latch is disabled.)





JK Master-Slave Flip-Flop

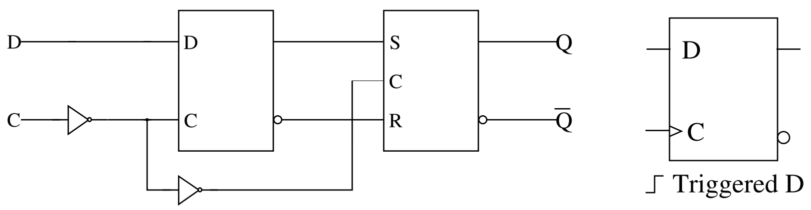
- Master Set is possible if the slave Q is currently "0" any time the clock C is high.
- Master Reset is possible if the slave Q is currently "1" any time the clock C is high.



J	K	Next State of Q
0	0	Q
0	1	0
1	0	1
1	1	$\overline{Q}$

Edge-Triggered Flip-Flops

- An **edge-triggered** flip-flop **triggers** only during a **transition** of the clock signal.
  - Positive edge-triggered (0-to-1 transition) vs. Negative edge-triggered (1-to-0 transition)
  - **Setup time (T_{setup}):** The time required for input data to be stable **before the clock edge**.
  - **Hold time (T_{hold}):** The time data must remain stable **after the clock edge**.
  - **Clock skew:** Maximum difference in clock arrival times at different flip-flops.



D–type postive–edge–triggered flip–flop