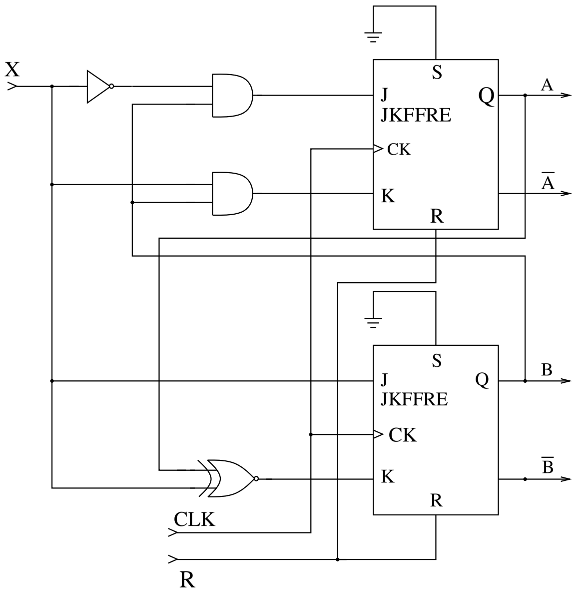
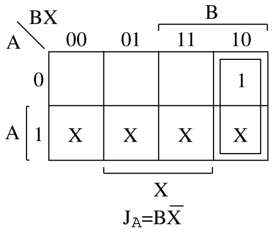
Designing with JK Flip-Flops (cont'd)

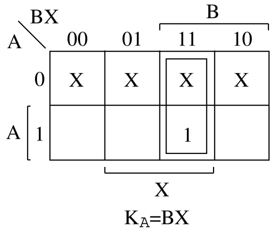
- Simplify the flip-flop input and output equations.

$$\begin{aligned} J_A &= B\bar{X};\ K_A = BX; \\ J_B &= X;\ K_B = AX + \bar{A}\bar{X} \end{aligned}$$

- Draw the logic diagram with flip-flops and combinational gates.

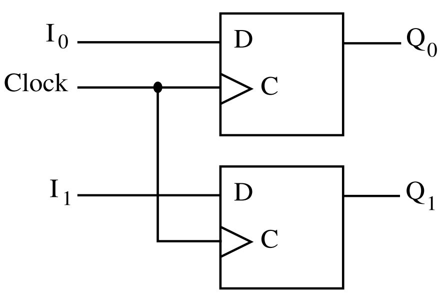






Register

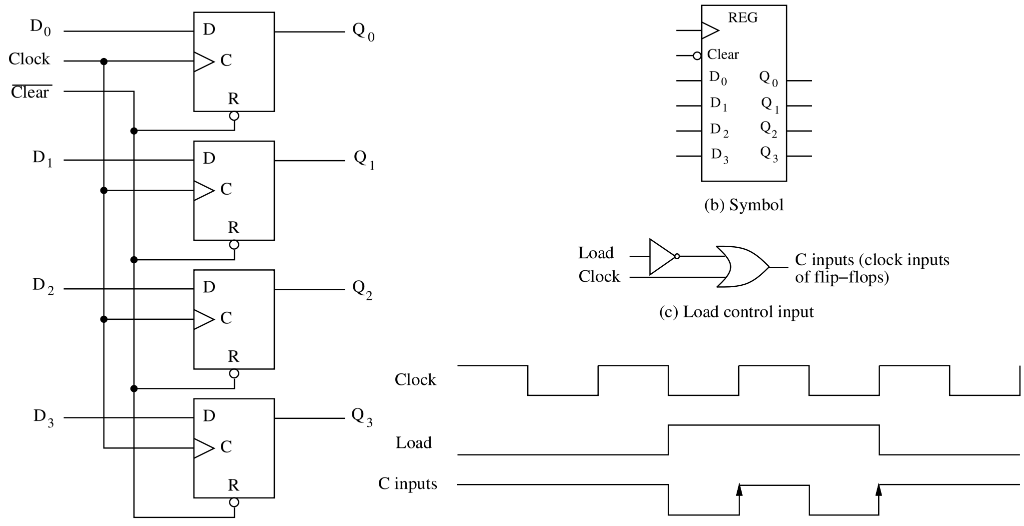
- A **register** is a collection of flip-flops with a common clock used primarily to hold (a vector of) binary information.
- Generally, registers are used to perform simple data storage and movement operations.
- A 2-bit register: # of states? # of inputs/outputs? next state? Moore or Mealy?



Current state	Next state $Q_1(t+1)\ Q_0(t+1)$				Output
$Q_1 Q_0$	$I_1 I_0$				$Q_1 Q_0$
	00	01	10	11	
00	00	01	10	11	00
01	00	01	10	11	01
10	00	01	10	11	10
11	00	01	10	11	11

Registers

- How can we “selectively” store data in some registers and leave the others unchanged?
  - Use a flip-flop that can “hold” under some set of logic inputs: SR, JK, and T: “hold” state when inputs are “0”.
  - “Gate” the input with a load control logic signal (**clock gating**).



(a) Logic diagram

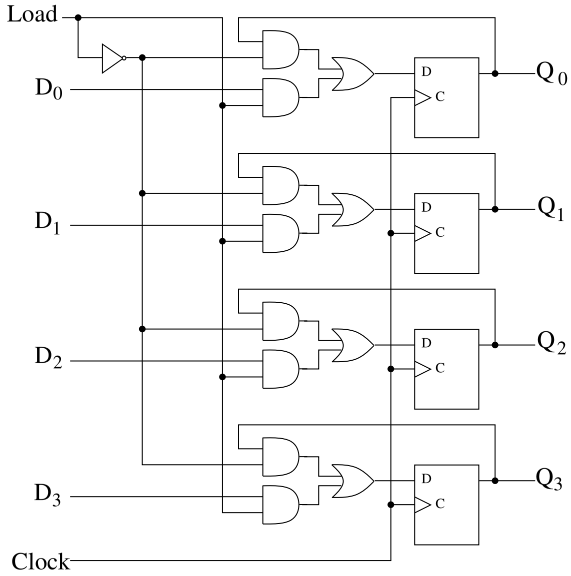
(b) Symbol

(c) Load control input

(d) Timing diagram

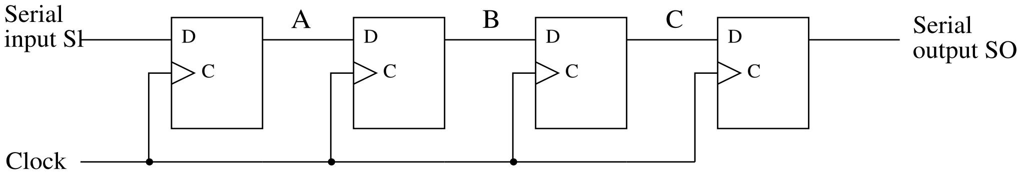
Registers with Load Control

- Clock gating might cause the **clock skew** problem.
- Better way: Run the clock continuously and use a load control to selectively change the register contents.
- $Load = 1$: Outputs are replaced by the current inputs; $Load = 0$: Data holds.

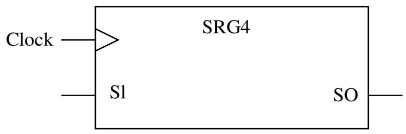


Shift Registers

- **Shift registers** are a special class of registers that can be used to store and manipulate data.
- The data input, SI, is often called "serial input" (shift-right input: shift a 1-bit input to the right at each clock).
- The data output, SO, is often called "serial output".
- Collectively, A, B, C, and SO are often called the "parallel outputs."



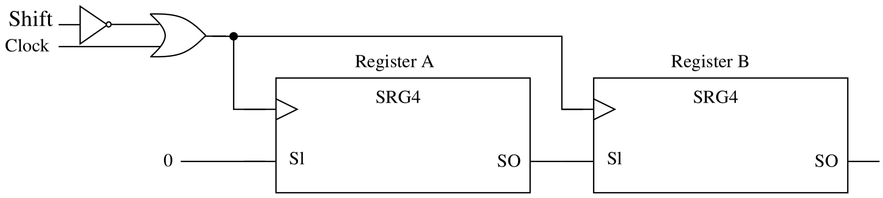
(a) Logic diagram

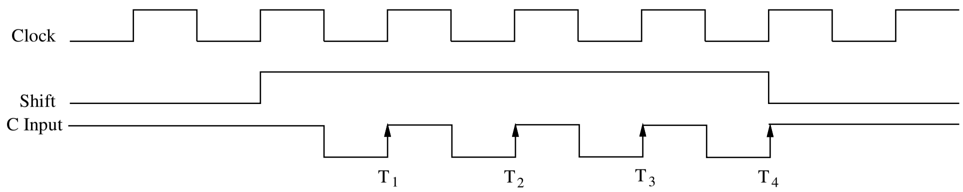


(b) Symbol

Serial Transfer

- $Shift = 1$: Enables the shift register; $Shift = 0$: Disables the shift register.





Timing pulse	Shift Register A				Shift Register B			
Initial value	1	0	1	1	0	0	1	0
After T_1	0	1	0	1	1	0	0	1
After T_2	0	0	1	0	1	1	0	0
After T_3	0	0	0	1	0	1	1	0
After T_4	0	0	0	0	1	0	1	1