IC Fabrication Dilemma

- IC fabrication dilemma:
  - IC logic density increases **exponentially** with time.
  - The more ICs you make, the **cheaper** they get.
  - Complex logic ICs have very **specific** functions, so you make **fewer**.
- **Question:** How do I make very high volume parts that are very dense?
  - Ans #1: Microprocessors that have very large volume (e.g., automobile ignition controllers, etc).
  - Ans #2: **Programmable logic.**

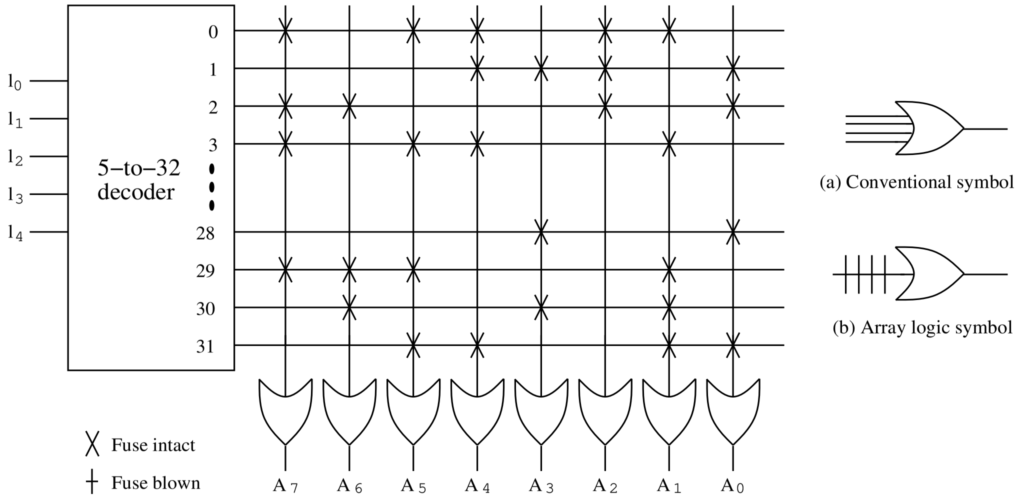
Programmable Logic Family

1. **Simple Programmable Logic Device (SPLD)** (mostly, 2-level)
   - **Read Only Memory (ROM):** A **fixed** array of **AND** gates and a **programmable** array of **OR** gates.
   - **Programmable Logic Array (PLA):** A **programmable** array of **AND** gates feeding a **programmable** array of **OR** gates.
   - **Programmable Array Logic (PAL):** A **programmable** array of **AND** gates feeding a **fixed** array of **OR** gates.
2. **Complex Programmable Logic Device (CPLD):** Multiple SPLDs incorporated on a single chip with programmable switching network interconnecting them.
3. **Field Programmable Gate Array (FPGA):** A **(re)programmable** logic device that can be used to implement multi-level logic and configured by the end users.

- Devices may be
  - **Permanently programmed** at the time of IC manufacture,
  - **Programmed at the time of use**, or
  - **Dynamically re-programmed** during use

Read Only Memory (ROM)

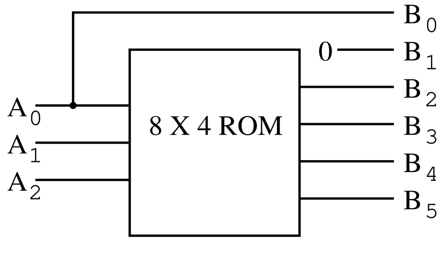
- ROM or Programmable ROM (PROM) have n **input,** m **output** lines and 2^n decoded minterms.



ROM Implementation

- Implement the circuit that accepts a 3-bit number and generates an output binary number equal to the square of the input number.

Inputs			Outputs						
A_2	A_1	A_0	B_5	B_4	B_3	B_2	B_1	B_0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	1
0	1	0	0	0	0	1	0	0	4
0	1	1	0	0	1	0	0	1	9
1	0	0	0	1	0	0	0	0	16
1	0	1	0	1	1	0	0	1	25
1	1	0	1	0	0	1	0	0	36
1	1	1	1	1	0	0	0	1	49



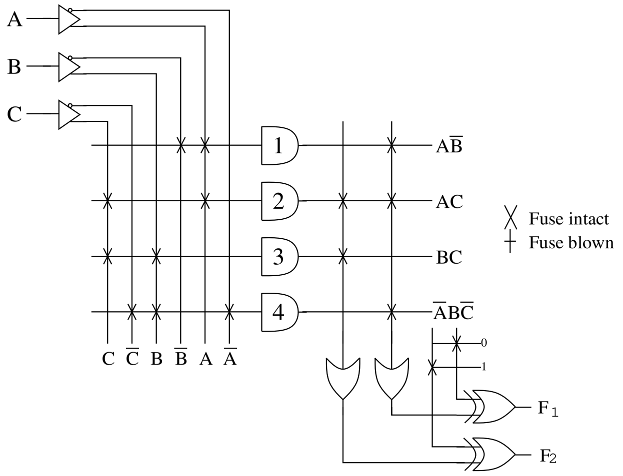
Block diagram

Programmable Logic Array (PLA)

- The AND terms limit the application of a PLA, so try to reduce the # of AND terms to fit in a PLA.

- Implement $F_1 = A\bar{B} + AC + \bar{A}B\bar{C}$ and $F_2 = \overline{AC + BC}$.

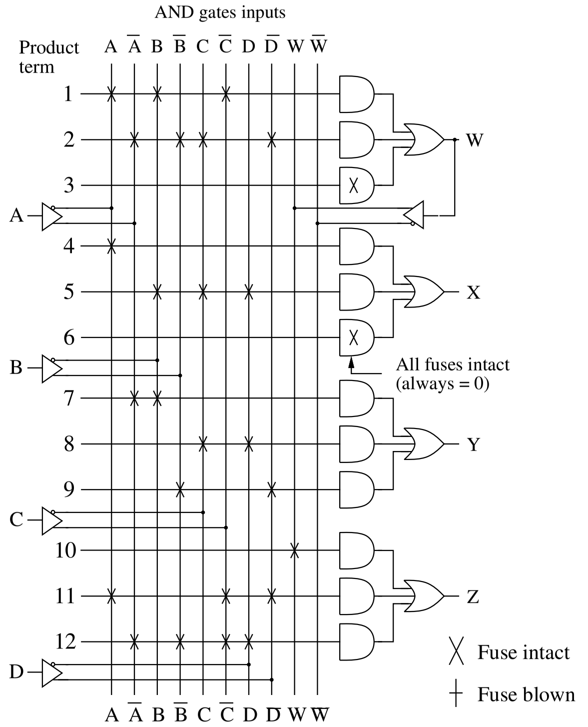
	Product term	Inputs A	Inputs B	Inputs C	Outputs (T) F_1	Outputs (C) F_2
$A\overline{B}$	1	1	0	–	1	–
AC	2	1	–	1	1	1
BC	3	–	1	1	–	1
$\overline{A}B\overline{C}$	4	0	1	0	1	–



Programmable Array Logic (PAL)

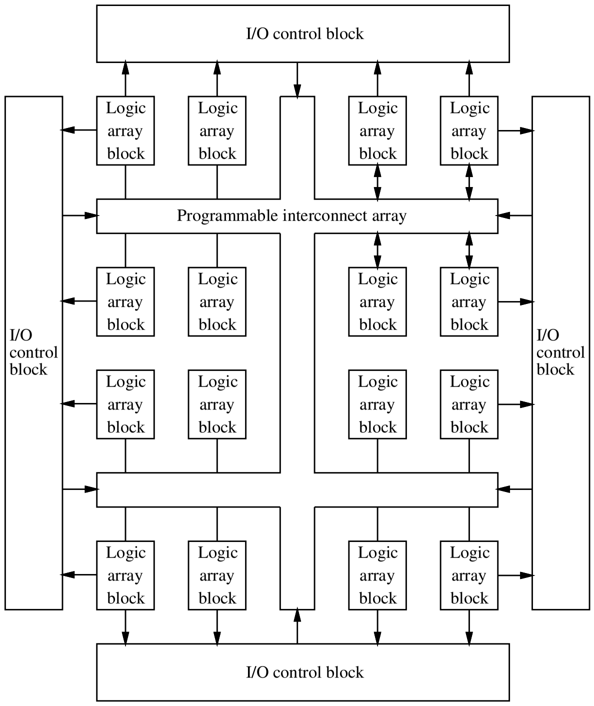
- The OR terms limit the application of a PAL, so try to reduce the # of OR terms to fit in a PAL.

Product term	AND inputs A	B	C	D	W	Outputs
1	1	1	0	–	0	W = $AB\overline{C}$
2	0	0	1	0	–	+ $\overline{A}\overline{B}C\overline{D}$
3	–	–	–	–	–	
4	1	–	–	–	–	X = A
5	–	1	1	1	–	+ BCD
6	–	–	–	–	–	
7	0	1	–	–	1	Y = $\overline{A}B$
8	–	–	1	1	–	+CD
9	–	0	–	0	–	+$\overline{B}\overline{D}$
10	–	–	–	–	–	Z = W
11	1	–	0	0	–	+ $A\overline{C}\overline{D}$
12	0	0	0	1	–	+$\overline{A}\overline{B}\overline{C}D$



Complex Programmable Logic Device (CPLD)

- A programmable logic device that incorporates multiple SPLDs on a single chip with programmable switching network interconnecting them.



Field Programmable Gate Array (FPGA)

- A **(re)programmable** logic device that can be used to implement multi-level logic and configured by the end users.