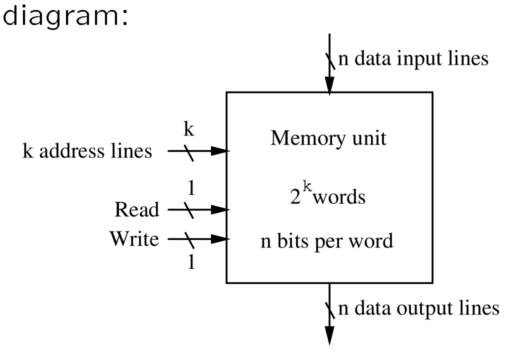
Memory Organization

- A memory block diagram:



- A memory of 10 address bits, 16 data bits (1024 × 16 memory; $k = 10, n = 16$):

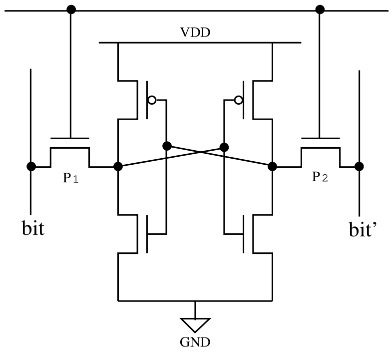
Memory address: Binary	Memory address: Decimal	Memory contents
0000000000	0	10110101 01011100
0000000001	1	10101011 10001001
0000000010	2	00001101 01000110
	⋮	⋮
1111111101	1021	10011101 00010101
1111111110	1022	00001101 00011110
1111111111	1023	11011110 00100100

Types of Memory

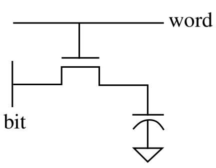
- **Read-only memory (ROM):**
  - ROM can perform only the memory **read** operation.
  - A programmable logic device (PLD) that stores information by **programming** the device.
  - Electrically or UV-erasable ROMs allow the ROM to be erased, then reprogrammed many times.
  - Erasable ROMs require special processing.
- **Random-access memory (RAM):**
  - RAM can perform both the **read** and the **write** operations.
  - RAM takes the same time to access memory. (**Serial memory** takes different times to access information, e.g., disk, tape.)
- **Volatile memory:** Memory units that **lose** stored information when power is turned off.
  - SRAM, DRAM, etc.
- **Non-volatile memory:** Memory units that **retain** stored information when power is turned off.
  - ROM, PROM, EPROM, EEPROM, **flash memory**, disk, etc.

SRAM and DRAM

- **Static RAM (SRAM)** consists of internal latches that stores the binary information.
  - The stored information remains valid as long as power is applied to the RAM.
- **Dynamic RAM (DRAM)** stores the binary information in the form of electric charges on capacitors.
  - The capacitors must be periodically recharged by **refreshing** the DRAM.
- Capacity: DRAM/SRAM $\approx$ 4–8; Cycle time: DRAM/SRAM $\approx$ 8–16; Cost: SRAM/DRAM $\approx$ 8–16.
- Typical applications: Cache $\longleftrightarrow$ SRAM; Main memory $\longleftrightarrow$ DRAM.



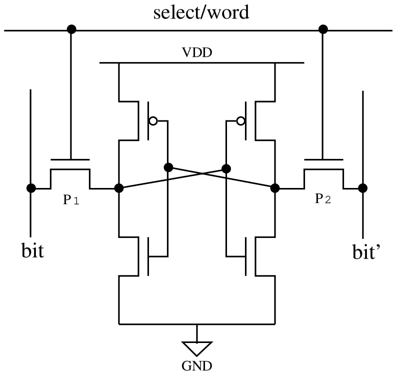
SRAM cell



DRAM cell

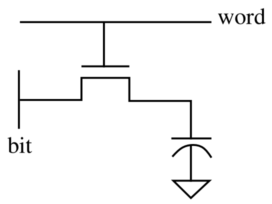
Static RAM

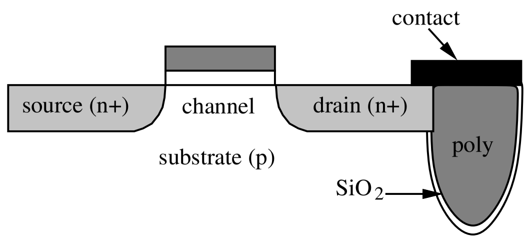
- Core cell typically uses 6-transistor circuit to store value.
- Value is stored symmetrically; both true and complement are stored on cross-coupled transistors.
- Read
  - Precharge bit and bit' to V_{DD}.
  - Set $select$ line high from row decoder.
  - One bit line will be pulled down.
- Write
  - Set bit and bit' lines to desired values.
  - Set $select$ line high.
  - Drive on bit lines will flip state if necessary.



One-Transistor DRAM Cell

- Value is stored on a capacitor.
- DRAM loses value due to charge leakage; must be refreshed periodically.
- Popular in embedded systems (embedded microprocessor/memory).
- Read
  - Precharge *bit* line to V_{DD}.
  - Activate *word* line.
  - The value stored on the capacitor is passed to *bit* line.
- Write
  - Set *word* line high to connect *bit* line and capacitor.
  - Set *bit* accrodingly and force capacitor to proper value.

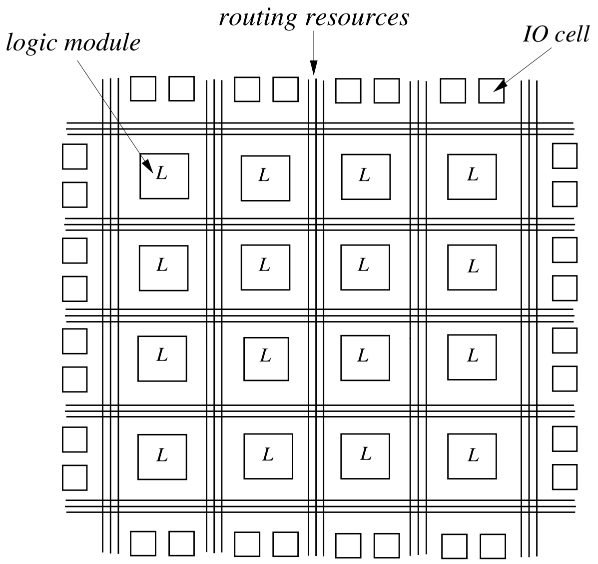




FPGAs

- A new chip technology (Xilinx 1985).
- A (re)programmable logic device that implements multi-level logic.
- Programmed by users to implement circuit designs.
- No fabrication step.
  - Low prototyping cost.
  - Short manufacturing time.
- High density (million gates).
- Disadvantages: larger chip size, slower speed.
- Popular applications: prototyping, FPGA-based computers, on-site hardware reconfiguration, DSP, logic emulation, network components, etc.

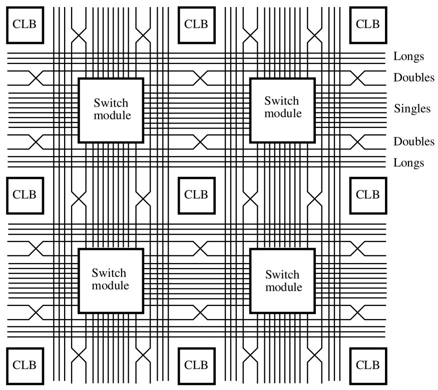
The Conceptual FPGA Architecture



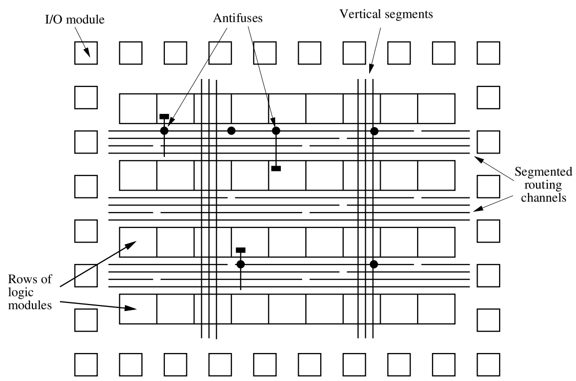
- Logic modules + Routing resources + I/O cells = FPGAs.

Popular FPGA Architectures

- Array-based: Lucent Technolgies, Xilinx, etc.
- Row-based: Actel, etc.



(a) Array–based.

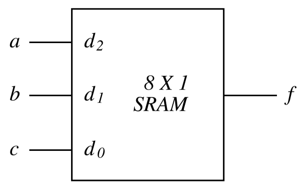


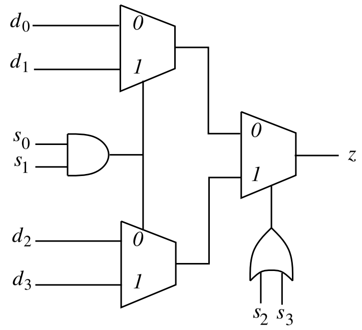
(b) Row–based.

Logic Module Architecture

- Lookup table-based: a segment of SRAM (Exp: function $f = ab + \overline{a}c$)
  - Limited input size (typically, 3–5)
- Multiplexer-based: (function $z = \overline{(s_3 + s_2)}\,\overline{s_1 s_0} d_0 + \overline{(s_3 + s_2)} s_1 s_0 d_1 + (s_3 + s_2)\overline{s_1 s_0} d_2 + (s_3 + s_2) s_1 s_0 d_3$)
  - Function $f = ab + \overline{a}c$: setting $d_0 = \times, d_1 = \times, d_2 = c, d_3 = b, s_0 = a, s_1 = 1, s_2 = 1, s_3 = \times$.

a	b	c	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

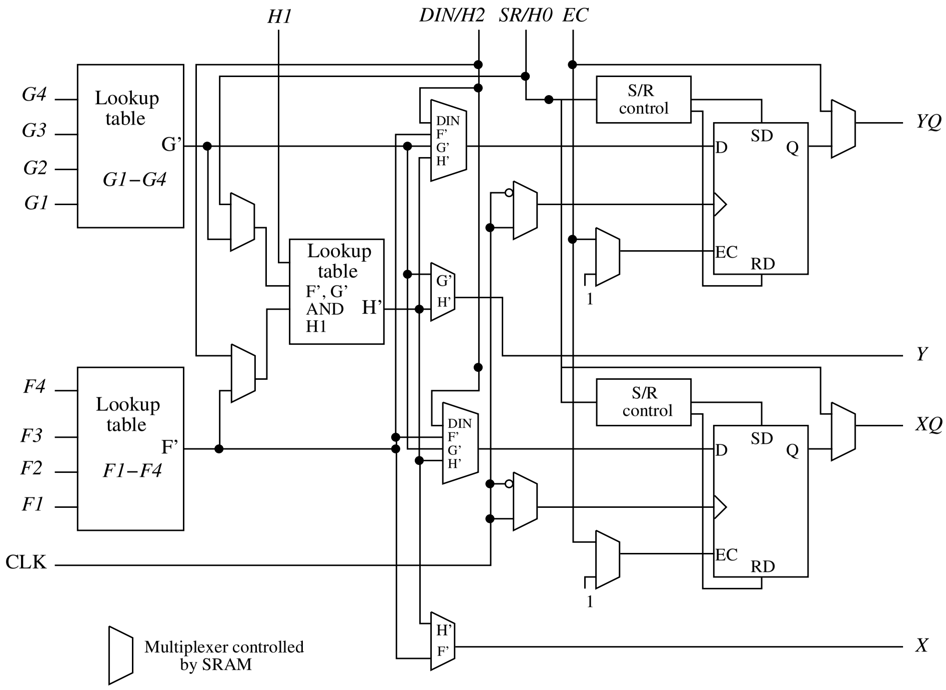




(a) Lookup table–based logic module and SRAM. (b) Multiplexer–based logic module.

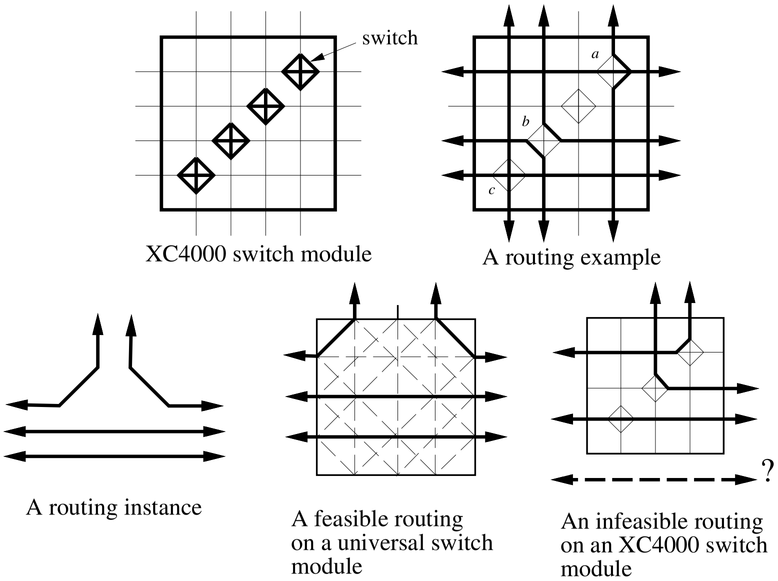
Xilinx XC4000 Logic Block Revisited

- Two 4-input LUTs and one 3-input LUT.



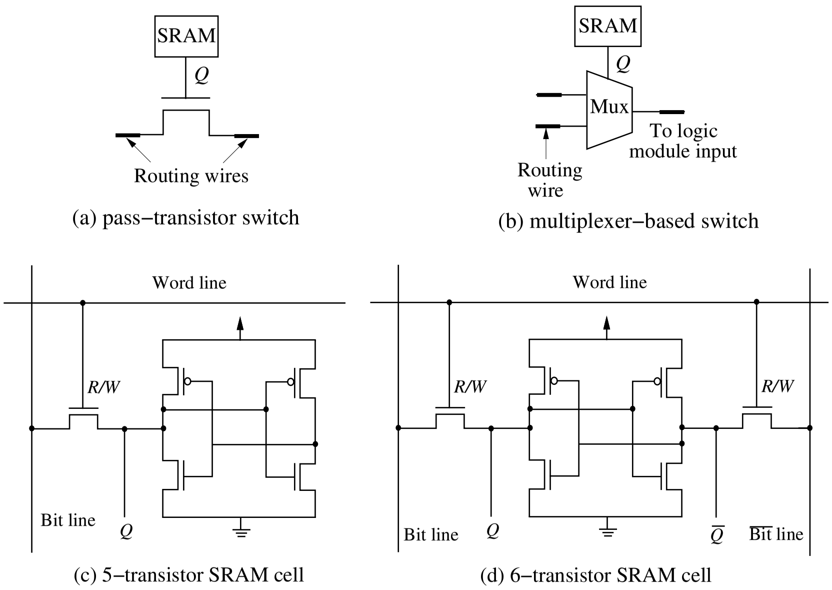
Switch-Module Architecture

- Each switching point on the diagonal of an XC4000 switch module contains six switches.
- The universal switch module can accommodate up to 25% more routing instances than the Xilinx XC4000 one.



Programming Technology: SRAM

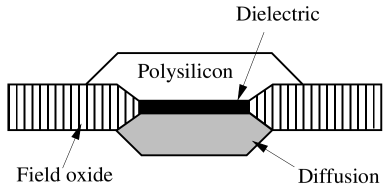
- Reconfigurable.
- Larger area, higher resistance/capacitance (larger delay), lower power consumption.



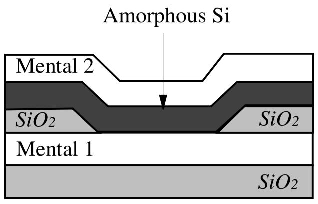
(a) pass–transistor switch
(b) multiplexer–based switch
(c) 5–transistor SRAM cell
(d) 6–transistor SRAM cell

Programming Technology: Antifuse

- Normal state: high impedance; higher-than-normal voltage: low impedance.
- One-time programmable.
- Smaller area, lower resistance/capacitance (higher performance), larger power consumption.



(a) Actel PLICE antifuse.



(b) QuickLogic ViaLink antifuse.

Programming Technology Summary

- Based on the 0.5 μm technology.

Programming technology	SRAM	PLICE anti-fuse	ViaLink anti-fuse
Manufacturing Complexity	+	–	–
Reprogrammable?	Yes in circuit	No	No
Physical size	Large (12X)	Small (2X)	Small (1X)
ON resistance (Ω)	600–800	100–500	30–80
OFF capacitance (fF)	10–50	3–5	1
Power consumption	++	+	+
Volatile?	Yes	No	No

FPGA Design Process