Chapter 2: Transistors and Layout

- **Reading:**
  - Wolf: Chapter 2.1 → Chapter 2.2 → Chapter 3.3.1 → Chapter 2.6 → Chapter 2.5 → Chapter 2.3 → Chapter 2.4
- **Supplementary material:**
  - Weste & Eshraghian: Chapter 1.3–1.5, Chapter 3.2, Chapter 2.1.

Conductivity of Materials

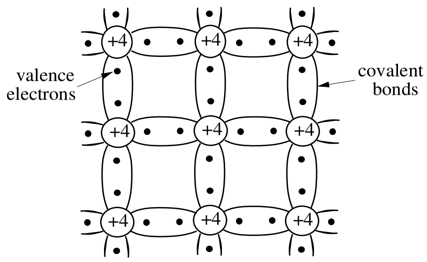
- **Insulator:** material with practically no available charge carriers.
- **Conductor:** material with large number of mobile carriers.
- **Semiconductor:** material with conductivities between those of insulators and conductors.
- **Drift velocity** U of carriers:

$$U = \sigma E,$$

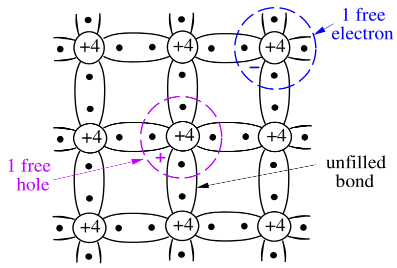
  σ: conductivity; E: electric field.
- Properties of the semiconducting material determine limits on the performance of the technology, e.g., Silicon (Si) v.s. Gallium Arsenide (GaAs).
  - $\sigma_{GaAs} > \sigma_{Si}$.

Conductivity

- As temperature ≈ absolute zero
  - The electrons in the outer shell are tightly bound
  - No free electrons, and silicon is an insulator
- At higher temperature (300°K)
  - Some electrons have enough thermal energy that can break some covalent bonds.
  - When a covalent bond is broken, there is a negatively charged free **electron** and a positively charged **hole**.
- Conduction in semiconductors is due to electrons and holes drifting in opposite directions under the influence of an electric field.



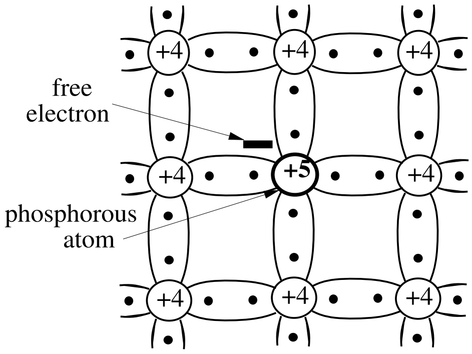
Silicon lattice with no free electron



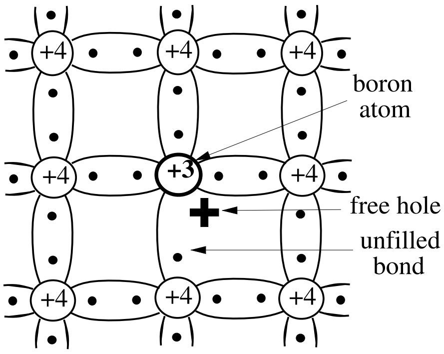
Silicon lattice with one covalent bond broken

Doping

- The number of electrons and holes are equal in a **pure** semiconductor (e.g., pure silicon).
- Pure silicon may be mixed with other elements (**impurities**) to change the number of available carriers.
- **N-type** silicon are doped with atoms of valence +5, e.g., phosphorous atoms (n+: heavily doped; n−: lightly doped).
- **P-type** silicon are doped with atoms of valence +3, e.g., boron atoms (p+: heavily doped; p−: lightly doped).

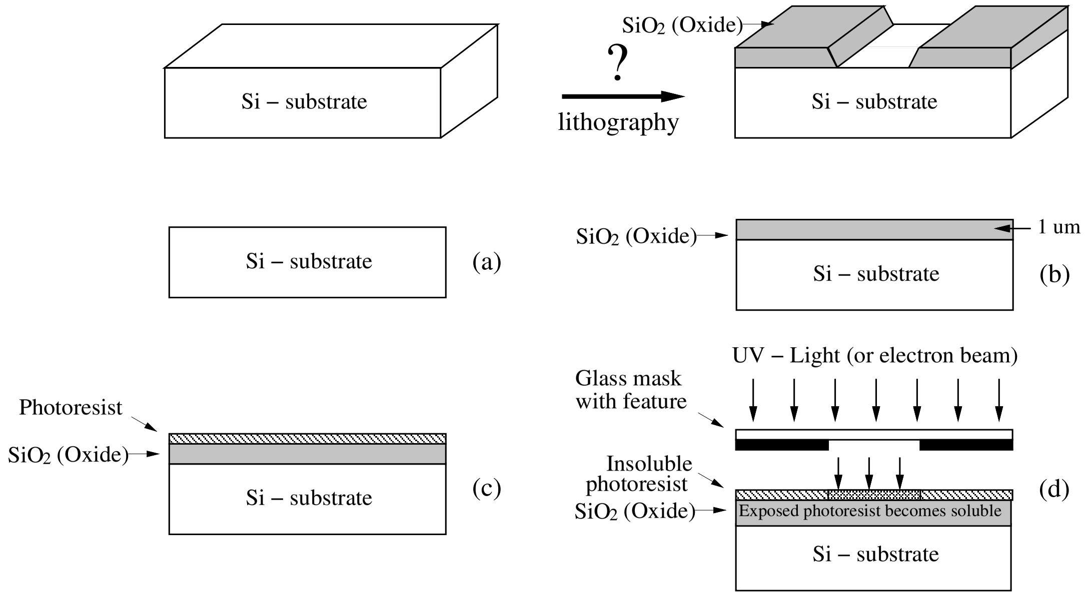


effect of n–type doping



effect of p–type doping

Basic Fabrication Flow



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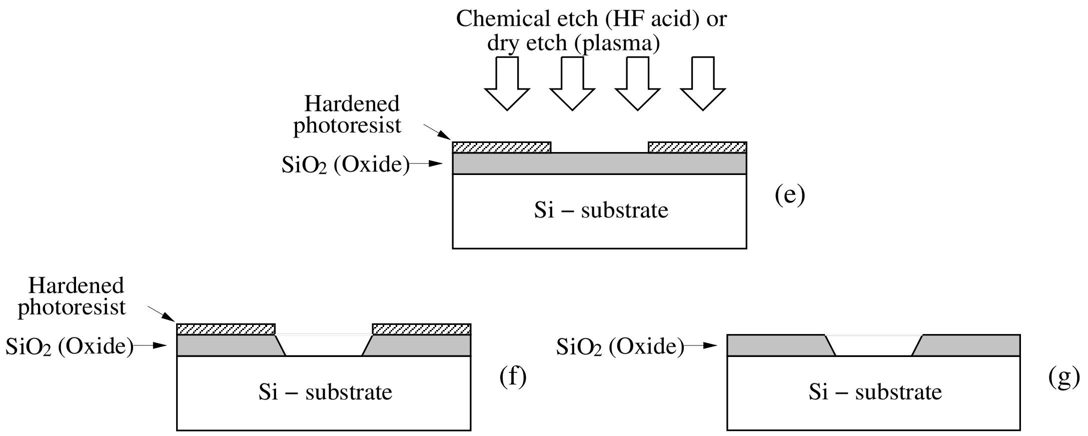
Basic Fabrication Flow (cont'd)



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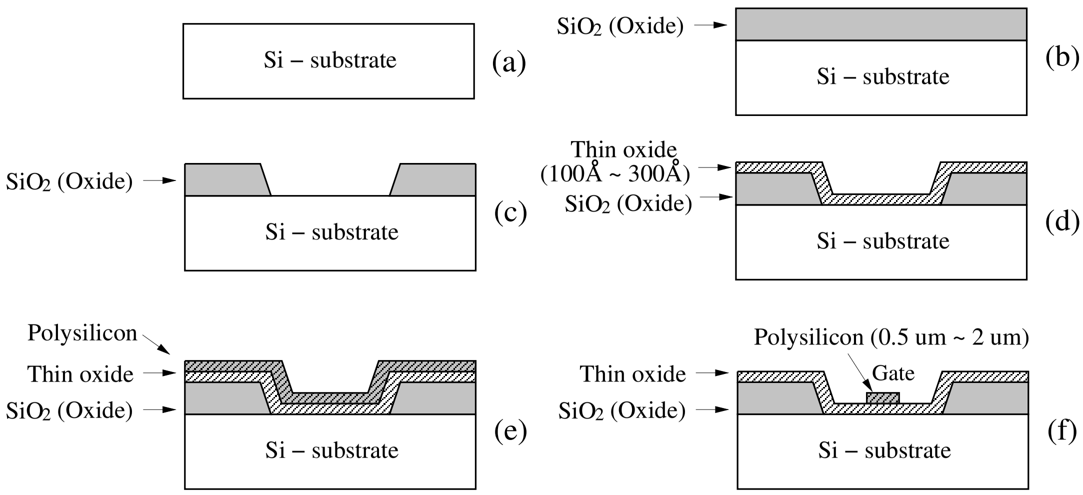
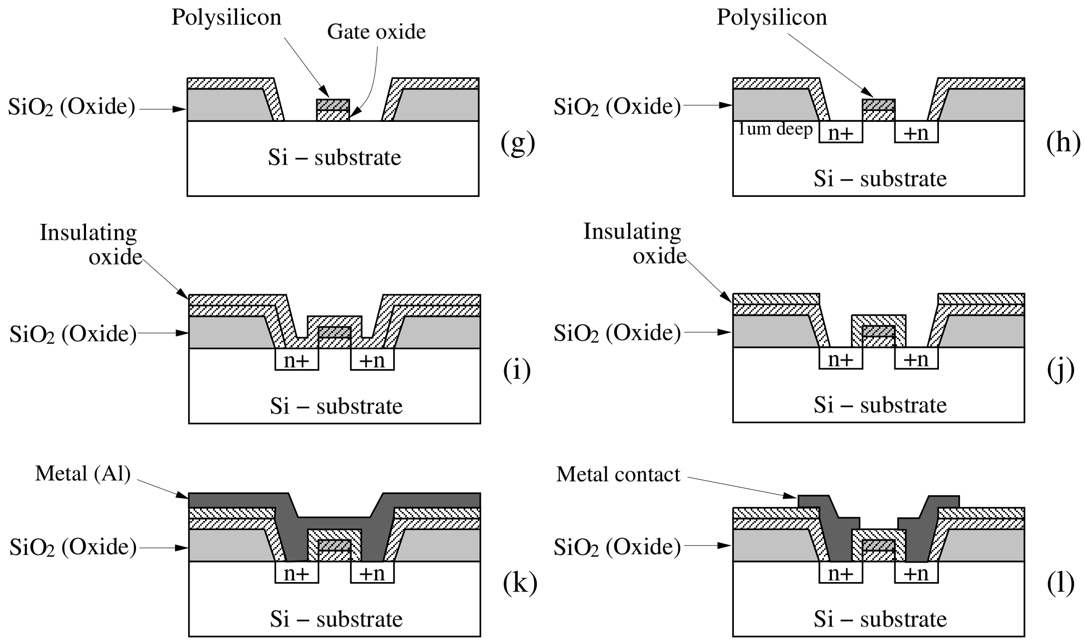
nMOS Transistor Fabrication

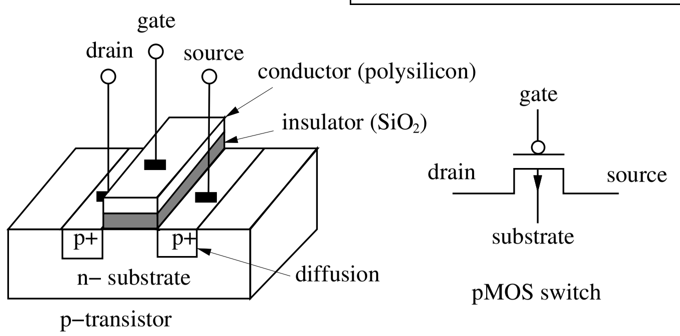
- n-type Metal-Oxide-Semiconductor (nMOS) transistor fabrication flow



nMOS Transistor Fabrication Flow (cont'd)

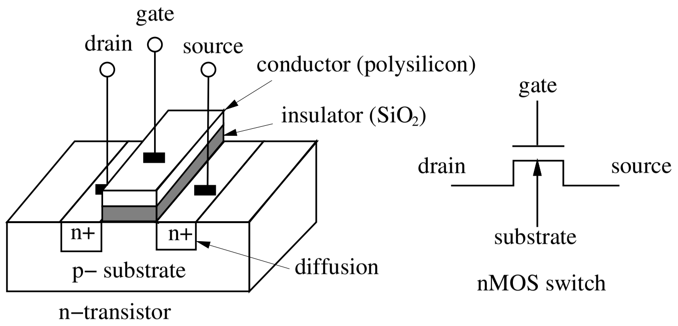


MOS Transistors



- control input: gate
- switch terminals: drain, source (physically equivalent)
- apply zero voltage to gate ==> switch ON

The pMOS switch passes signal "1" well.

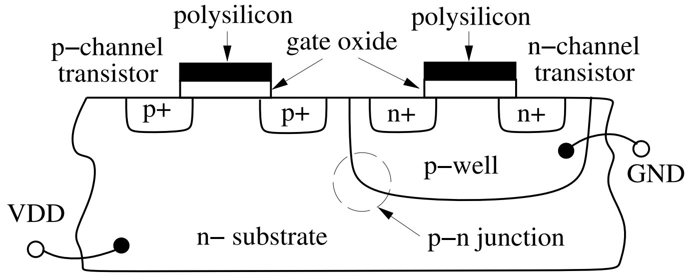


- apply > threshold voltage to gate ==> switch ON

The nMOS switch passes signal "0" well.

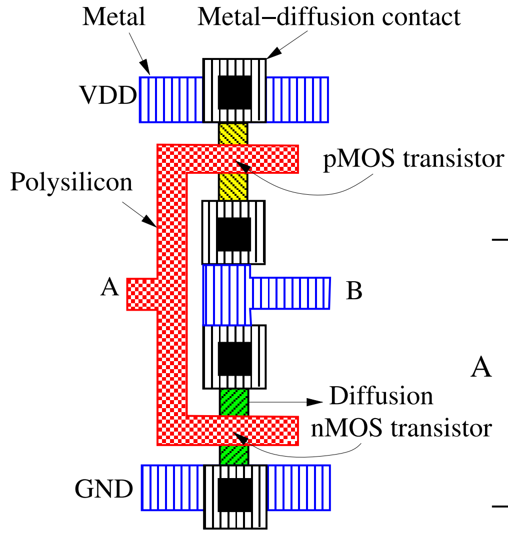
Complementary MOS (CMOS)

- The most popular VLSI technology (v.s. Bipolar CMOS (BiCMOS), nMOS, pMOS).
- CMOS uses both n-channel and p-channel transistors.
- CMOS dominates BiCMOS, nMOS and pMOS, due to CMOS's lower power dissipation, high regularity, reliable performance, high noise margin, larger fanout, etc.
- CMOS logic circuits draws nearly zero standby power consumption.
- Each type of transistor must sit in a material of the complementary type (the reverse-biased diodes prevent unwanted current flow).



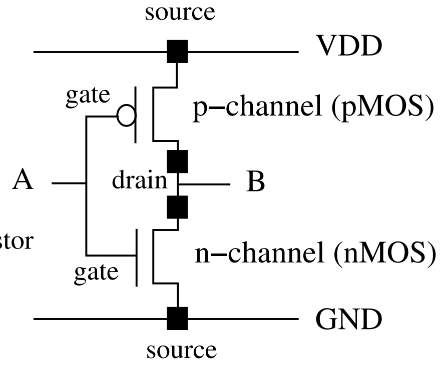
p−well CMOS structure

A CMOS Inverter



layout

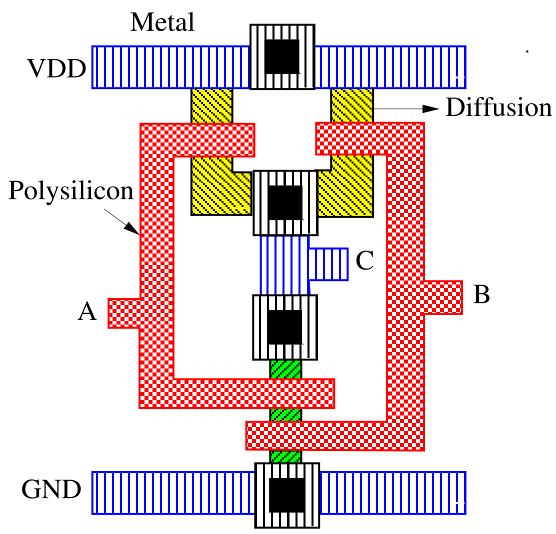
A	B
1	0
0	1



metal 1: blue — polysilicon: red — p–diffusion: yellow (p–well: light yellow)

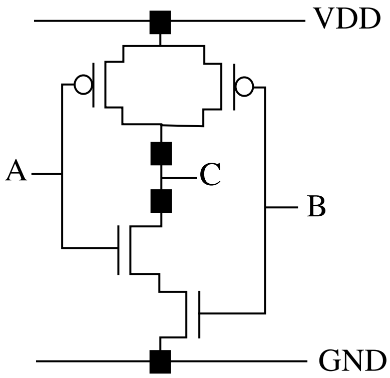
metal 2: brown — contact/via: black — n–diffusion: green (n–well: light green)

A CMOS NAND Gate

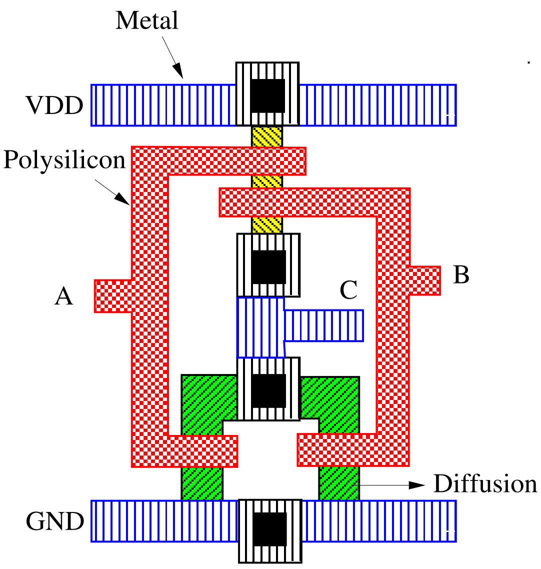


layout

in1 A	in2 B	out C
0	0	1
0	1	1
1	0	1
1	1	0

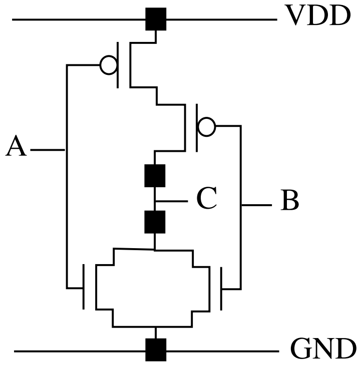


A CMOS NOR Gate

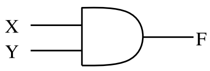
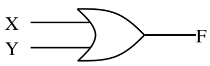
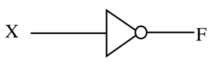
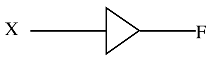
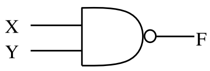
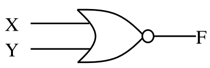
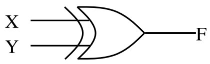


layout

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

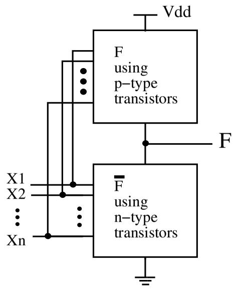


Basic CMOS Logic Library

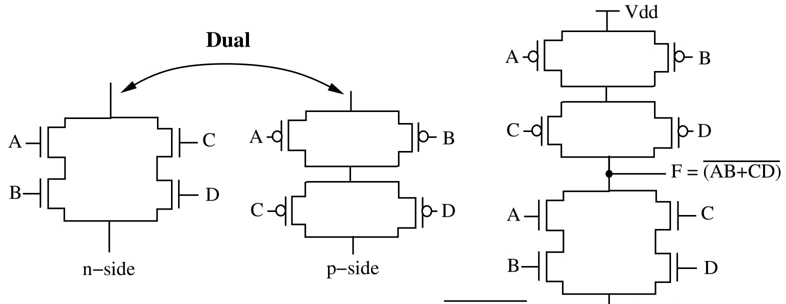
Name	Distinctive shape	Algebraic equation	Cost (# of transistors)	Scaled gate delay (ps)
AND		$F=XY$	**6**	**24**
OR		$F=X+Y$	**6**	**24**
NOT (inverter/ repeater)		$F=\overline{X}$	**2**	**10**
Buffer (driver/ repeater)		$F=X$	**4**	**20**
NAND		$F=\overline{XY}$	**4**	**14**
NOR		$F=\overline{X+Y}$	**4**	**14**
Exclusive−OR (XOR)		$F=X\overline{Y}+\overline{X}Y$ $=X\oplus Y$	**14**	**42**

Construction of Compound Gates

- Example: $F = \overline{A \cdot B + C \cdot D}$.
- Step 1 (**n**-network): **Invert** F to derive n-network ($\overline{F} = A \cdot B + C \cdot D$).
- Step 2 (n-network): Make connections of transistors:
  - AND $\Longleftrightarrow$ Series connection; OR $\Longleftrightarrow$ Parallel connection.
- Step 3 (**p**-network): Expand F to derive p-network ($F = \overline{AB + CD} = \overline{AB} \cdot \overline{CD} = (\overline{A} + \overline{B}) \cdot (\overline{C} + \overline{D})$); **each input is inverted.**
- Step 4 (p-network): Make connections of transistors (same as Step 2).
- Step 5: Connect the n-network to GND (typically, 0V) and the p-network to VDD (5V, 3.3V, or 2.5V, etc).



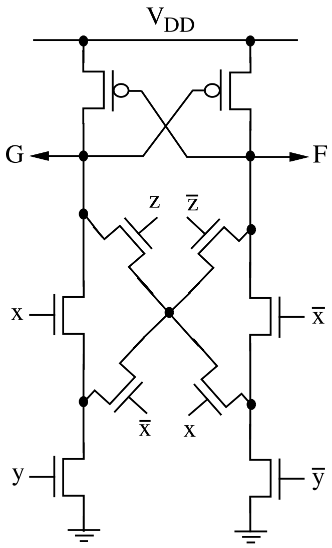
General Structure



CMOS compound gate for F = $\overline{(AB + CD)}$

A Complex CMOS Gate

- The functions realized by the n and p networks must be complementary, and one of the networks must conduct for every input combination.
- Duality is not necessary.



x	y	z	F	G
0	0	0	0	1
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

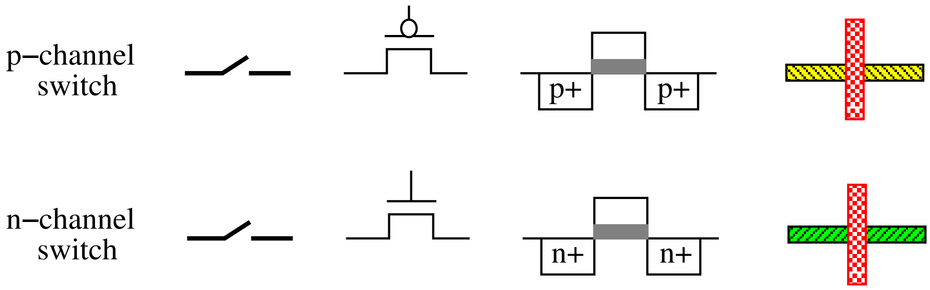
F = ?
G = ?

CMOS Properties

- There is always a path from one supply (VDD or GND) to the output.
- There is never a path from one supply to the other. (This is the basis for the low power dissipation in CMOS—virtually no static power dissipation.)
- There is a momentary drain of current (and thus power consumption) when the gate switches from one state to another.
  - Thus, CMOS circuits have dynamic power dissipation.
  - The amount of power depends on the switching frequency.

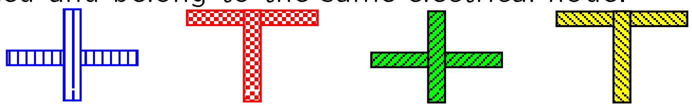
Stick Diagram

- Intermediate representation between the transistor level and the mask (layout) level.
- Gives topological information (identifies different layers and their relationship)
- Assumes that wires have no width.
- Possible to translate stick diagram automatically to layout with correct **design rules**.

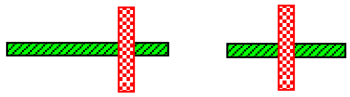


Stick Diagram (cont'd)

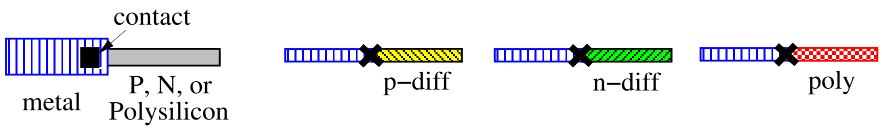
- When the same material (on the same layer) touch or cross, they are connected and belong to the same electrical node.



- When **polysilicon** crosses N or P **diffusion**, an N or P transistor is formed.
  - Polysilicon is drawn on top of diffusion.
  - Diffusion must be drawn connecting the source and the drain.
  - Gate is automatically self-aligned during fabrication.

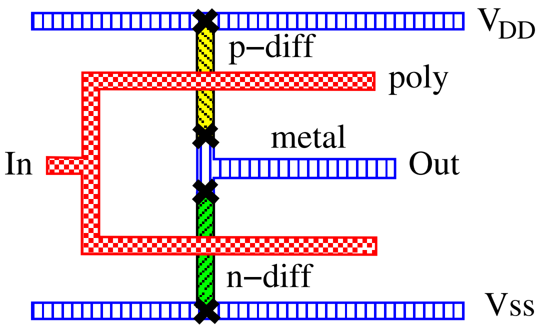


- When a metal line needs to be connected to one of the other three conductors, a **contact** cut (**via**) is required.

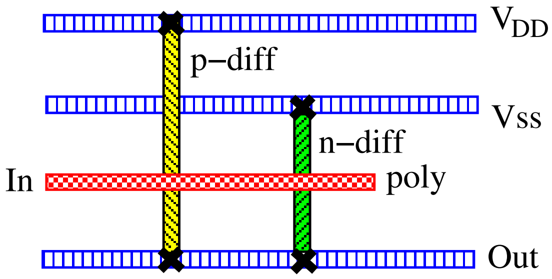


CMOS Inverter Stick Diagrams

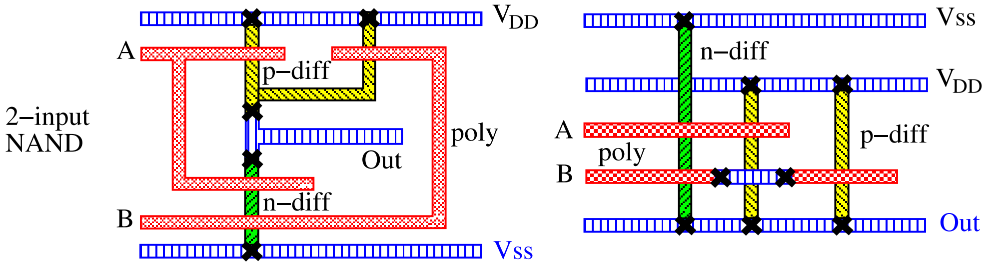
- Basic layout



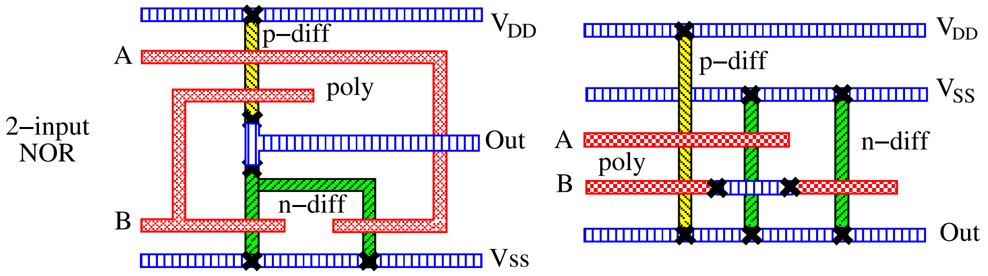
- More area efficient layout



CMOS NAND/NOR Stick Diagrams



area efficient? contacts?

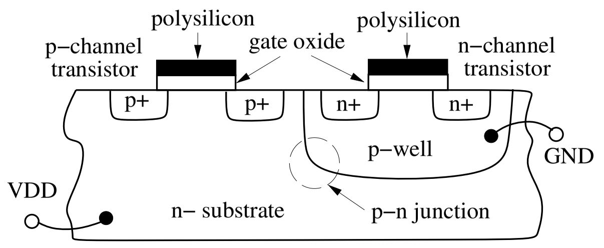


Dominant CMOS Technologies

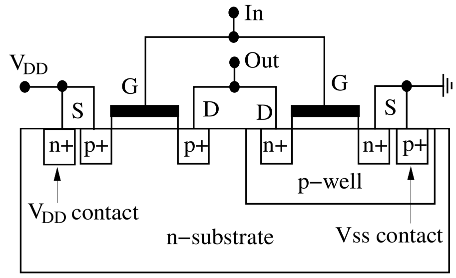
- Four CMOS structures
  - p-Well (p-tub)
  - n-Well (n-tub)
  - Twin-well (twin-tub)
  - Silicon On Insulator (SOI)

Typical p-Well Fabrication Flow

- Start with n substrate (donor $N_d = 10^{15}/cm^3$)
- Form p-well region (Brown mask) (acceptor $N_a = 3 \times 10^{16}/cm^3$)
- Define pMOS and nMOS active regions (Green mask)
- Form field and gate oxidations
- Form polysilicon (Red mask)
- Implant p+ diffusion (Yellow mask)
- Implant n+ diffusion (Green mask)
- Create contact cut (Black mask)
- Metalization (Blue mask)

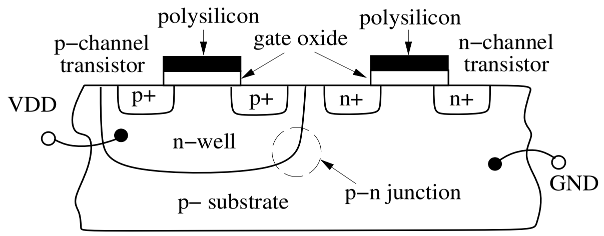


p−well CMOS structure

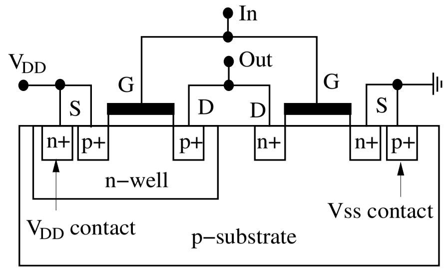


Typical n-Well Fabrication Flow

- Start with p substrate
- Form n-well region
- Define pMOS and nMOS active region
- Form field and gate oxidations
- Form polysilicon
- Implant n+ diffusion
- Implant p+ diffusion
- Create contact cut
- Metalization

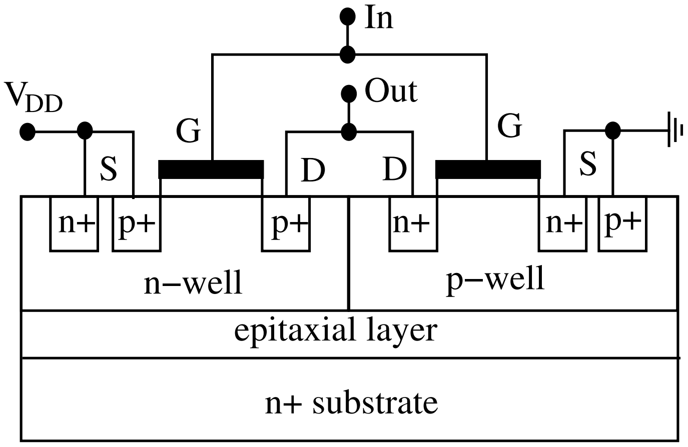


n−well CMOS structure



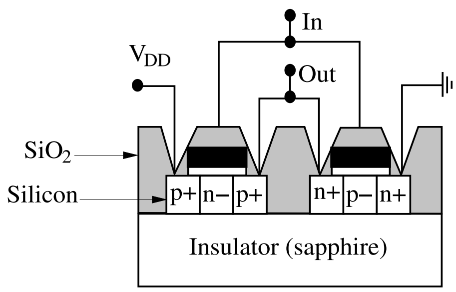
Twin-Well Structure

- Add an epitaxial (EPI) layer between n/p wells and the substrate (n+ or p+) for protection against **latch-up** (shorting of V_{DD} and V_{SS}).
- Similar to p-well process (but with both a p-well and an n-well).

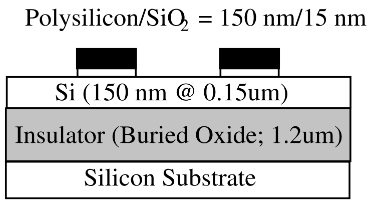


Silicon On Insulator (SOI) Structures

- Old days: Deposits a thin layer of silicon on an insulator; diffusions penetrate through the silicon layer to the insulator surface.
- Nowadays: The insulator is based on a buried oxide layer.
- Advantages
  - Free of latch-up problem.
  - Low voltage, low power.
  - Offers the highest CMOS operating frequencies.
- Disvantages
  - More complex process flow, higher cost.



Silicon on Sapphire (SOS)



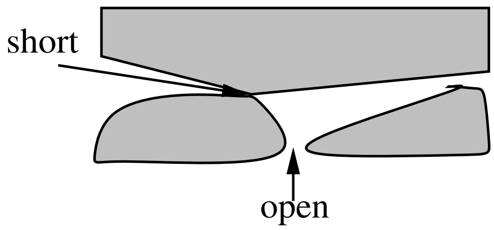
State−of−the−art SOI

Fabrication Problems

- Photoresist shrinkage, tearing.
- Variations in material deposition.
- Variations in oxide thickness.
- Impurities.
- Variations across a wafer.
- Transistor problems
  - Variations in threshold voltage
    - Oxide thickness (100–300 Å@ 0.35–1.0 μm)
    - Ion implantation
    - Poly variation
- Changes in source/drain diffusion overlap.
- Variations in substrate.

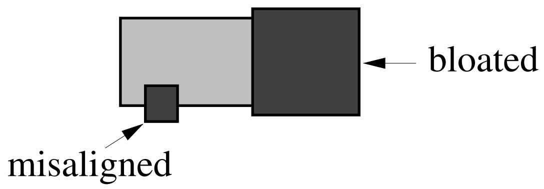
Wiring Problems

- Diffusion: changes in doping cause variations in resistance, capacitance.
- Poly, metal: variations in height, width cause in resistance, capacitance.
- Shorts and opens



Via (Contact) Problems

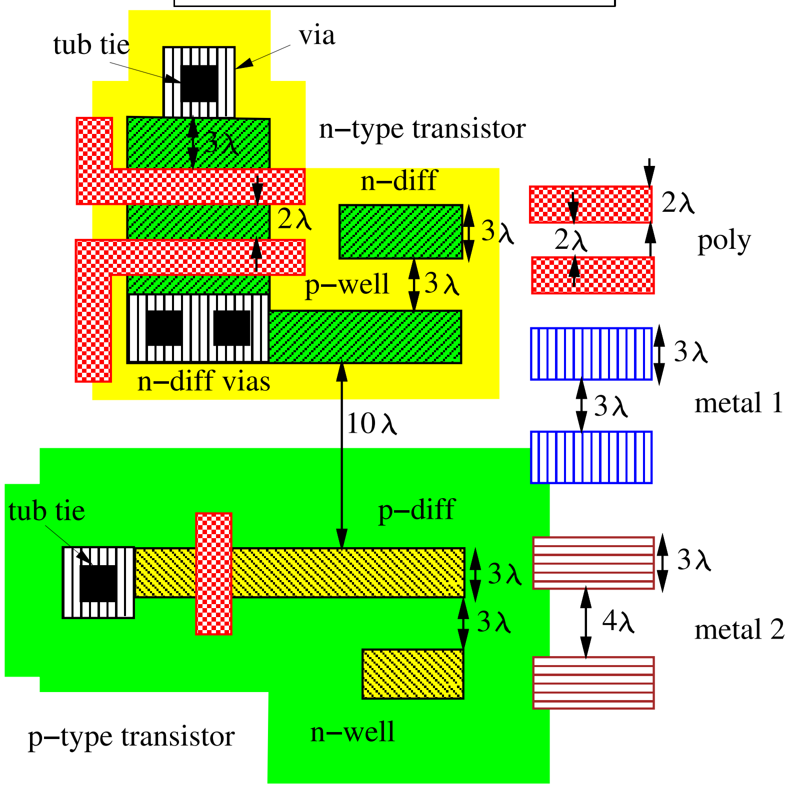
- Via may not be cut all the way through.
- Undersized via has too much resistance.
- Via may be too large and create short.



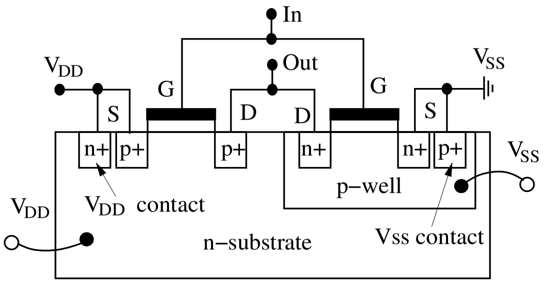
Design Rules

- Layout rules are used for preparing the masks for fabrication.
- Fabrication processes have inherent limitations in accuracy.
- Design rules specify geometry of masks to optimize yield and reliability (trade-offs: area, yield, reliability).
- Three major rules:
  - Wire width: Minimum dimension associated with a given feature.
  - Wire separation: Allowable separation.
  - Contact: overlap rules.
- Two major approaches:
  - "Micron" rules: stated at micron resolution.
  - λ rules: simplified micron rules with limited **scaling** attributes.
- λ may be viewed as size of minimum feature.
- Design rules represents a tolerance which insures very high probability of correct fabrication (not a hard boundary between correct and incorrect fabrication).
- Design rules are determined by experience.

SCMOS Design Rules



V_{DD} (Power) and V_{SS} (Ground)



- V_{DD}: Comes from V_{DD} pads.
  - An n+ diffusion in the n- substrate, connecting a metal line via a contact, gives V_{DD}.
  - All logic must get V_{DD} from a substrate contact.
- V_{SS}: Comes from V_{SS} pads.
  - Connected to the p-well (p- substrate) via metal-to-p+ contact inside the p-well.
  - For every 2 □'s of p-well, there must be at least one metal-to-p+ contact.