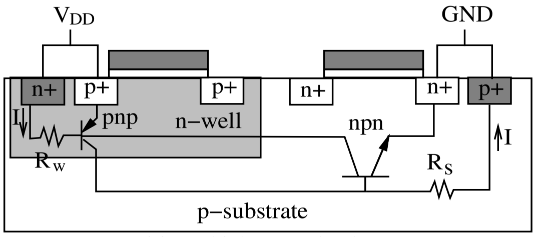
MOSIS Layout Design Rules

- MOSIS design rules (SCMOS rules) are available at http://www.mosis.org.
- 3 basic design rules: Wire width, Wire separation, Contact rule.
- MOSIS design rule examples

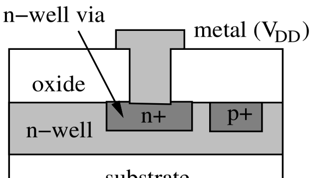
R1	Min active area width	3 λ
R3	Min poly width	2 λ
R4	Min poly spacing	2 λ
R5	Min gate extension of poly over active	2 λ
R8	Min metal width	3 λ
R9	Min metal spacing	3 λ
R10	Poly contact size	2 λ
R11	Min poly contact spacing	2 λ

Latch-up

- CMOS ICs have parasitic silicon-controlled rectifiers (SCRs) (p-to-n path).
- When powered up, SCRs can turn on, creating low-resistance path from power to ground (**latch-up**).
- Current can destroy the transistor.
- Early CMOS problem.
- Use **tub ties** to connect tub (well) to power to solve the latch-up problem.



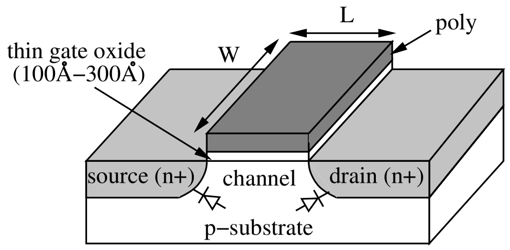
Parasitics which cause latch–up



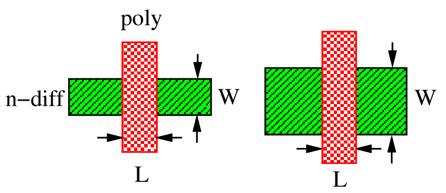
Adding tub ties (vias) to make low–resistance connections to tubs (reduce Rs and Rw) to avoid latch–up (cf. power/ground rules).

n-type Transistor Structure

- **Channel**, the intersection region of poly and diffusion, is where the transistor action take place.
- The gate is insulated from the substrate by the thin silicon dioxide (**gate oxide**) (100–300 Å@ .35–1 μm, resistance $> 10^{12}\Omega$; cf. $1\mu m$ for **field oxide**), so the current through the gate is almost zero.
- When the gate-to-source voltage V_{gs} is zero, p-n junctions form diodes $\Longrightarrow$ no current can flow from the drain to the source.
- When the gate voltage $V_{gs} > V_t$ (**threshold voltage**), enough electrons form an **inversion layer** at the channel boundary $\Longrightarrow$ the source and the drain conduct.
- Current flow is a function of the W/L (width/length) ratio; the greater the ratio, the larger the current (L**: feature size**).



n–type transistor

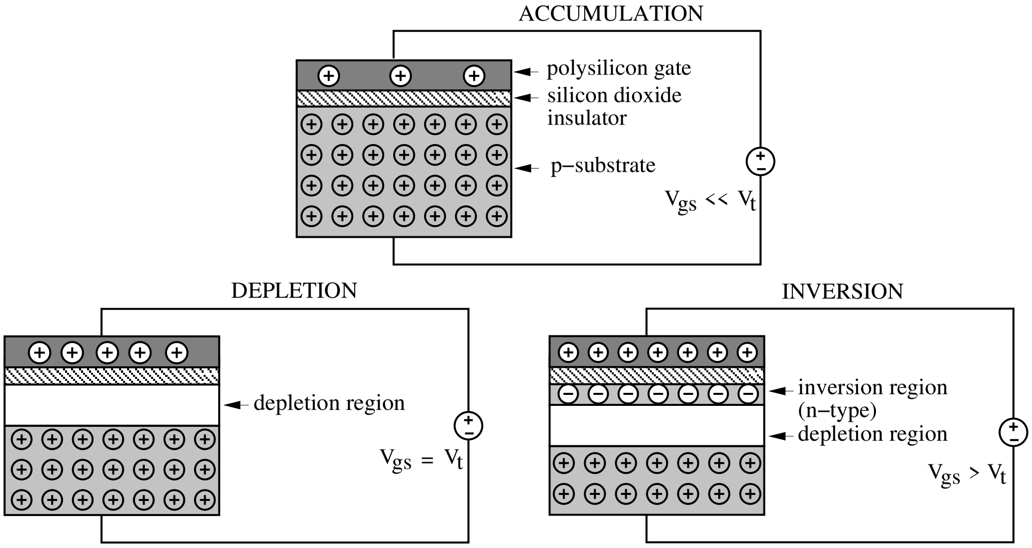


wider (larger) transistor
smaller resistance

nMOS Transistor Operation

- Field plate or gate influences region between the source and drain.
- The horizontal component of the electric field associated with $V_{ds} > 0$ responsible for sweeping electrons from the channel towards the drain.
- A positive voltage on the gate produces an electric field across the substrate which attracts electrons towards the gate and repels holes.
- If sufficient voltage is applied, the region under the gate changes from p-type to n-type and provides a conduction path between the source and drain (surface of the underlying p-type silicon is said to be **inverted**).
- Gate voltage at which conduction takes place is termed the **Threshold voltage** V_t.
- Current flow occurs when the drain-to-source voltage $V_{ds} > 0$, and it consists of almost electrons that flow from the source to drain in the channel.
- A **depletion region** devoid of mobile carries insulates the channel from the rest of substrate.

Modes in nMOS Structure

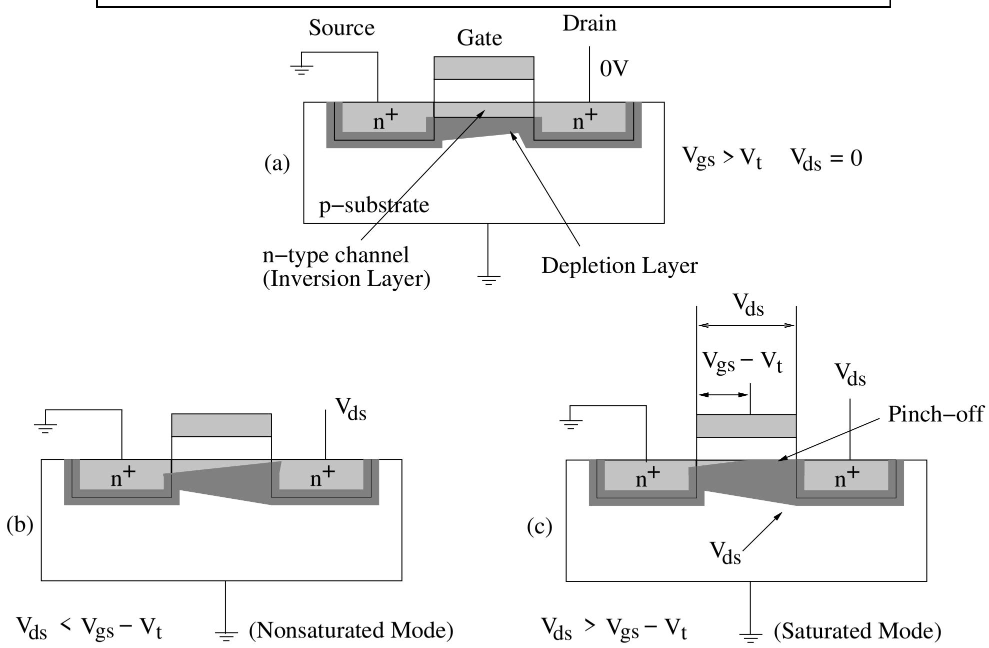


- PN junction v.s. the inversion layer-substrate junction
  - **PN junction:** the n-type conductivity is brought about by a fabrication process; i.e., the electrons are introduced into the semiconductor by the introduction of donor ions.
  - **Inversion layer-substrate junction:** the n-type layer is induced by the electric field applied to the gate; i.e., a field-induced junction.

nMOS Transistor Operation (cont'd)

- As V_{ds} is increased, the resistive drop along the channel begins to change the shape of the channel.
- At source end of the channel, the full gate voltage is effective in inverting the channel.
- At drain end of the channel, only the difference between the gate and the drain voltage is effective.
- If $V_{ds} > V_{gs} - V_t$, then $V_{gd} < V_t$ and the channel becomes "pinched off" (i.e., the channel no longer reaches the drain). However, conduction is done by electron drift under the influence of positive drain voltage: as the negative electrons leave the channel, they are subsequently accelerated towards the drain.
- Voltage across the pinch-off channel tends to remain fixed at $(V_{gs} - V_t)$. As a result, the channel current remains constant with increasing V_{ds} (**saturated** state).

Channel Shape under Different Voltages



Drain Current I_{ds} Characteristics

- **Cutoff region:** $V_{gs} < V_t$

$$I_{ds} = 0$$

- **Linear region:** $V_{ds} < V_{gs} - V_t$

$$I_{ds} = \beta\left((V_{gs} - V_t)V_{ds} - \frac{1}{2}V_{ds}^2\right)$$

- **Saturated region:** $V_{ds} \geq V_{gs} - V_t$

$$I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2$$

  – V_{gs} (V_{ds}): gate-to-source (drain-to-source) voltage
  – I_{ds}: current between the drain and source
  – V_t: transistor **threshold voltage**
  – β: **Transistor gain factor** $\left(\beta = k'\frac{W}{L}\right)$
  – k': transistor **transconductance** $\left(k' = \frac{\mu\varepsilon}{t_{ox}} = \frac{\partial I_{ds}}{\partial V_{gs}}\Big|_{V_{ds}=constant}\right)$ (μ: carrier mobility; ε: **permittivity** of the gate insulator; transconductance unit: siemens/mho)
  – W/L: width-to-length ratio

Drain Current I_d Characteristics (cont'd)

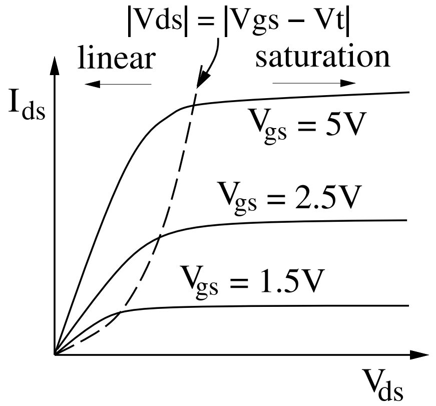
- **Linear region:** $V_{ds} < V_{gs} - V_t$

$$I_{ds} = \beta\left((V_{gs} - V_t)V_{ds} - \frac{1}{2}V_{ds}^2\right)$$

- **Saturated region:** $V_{ds} \geq V_{gs} - V_t$

$$I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2$$

where $\beta = k'\frac{W}{L}$.



	k'	V_t
n–type	$k'_n = 73\ \mu A/V^2$	0.7V
p–type	$k'_p = 21\ \mu A/V^2$	–0.8V

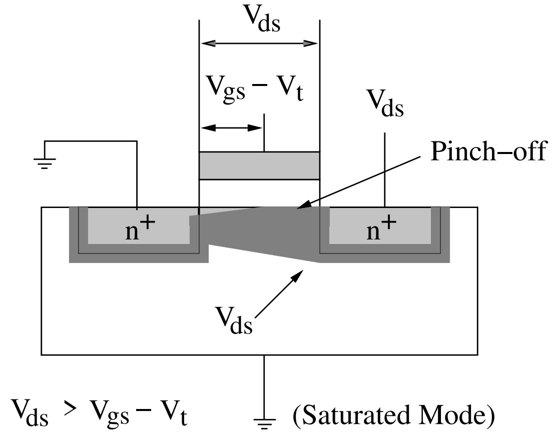
0.5 μm parameters

Channel Length Modulation

- Increasing V_{ds} in saturation causes the channel to shorten slightly, which slightly increases the drain-to-source current.
- **Channel length modulation factor** λ describes small dependence of the drain-to-source current on V_{ds} in saturation.

$$I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2(1 + \lambda V_{ds})$$

where $\lambda \in [0.005V^{-1}, 0.02V^{-1}]$.

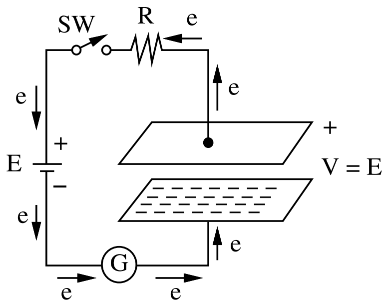


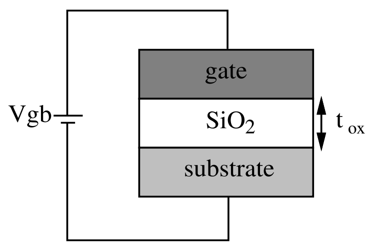
MOS Gate as Capacitor

- Basic structure of gate is parallel-plate capacitor.
- Parallel-plate oxide capacitance per unit area (F/cm^2):

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

  - ε_{ox}: **permittivity** of silicon dioxide ($\approx 3.9\varepsilon_0$; $\varepsilon_0 = 8.85 \times 10^{-14} F/cm$)
  - t_{ox}: oxide thickness in cm.
- Related formulae: $C = Q/V$; 1 Farad = 1 Coulomb / Volt.
- Gate capacitance helps determine charge in channel which forms inversion region.





Values and Formulae

Charge of an electron	q	1.6×10^{-19} Coulomb
Si intrinsic (undoped) carrier concentration	n_i	$1.45 \times 10^{10}/cm^3$
Permittivity of free (empty) space	ε_0	$8.85 \times 10^{-14} F/cm$
Permittivity of Si	ε_{si}	$11.8\varepsilon_0 = 1.06 \times 10^{-12} F/cm$
Permittivity of silicon dioxide	ε_{ox}	$3.9\varepsilon_0 = 3.45 \times 10^{-13} F/cm$
Boltzmann's constant	k	$1.38 \times 10^{-23} J/^{\circ}K$
Thermal voltage ($T = 300^{\circ}K$)	kT/q	0.026 V
p-substrate (**a**cceptor) doping concentration	N_a	$10^{16}/cm^3$
n-substrate (**d**onor) doping concentration	N_d	$10^{15}/cm^3$
Oxide thickness	t_{ox}	100Å–300Å

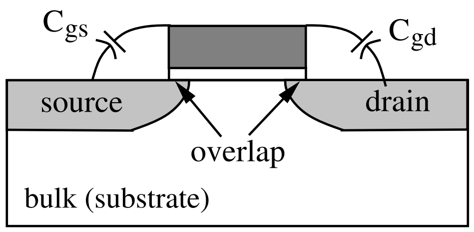
- $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$.
- $C = Q/V$; 1 Farad = (1 Coulomb) / (1 Volt).
- $W = N \cdot m$; 1 Joule = (1 Newton) · (1 Meter).
- $V = W/Q$; 1 Volt = (1 Joule) / (1 Coulomb).
- $P = W/t$; 1 Watt = (1 Joule) / (1 Second).
- Relative permittivity (dielectric constant): $\varepsilon_r\varepsilon_0$.

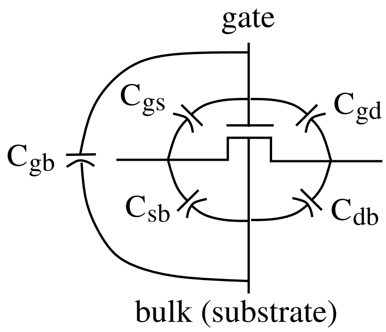
Basic Transistor Parasitics

- Gate to substrate, also gate to source/drain.
- Source/drain **capacitance**, resistance.
- **Gate capacitance** C_g is determined by active area ($W \times L \times c_g$; c_g: unit capacitance).
- **Source/drain overlap capacitances** C_{gs}, C_{gd} are determined by source/gate and drain/gate overlaps (C_{ol} per unit width overlap capacitance):

$$C_{gs} = C_{ol} W.$$

- Gate/bulk overlap capacitance.





Threshold Voltage

- The voltage at which the # of minority carriers (electrons in an n-transistor) in the channel equals that of majority carriers in the substrate (cut-off if I_{ds} equals zero or not).
- Four major components (source-substrate voltage $V_{sb} = 0$):

$$V_{t0} = V_{fb} + \phi_s + V_{pp} + V_{ii}.$$

1. **Flatband voltage:** $V_{fb} = \Phi_{gb} - Q_f / C_{ox}$
   - Φ_{gb}: difference in work function between the gate material and silicon substrate ($\Phi_g - \Phi_{si}$).
     * If the gate polysilicon is n-doped at a concentration of N_{dp},

$$\Phi_{gb} = -\frac{kT}{q} \ln \left(\frac{N_a N_{dp}}{n_i^2} \right).$$

     * If the gate polysilicon is p-doped at a concentration of N_{ap},

$$\Phi_{gb} = \frac{kT}{q} \ln \left(\frac{N_{ap}}{N_a} \right).$$

   - Q_f: fixed surface charge due to imperfections in the silicon-oxide interface and doping.

Threshold Voltage (cont'd)

$$V_{t0} = V_{fb} + \phi_s + V_{pp} + V_{ii}.$$

2. **Surface potential:** ϕ_s is about twice the difference between the Fermi energy levels (potential) ϕ_F of the doped and intrinsic semiconductors.

$$\phi_s \approx 2|\phi_F| = 2\frac{kT}{q}\ln\frac{N_a}{n_i}$$

   – **Fermi energy level:** energy at which the probability of occupation by an electron is 1/2.

3. **Voltage across the parallel-plate capacitor**: V_{pp}

$$V_{pp} = \frac{Q_b}{C_{ox}} = \frac{\sqrt{2q\varepsilon_{si}N_a\phi_s}}{C_{ox}}.$$

4. **Additional ion implantation**: V_{ii}

$$V_{ii} = \frac{qD_i}{C_{ox}}$$

   – D_i: ion implantation concentration.

Body Effect

- **Body effect:** Variation of threshold voltage with non-zero source-substrate voltage (i.e., $V_{sb} \neq 0$).

$$V_t = V_{t0} + \Delta V_t.$$
$$\Delta V_t = \gamma(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}).$$

- **n**-type transistor (**p**-substrate; **a**cceptor) body effect factor: $\gamma = \gamma_n$

$$\gamma_n = \frac{\sqrt{2q\varepsilon_{si}N_a}}{C_{ox}}.$$

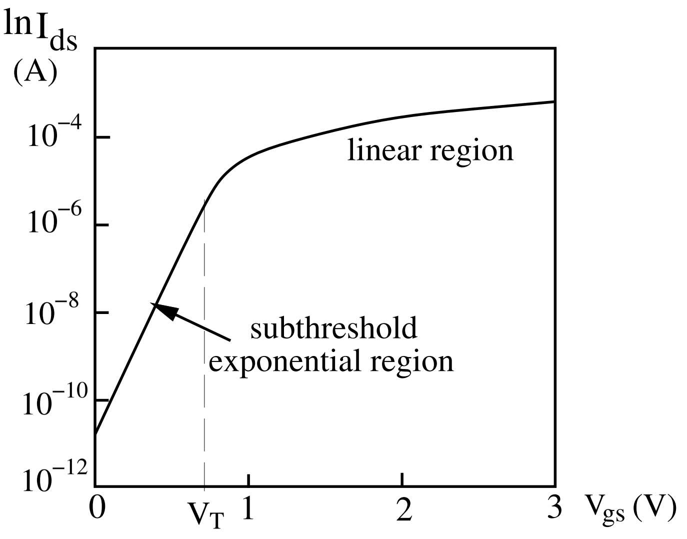
- **p**-type transistor (**n**-substrate; **d**onor) body effect factor: $\gamma = \gamma_p$

$$\gamma_p = \frac{\sqrt{2q\varepsilon_{si}N_d}}{C_{ox}}.$$

- Body effect may affect the speed of complex logic gates.

Subthreshold Current

- **Subthreshold current** (the current when $V_{gs} < V_t$) is an exponential function of V_{gs}.
- Subthreshold conduction affects the design of dynamic gates since the subthreshold current changes the charge stored in the gate.



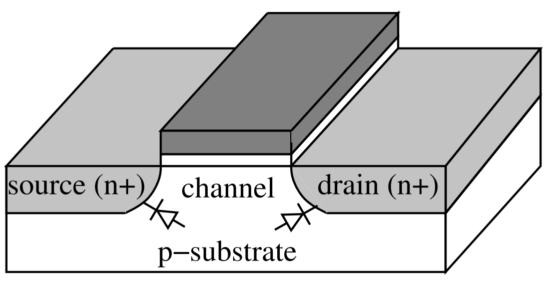
Leakage Current

- Flow from the source or drain to the substrate due to diode formed by junction.
- General form of leakage current is given by diode law:

$$I_l = I_{l0}\left(e^{qV_d/kT} - 1\right)$$

I_{l0}: reverse saturation current ($\approx$ 30 nA)
q: electronic charge ($1.6 \times 10^{-19} C$)
k: Boltzmann's constant ($1.38 \times 10^{-23} J/^{\circ}K$)
T: temperature

- Leakage currents are the source of static power dissipation in CMOS circuits.

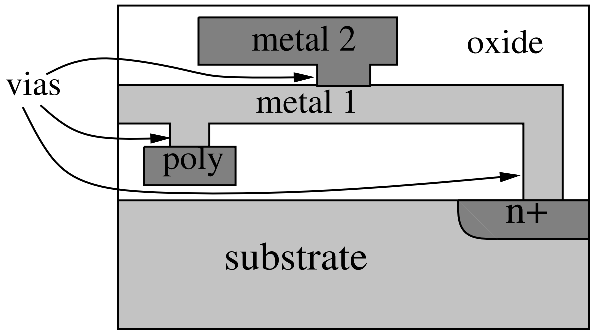


Wire Issues

- Metal lines, with limited current-carrying capacity, are used to supply power throughout a chip.
- **Metal migration (electromigration):** Under high current, electron collisions with metal grains cause the metal to move.
- **Mean time to failure (MTF, MTTF):** the time for 50% of testing sites to fail:

$$MTF \;=\; j^{-n} e^{Q/kT}$$

  j: current density; $n \in [1,3]$; Q: diffusion activation energy.
- Metal wires can handle 1.5 mA per μm width.



The MOS Resistor

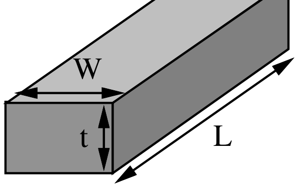
- The resistance of a bar of uniform material:

$$R \;=\; \frac{\rho L}{A} = \left(\frac{\rho}{t}\right)\left(\frac{L}{W}\right)$$

  - ρ: resistivity of the material
  - L: length of the resistor
  - W: width of the material
  - A: cross-section (area) of the resistor
  - t: thickness of the material
- The channel resistance of a MOS transistor (linear region):

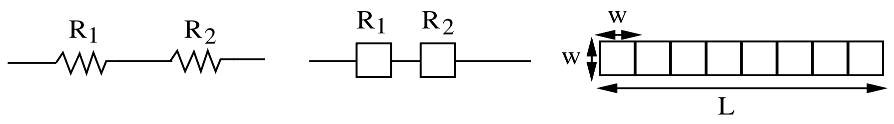
$$R_c \;=\; k\left(\frac{L}{W}\right)$$

  where $k = \frac{1}{\mu C_{ox}(V_{gs} - V_t)}$ (μ: carrier mobility).

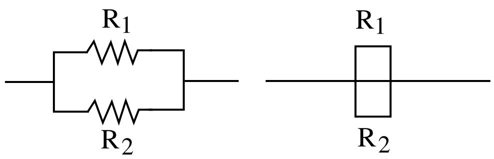


Resistors Connected in Series and Parallel

- Series
  - Equivalent resistance: $R = R_1 + R_2$.
  - Any resistor pattern on the photomask can be divided into squares of dimension W on each side.
  - The number of squares in any pattern is equal to the ratio L/W.
  - Resistance = $r\times$ # of $\square$'s = rL/W.



- Parallel
  - Equivalent resistance: $R = \frac{1}{\frac{1}{R_1}+\frac{1}{R_2}}$.
  - Resistance = $r\times$ (# of $\square$'s)$^{-1}$ = rL/W.

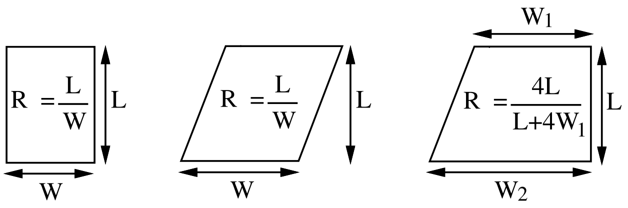


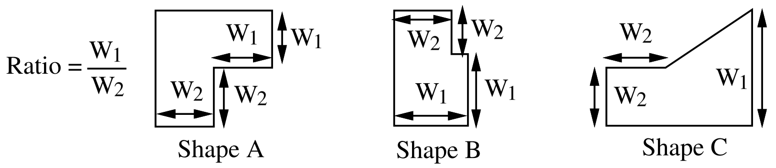
Typical Sheet Resistance

- Table is based on the 0.5–1 μm CMOS technology.
- Check the SIA roadmap for the values for various technologies.

Material	Sheet resistance (Ω/square)		
	Min	Typical	Max
Inter-metal (metal1–metal2)	0.05	0.07	0.10
Top-metal (metal3)	0.03	0.04	0.05
Polysilicon	15	20	30
Diffusion (n+, p+)	10	25	100
n-well	1K	2K	5K

Resistance of Non-rectangular Regions





Shape A		Shape B		Shape C	
Ratio	Resistance	Ratio	Resistance	Ratio	Resistance
1.0	2.50	1.5	2.10	1.5	1.45
1.5	2.55	2.0	2.25	2.0	1.80
2.0	2.60	3.0	2.50	3.0	2.30
3.0	2.75	4.0	2.65	4.0	2.65

Load Capacitance Estimation

- The total load capacitance on the output of a gate is the sum of
  - **Gate capacitance** (of other inputs connected to this output)
  - **Diffusion (thin-oxide) capacitance** (of the source/drain regions connected to the output)
  - **Routing capacitance** (of connections between the output and other inputs)
- Understanding the source of parasitic loads and their variations is essential in the design process.

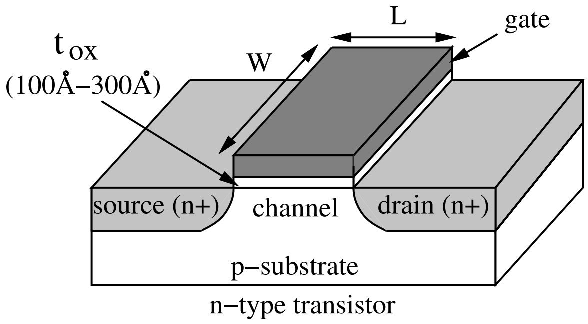
Gate Capacitance

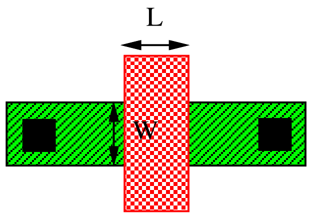
- Gate capacitance: $C_g = C_{ox} \cdot A$ ($C_{ox} = \varepsilon_{ox}/t_{ox}$).
  - ε_{ox}: permittivity of silicon dioxide ($\approx 3.9\varepsilon_0$)
  - t_{ox}: oxide thickness.
  - A: area of gate.
- With a thin-oxide thickness of 100 $\rightarrow$ 200 Å,

$$C_{ox} = \frac{3.9 \times 8.85 \times 10^{-14}}{(100 \rightarrow 200) \times 10^{-8}} \approx (35 \rightarrow 17) \times 10^{-4} pF/\mu m^2.$$

- Exp: If $W = 4\mu m, L = 1\mu m, t_{ox} = 100$ Å,

$$C_g = 4 \times 35 \times 10^{-4} pF \approx 0.014 pF.$$





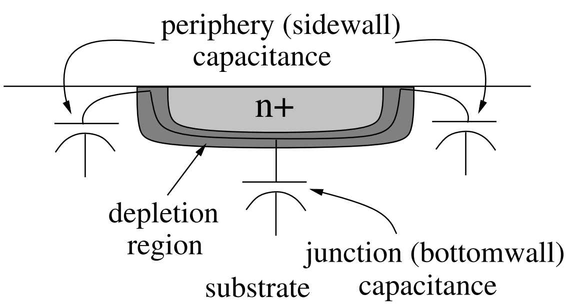
Diffusion Capacitance

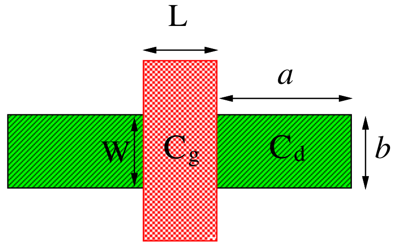
- The total diffusion (thin-oxide) capacitance C_d:

$$\begin{aligned} C_d &= C_{ja} \times diffusion\_area + C_{jp} \times diffusion\_perimeter \\ &= C_{ja} \cdot (ab) + C_{jp} \cdot (2a + 2b) \end{aligned}$$

  - C_{ja}: Junction (bottomwall) capacitance / μm^2
  - C_{jp}: Periphery (sidewall) capacitance / μm

0.5 μm parameters	n-diffusion wire	p-diffusion wire
C_{ja}	0.6 $fF/\mu m^2$	0.9 $fF/\mu m^2$
C_{jp}	0.2 $fF/\mu m$	0.3 $fF/\mu m$



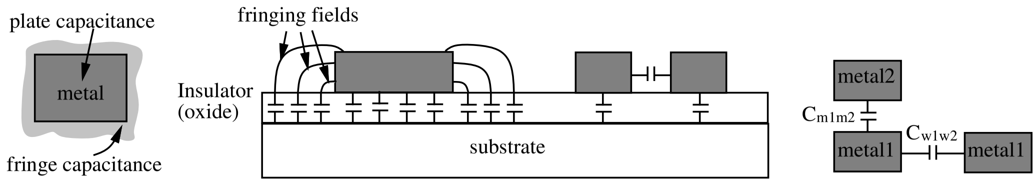


Routing Capacitance

- Routing capacitance is usually computed using the **parallel-plate approximation**: $C_r = \varepsilon A/t$
  - A: area of capacitor
  - t: insulator thickness
  - ε: permittivity (dielectric constant) of insulator
- Other factors that modify this approximation
  - **Fringe capacitance**
  - Interelectrode capacitance (e.g., poly-metal)
- Considering plate and fringe capacitances,

$$C_r = C_p \times area + C_f \times perimeter$$

  - C_p: plate capacitance / μm^2 (0.5μm :$\approx$ 0.04$fF/\mu m^2$)
  - C_f: fringe capacitance / μm (0.5μm :$\approx$ 0.09$fF/\mu m$)



Typical CMOS Capacitances

- Table is based on the 1 μm n-well CMOS technology.
- Check the SIA roadmap for the values of various technologies.

Parameter	Capacitance (Atto farads /μm^2)	Comments
C_{jan}	300	n-diffusion area—varies with process
C_{jpn} ($aF/\mu m$)	400	n-diffusion periphery—varies
C_{jap}	500	p-diffusion area—varies with process
C_{jpp} ($aF/\mu m$)	400	p-diffusion periphery—varies
C_{gs}	1800	gate cap.—increases as t_{ox} thins
C_p	50	poly over field oxide
C_{m1}	30	metal1 over field oxide
C_{m1p}	60	metal1 to poly
C_{m1d}	60	metal1 to diffusion
C_{m2}	20	metal2 to substrate
C_{m2m1}	50	metal2 to metal1
C_{m2p}	30	metal2 to poly
C_{m3}	10	metal3 to substrate
C_{m3m2}	30	metal3 to metal2
C_{m3m1}	15	metal3 to metal1
C_{m3d}	10	metal3 to diffusion