National Chiao Tung University November 7, 2000
Dept. of Computer & Information Science Handout #10
Introduction to VLSI Design, Fall 2000 Yao-Wen Chang

Practice Exam (1999 Final Exam)

Instructions. This is a two-hour open-book, open-note test, to be graded out of 100. There are ten parts of questions. **Pace Yourself and Good Luck!**

Question 1. (12 pts)

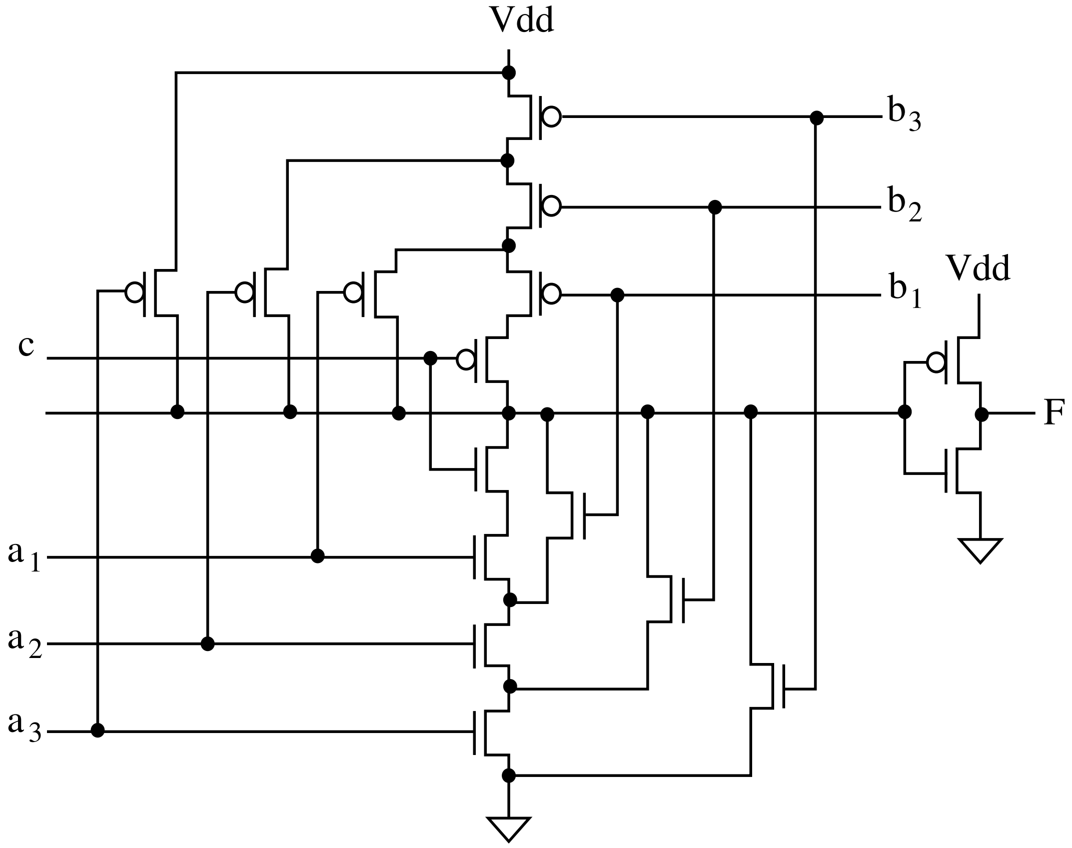


Figure 1: A CMOS circuit.

(a) (6 pts) The figure above shows a CMOS circuit implementing the function F. Write the logic function for F in terms of the inputs $a_1, a_2, a_3, b_1, b_2, b_3$, and c.

(b) (6 pts) Implement the logic function $G = \overline{A(B+CD)}$ by using the domino logic. Attempt to reduce the number of transistors and the number of transistors in series (including clocking transistors) in any path from an internal node to power or ground.

Question 2. (6 pts) Figure 2 shows a stick diagram. Describe the function F in terms of the inputs ϕ, A, B, and C.

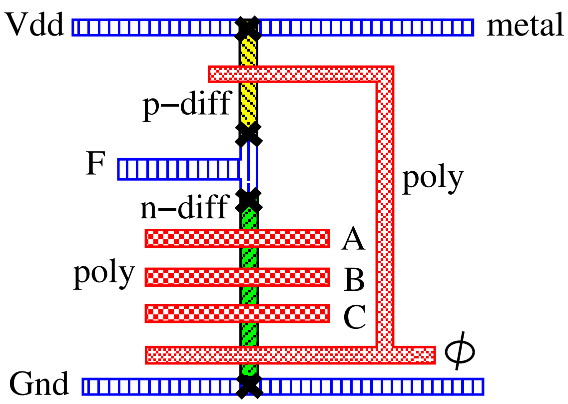


Figure 2: A stick diagram.

Question 3. (10 pts) An n-channel transistor is shown below with a $1\mu m$ polysilicon gate. Other dimensions are given in the figure (in microns). Below show several parameters.

Sheet resistance of polysilicon $= 20\ \Omega/\Box$
n-device area capacitance $C_{ja} = 2 \times 10^{-4} pF/\mu m^2$
n-device peripheral capacitance $C_{jp} = 4 \times 10^{-4} pF/\mu m$

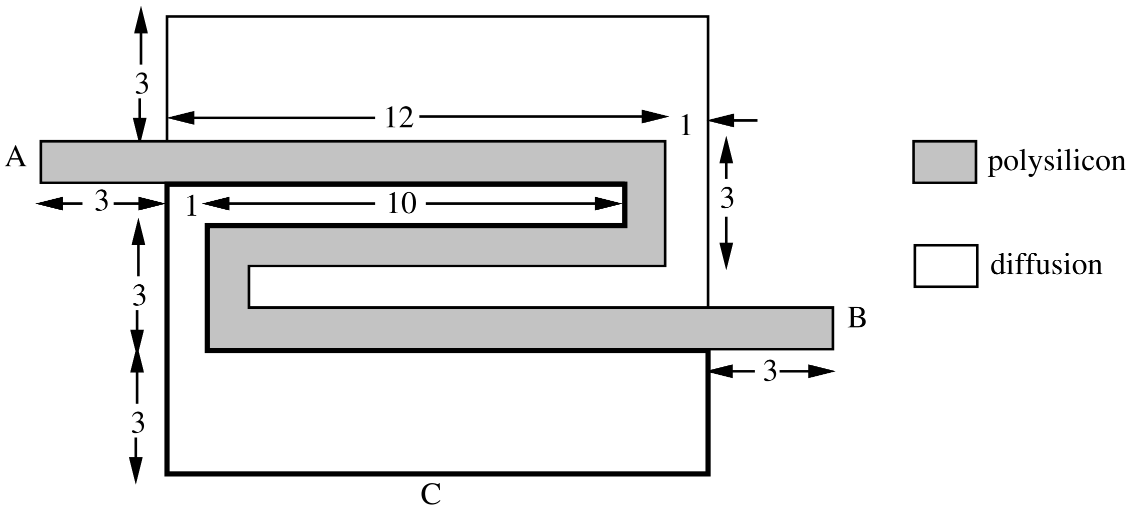


Figure 3: An n-channel transistor cross section.

(a) (5 pts) Determine the resistance of the polysilicon wire from A to B.

(b) (5 pts) Determine the capacitance of the diffusion as seen at node C. (**Hint:** The region seen at C is marked by bold lines. Also you might want to see Page 85 of the class notes.)

Question 4. (6 pts) Consider a 4-bit carry lookahead adder with inputs $A = a_3a_2a_1a_0$, $B = b_3b_2b_1b_0$, c_0 and outputs $S = s_3s_2s_1s_0$ and c_4. Let $g_i = a_ib_i$ and $p_i = a_i \oplus b_i$. Let $A = 1010$ and $c_0 = 0$. If the propagate function $p_2 = 1$ and generate function $g_1 = 1$. Find c_4. (**Hint:** $s_i = a_i \oplus b_i \oplus c_i$ and $c_{i+1} = a_ib_i + b_ic_i + a_ic_i$.)

Question 5. (11 pts) A 2-bit comparator cell which takes inputs $X = x_1x_0$ and $Y = y_1y_0$, and produces a 2-bit result $Z = z_1z_0$ can be specified as follows:
$X > Y, Z = 10$
$X < Y, Z = 01$
$X = Y, Z = 00$ or 11.

(a) (5 pts) Write a VHDL code for the 2-bit comparator, which can be compiled on the Xilinx Foundation Series environment.

(b) (6 pts) If each cell has some fixed delay, show how the cells may be interconnected to compare two 8-bit numbers with three cell delays (use additional cells as necessary).

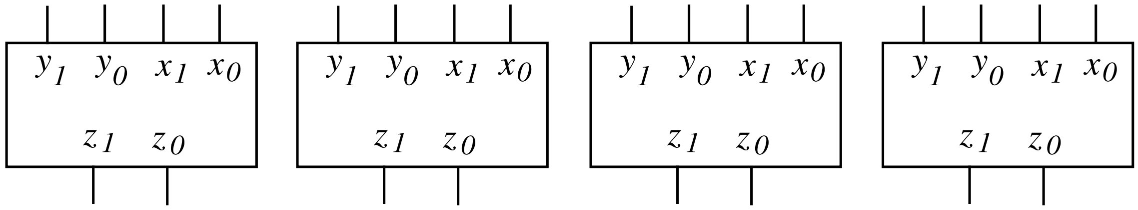


Figure 4: Basic cells.

Question 6. (12 pts) Figure 5 shows two channel routing instances.

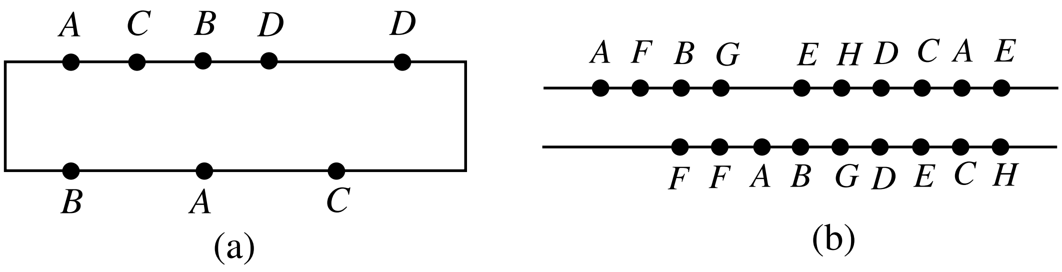


Figure 5: Two channel routing instances.

(a) (6 pts) Assume that coupling capacitance occurs only between adjacent horizontal wires (only that with unit distance is considered) and is proportional to overlap length. For the channel routing instance shown in Figure 5(a), find a routing solution with the minimum number of tracks and the minimum total crosstalk as the 2nd objective.

(b) (6 pts) Apply the dogleg channel router to the routing instance shown in Figure 5(b) to find a solution that uses the least number of tracks. How many tracks are there in your solution?

Question 7. (11 pts) You are to map the Boolean network shown in Figure 6 onto the gate library:

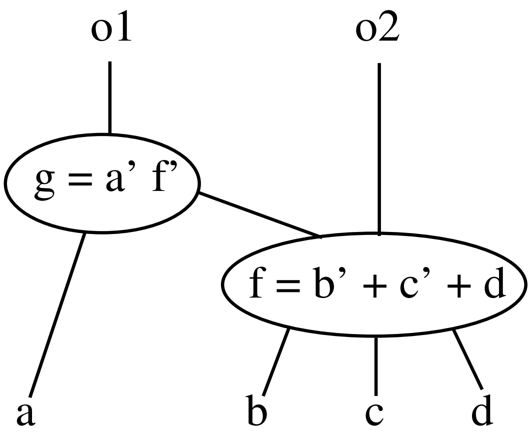


Figure 6: A Boolean network.

inverter (area = 1, power consumption = 1), 2-input NAND (area = 3, power consumption = 2), 2-input NOR (area = 3, power consumption = 3), 3-input NAND (area = 4, power consumption = 5).

(a) (6 pts) Find the mapping of the Boolean network with the minimum area.

(b) (5 pts) Find the mapping of the Boolean network with the minimum power consumption as the 1st objective and the minimum area as the 2nd objective.

Question 8. (10 pts) Consider one fault at a time. Find the test vectors for the faults (a) stuck-at 0 for Test $T1$ and (b) stuck-at 1 for Test $T2$ if testable; explain why the fault(s) is (are) undetectable, otherwise.

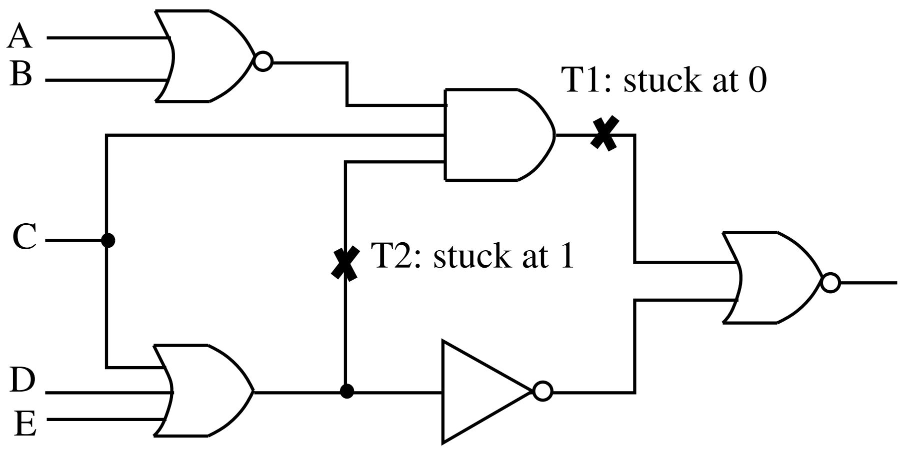
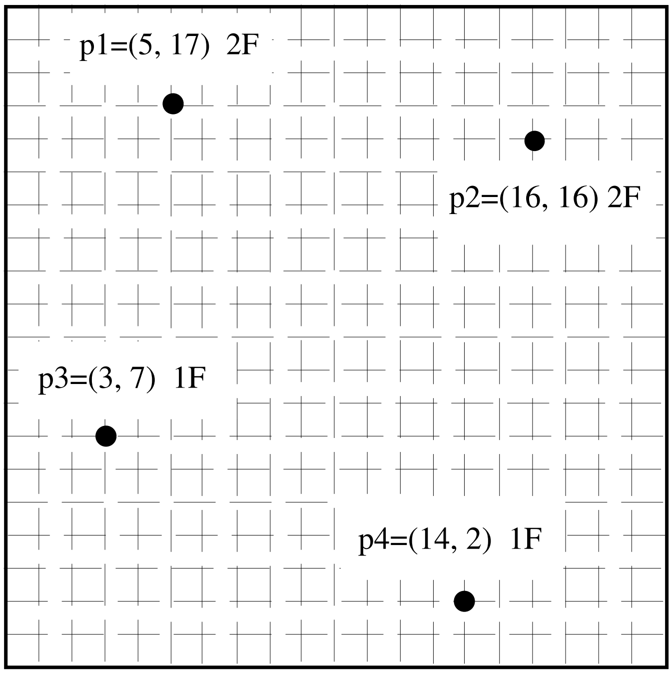
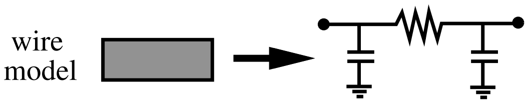


Figure 7: Circuit to be tested.

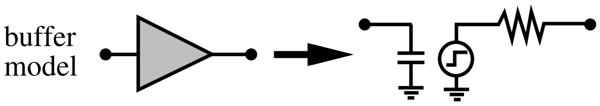
Question 9. (16 pts) Consider the 4-point **gridded-based** instance given in Figure 8(a) (with the coordinate and capacitive loading [in F] of each pin shown).



(a)



(b)



(c)

Figure 8: Clock instance.

(a) (8 pts) Assume that the per unit values of resistance and capacitance are $\alpha = 0.1\Omega$ and capacitance $\beta = 0.2F$, respectively. Find the routing with exact zero skew based on the Elmore delay model discussed in class. Apply the π-model for wires (shown in Figure 8(b)) and the snaking technique if necessary. What is the resulting skew and delay? Show your work.

(b) (8 pts) Assume that you are given two identical buffers with intrinsic resistance $r_b = 0.2\Omega$ and capacitance $c_b = 0.5F$. Apply the switch-resistor model for buffers (shown in Figure 8(c)). Find the coordinates (in your solution to Part (a)) for inserting the two buffers to minimize delay. What is the resulting skew and delay? Show your work.

Question 10. (6 pts) Assume that the circuit shown in Figure 9 has no delays (including wire delays) except components' latencies, but does have a fixed clock overhead of 2 ns for setup & hold times and clock skew when pipelined. Pipeline (i.e., partition) the circuit into three stages (i.e., pipeline depth = 3) to maximize the speedup over the single-cycle, unpipelined design. What is the speedup? What is the total time to execute the pipelined circuit through all stages? Show your pipeline structure.

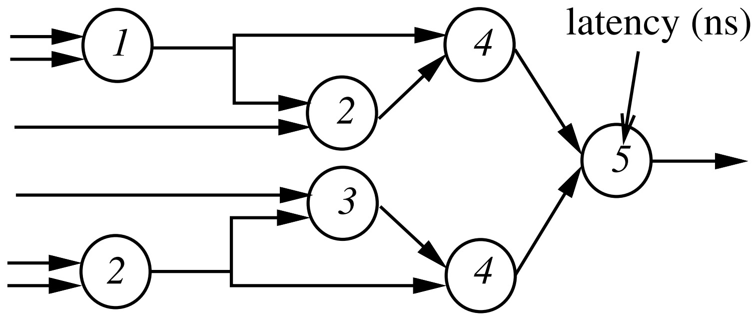


Figure 9: A circuit.