National Chiao Tung University — October 12, 2000
Dept. of Computer & Information Science — Handout #4
Introduction to VLSI Design, Fall 2000 — Yao-Wen Chang

Project #1 (due November 1, 2000)

Project #1 must be done with Xilinx Foundation Series M3.1i by choosing "XC4010XL-TQ176" as your target device. The software is available in EC 224. Please also download from the course web site a short note on how to use the software.

Projects: You might find Hennessy and Patterson's books useful for this project.

(1) Design a 16-bit ripple carry adder and a 16-bit carry lookahead adder using the schematic editor.

(2) Design a 32-bit ripple carry adder and a 32-bit carry lookahead adder using the VHDL/Verilog hardware description language.

(3) For each part, answer the following questions:

- (a) What is the longest net delay?
- (b) What is the number of CLBs for each design?
- (c) What is the utilization of 4 input LUTs and 3 input LUTs?
- (d) What is the score for each design?

(4) Extra questions on Xilinx Foundation Series M3.1i:

- (a) Which report file will list various Placer Scores the compiler attempted ?
- (b) Which report will show the utilization of CLBs located?
- (c) Which report file will show the longest net delay?
- (d) Which report file will list all the pin assignments used by the compiler?
- (e) Which report file lists the Design Rule Checker (DRC) messages?
- (f) Which report file will show if the design files were merged correctly?
- (g) Which report file lists the CLBs whose placement was Guided?

Submit the following:

- Submit every subcell and top cell, simulation results (waveform diagrams), Place&Route reports, VHDL/Verilog codes, and documentation.
- A floppy disk with all aforementioned files, and create a directory, "h1", to place all files in it. Please label your name and student ID on the floppy disk. **(Note that the TA will use the submitted files for demo, and no additional files are allowed to be added during demo.)**
- Answers to questions in Parts (3) and (4).
- **Attention: You are allowed to use only basic gates in the library. They are NAND, NOR, AND, OR, NOT, XOR, XNOR, MUX, and BUFFER gates.**
- **There will be a demo session in the afternoon of November 1.** The schedule is to be announced.

Reference Books:

- J. L. Hennessy and D. A. Patterson, *Computer Architecture: A Quantitative Approach*, Second Edition, Morgan Kaufmann Publishers, 1996.
- J. L. Hennessy and D. A. Patterson, *Computer Organization and Design: The Hardware/Software Interface*, Morgan Kaufmann Publishers 1994.