National Chiao Tung University
Dept. of Computer & Information Science
Introduction to VLSI Design, Fall 2000

December 12, 2000
Handout #15
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Project #3 (due December 29)

In this project, you are asked to design an ALU of a 16-bit RISC microprocessor using Verilog or VHDL on the Xilinx Foundation Series M3.1i System with the device XC4010XL-PC84. In addition to the text and references, you may also want to look at the following references:

- D. D. Gajski, *Principles of Digital Design*, Prentice-Hall Inc., 1997. ISBN: 0-13-242397-9.
- R. H. Katz, *Contemporary Logic Design*, The Benjamin/Cummings Pub. Com., 1994. ISBN: 0-8053-2703-7.
- M. M. Mano and C. R. Kime, *Logic and Computer Design Fundamentals*, Prentice-Hall, Inc., 1997. ISBN: 0-13-206780-3.
- C. H. Roth, Jr, *Fundamentals of Logic Design*, 4th Ed., PWS Publishing Com., 1995. ISBN: 053495472-3 (0-314-92218-0).
- J. F. Wakerley, *Digital Design Principles and Practices*, Prentice-Hall Inc., 1990. ISBN: 0-13-212879-9.

For this project, you MUST follow the specification given below.

Develop a hierarchical design by first identifying the modules which will implement the specification.

```
I/O: Bit 15 is the most significant bit.
INPUTS: A[15..0], B[15..0], ALU_Code[4..0]
OUTPUTS: C[15..0], overflow
```

The following describes the bit patterns for the ALU control signals.

- The ALU control signals (ALU_Code) consist of 5 bits and define a total of 17 instructions.
- There are two fields in these five signals: *operation-type field* and *operation field.*
- The two high order bits denote the operation type while the lower three bits represent the operations.
- The bit patterns for the operation type field are as follows:

  ```
  arithmetic operation:  00
  logic operation:  01
  shift operation:  10
  set condition operation:  11
  ```

- The bit patterns for the operation field are as follows:
  - `arithmetic operation:  00xxx`

    ```
    add:   000  signed addition (C ← A + B)
    addu:  001  unsigned addition (C ← A + B)
    sub:   010  signed subtraction (C ← A - B)
    subu:  011  unsigned subtraction (C ← A - B)
    ```

```
– logic operation:  01xxx
    and:     000  A AND B
    or:      001  A OR B
    nand:    010  A NAND B
    nor:     011  A NOR B
    xor:     100  A XOR B
    equal:   101  A EQUAL B
– shift operation:  10xxx
    lihi:  000  load high immediate (load upper half of register with immediate)
                E.g., if A = <0101010100110011> and B = <1010101011110000>,
                then C = <1010101000000000>.
    lilo:  001  load low immediate (load lower half of register with immediate)
    sll:   010  logic left shift A by the amount of B
    srl:   011  logic right shift A by the amount of B
– set condition operation:  11xx
    slt:  000  if A (signed) < B (signed) then C = <0...01> else C = <0...00>
    sgt:  001  if A (signed) > B (signed) then C = <0...01> else C = <0...00>
    sle:  010  if A (signed) <= B (signed) then C = <0...01> else C = <0...00>
    sge:  011  if A (signed) >= B (signed) then C = <0...01> else C = <0...00>
    seq:  100  if A (signed) = B (signed) then C = <0...01> else C = <0...00>
    sne:  101  if A (signed) != B (signed) then C = <0...01> else C = <0...00>
```

- If there is an overflow in the ALU operations, the signal **"overflow"** should be set to "1", otherwise it is "0".
- Determine the longest signal paths by checking the place&route report.

You might need to design a smaller decoder to decode "ALU_Code". (This is a standard logic design problem.)

Submit a disk that contains the following:

- Submit your Verilog/VHDL codes for all cells, simulation results (waveform diagrams), Place&Route reports, and documentation. (**Attention: Do virus checking before submission. Those disks with virus(es) will receive no grades.**)
- For this project, you are free to use any code/gate in the library.
- **There will be a demo session starting at 4:40pm, December 29.**

Grades will be based on

- correctness of the design (determined by your and TA's simulation results).
- performance (delay of the worst-case path(s)).
- efficiency of design (LUT count or CLB count).
- **Remember the rule: Those who copy others' designs will receive an F grade for this semester.**