A REUSABLE METHODOLOGY FOR NON-SLICING FLOORPLANNING

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ABSTRACT

Floorplanning is an important step in an early phase of VLSI design. For faster design convergence, there is an urgent need to start floorplanning as early as possible, even when not all modules are designed. Therefore, it is desirable to consider floorplanning with uncertainty to obtain a compact and reliable floorplan when the dimensions and interconnections of modules are not fully determined. In this paper, we propose a sequence-pair based floorplanner, named PLP, for uncertain designs. PLP with uncertain data can consider non-slicing floorplans, and then generate reliable and compact floorplans. Experimental results indicate that its performance is equivalent to the conventional sequence-pair floorplanner, however, PLP attains significant higher reliability. With 30%–70% uncertainty, our algorithm achieves at least 80% confidence that the area derivation is within only 1%.

1. INTRODUCTION

Floorplanning is one of the most important steps in an early phase of VLSI design. Some critical physical parameters, such as area, delay, and power, can be approximated after this stage. For faster design convergence, there is an urgent need to obtain a floorplan as early as possible. As mentioned in [1], by generating a floorplan early in the design process, i.e., when some modules have not been completely designed yet, the total design time can be decreased since some time-consuming processes can only be performed after a floorplan is obtained. Therefore, it is desirable to consider the problem of floorplanning with uncertainty to obtain a compact and reliable floorplan even when the dimensions and interconnections of modules are not fully determined.

In practice, some components must be designed from scratch, whereas some others are modifications of components from previous designs, and thus designers can specify some estimations about the final area of each incompletely designed module and its corresponding probability. The conventional floorplanning algorithms take a list of module information for which each module has a deterministic dimension. Therefore, these algorithms cannot handle the problem that some modules have multiple possible dimensions, represented by width and height probability distribution functions (PDF's). Intuitively, the reasonable approach is to use the expected values of the width distribution and height distribution as width and height respectively. However, we will show later that the expected value method cannot generate a reliable floorplan. Nostradamus [1] is the first floorplanner that can cope with uncertain dimensions of modules, and is effective to obtain a compact floorplan. However, it is based on the slicing structure [2] which does not correspond to most real designs. Further, it does not consider interconnection cost which is a crucial metric for contemporary interconnect-driven VLSI design methodology.

In this paper, we propose a sequence-pair [3] based floorplanner for uncertain designs. Our floorplanner for uncertain data can consider non-slicing floorplans [3, 4, 5, 6, 7], and can generate a reliable and compact floorplan. To cope with the uncertainty, we derive a probability-based longest path (PLP) algorithm for a constraint graph to evaluate the enclosing width and height distributions. After applying the PLP algorithm, we can obtain possible placements and interconnection costs. Our floorplanner with the estimated uncertain data can effectively generate a compact and *reliable*[1] floorplan. By a reliable floorplan, we mean one whose area at the time it is generated does not differ significantly from its area when all modules are designed completely. Experimental results indicate that the resulting average area is similar to the one obtained by a sequence-pair floorplanner, but PLP attains significant higher reliability than the sequence-pair floorplanner. With 30%–70% uncertainty, we have at least 80% confidence that the area derivation is within only 1%.

2. PROBLEM FORMULATION

In this paper, we follow the formulation presented by [1]. Let $M = \{m_1, m_2, ..., m_n\}$ be a set of n rectangular modules. Each module $m_i \in M$ is associated with a two tuple $(\mathcal{W}_i, \mathcal{H}_i)$ which denotes a pair of height and width distribution. Each distribution list contains pairs of potential heights (or widths) of a module and their probabilities.

We have

$$\begin{aligned} \mathcal{W}_i &= \{(w_{ij}, p_{w_{ij}}) | 1 \leq j \leq r_i\}, \\ \mathcal{H}_i &= \{(h_{ij}, p_{h_{ij}}) | 1 \leq j \leq s_i\}. \end{aligned} \quad (1)$$

The objective of floorplanning with uncertain designs is to minimize the expected value of area $\mathcal{A}_{tot}$ induced

[1] A formal definition of a reliable floorplan is given in Section 3.2.

by the assignment of the topology of m_i's, where $\mathcal{A}_{tot}$ is a probability distribution measured by possible enclosing rectangles of placement.

3. FLOORPLANNING WITH UNCERTAIN DESIGNS

To cope with uncertainty, we propose a *probability-based longest path* (*PLP*) algorithm to evaluate the enclosing width and height distributions.

3.1. Probability-based Longest Path (PLP) Algorithm

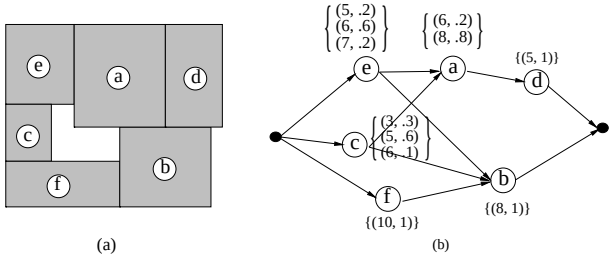

Fig. 1. (a) A placement (b) The probability-based constraint graph.

For uncertain designs, since a module may have many possible dimensions, the weight of the corresponding node in a horizontal (vertical) constraint graph gives the width (height) distribution of the module. Figure 1(b) shows the probability-based horizontal constraint graph for the placement of Figure 1(a). An edge $n_i \rightarrow n_j$ in a horizontal (vertical) constraint graph denotes that module m_i is on the left (bottom) side of module m_j. Since the weight of a node is a distribution, there could be many possible longest paths. Our goal is to obtain the enclosing width (height) distribution of a floorplan which is corresponding to the length distribution of longest paths of horizontal (vertical) constraint graph.

Thus, we propose the probability-based longest path (PLP) algorithm to estimate the length distribution of longest paths. Without loss of generality, we use the notation for horizontal constraint graphs, and the treatment of the vertical part is similar. Traditional longest path algorithms assume deterministic width of each node. Therefore, it is easy to calculate right and left boundary positions. When the width of modules are probability distributions, we need to define two distribution operators to manipulate boundary position distributions. The *distribution merge operation* is used to find the left boundary distribution, $\mathcal{L}_i$, while the *distribution addition operation* is used to find the right boundary distribution, $\mathcal{R}_i$. We detail the two operations in the following subsections.

3.1.1. Distribution Merge Operation

In traditional constraint graphs, the left boundary of a node n_i is determined by the largest right boundary of the incoming nodes of n_i. For an example in Figure 1(a), node a has incoming node e and c. The left boundary of node a is the right boundary of node e since node e dominates node c.

For probabilistic constraint graphs, we define the distribution merge operation that manipulates the set of all right boundary distributions of incoming nodes of n_i to derive the left boundary distribution. The probability that the longest path will pass through node e to node a is denoted as $P_{e\rightarrow a}(x)$. In other words, $P_{e\rightarrow a}(x)$ is the probability of the right boundary, x, of node e is larger than node c. Therefore,

$$P_{e\rightarrow a}(x) = P(\mathcal{R}_e = x)P(\mathcal{R}_c \leq x). \tag{2}$$

The probability that the left boundary of node a is x is the summation of $P_{e\rightarrow a}(x)$ and $P_{c\rightarrow a}(x)$. The formal definition of the probability that the longest path will pass through n_i to n_k is defined as follows:

$$P_{n_i\rightarrow n_k}(x) \quad = \quad P(\mathcal{R}_i = x) \prod_{n_j \in I_{n_k}} P(\mathcal{R}_j \leq x). \tag{3}$$

where I_{n_k} denotes the set of all n_k's incoming nodes.

To represent the left boundary distribution of n_k, $\mathcal{L}_k$, we should merge all possible longest path through n_i to n_k for each $n_i \in I_{n_k}$ into a single random variable $\mathcal{L}_k$ as follows:

$$P(\mathcal{L}_k = x) = \sum_{n_i \in I_{n_k}} P_{n_i\rightarrow n_k}(x). \tag{4}$$

Let $\odot$ denote the merge operation of a set of distributions.

$$\mathcal{L}_k = \odot(\mathcal{R}_i, \ldots, \mathcal{R}_j), \tag{5}$$

where $\mathcal{R}_i, \ldots, \mathcal{R}_j$ denote the set of right boundary distributions for all n_k's incoming nodes.

3.1.2. Distribution Addition Operation

The distribution addition operation was first presented in [1], which is defined as follows:

$$\begin{aligned} \mathcal{D}_1 \oplus \mathcal{D}_2 \quad &= \quad \{(d_{1i} + d_{2j}, p(d_{1i})p(d_{2j}))| \\ (d_{1i}, p(d_{1i})) \quad &\in \quad \mathcal{D}_1, (d_{2j}, p(d_{2j})) \in \mathcal{D}_2\}. \end{aligned} \tag{6}$$

The distribution list of $\mathcal{D}_1 \oplus \mathcal{D}_2$ consists of elements which are pairwise "addition" of the elements from the two distribution list $\mathcal{D}_1$ and $\mathcal{D}_2$. Thus, it is intuitive that $\mathcal{R}_i$ is derived by distribution addition operation on left boundary distribution and width distribution of node n_i

$$\mathcal{R}_i = \mathcal{L}_i \oplus \mathcal{W}_i, \tag{7}$$

where $\mathcal{W}_i$ denotes the width distribution of node n_i.

3.1.3. The Algorithm

To evaluate the distribution of the longest path length, given a weighted, directed acyclic graph $G = (V, E)$ with source S, target T, and the weight function $w : V \rightarrow \mathcal{W}$ (where $\mathcal{W}$ denotes the width random variable), the PLP algorithm returns the length distribution of longest paths. The algorithm traverses each node in increasing topological order. For each node n_k, we apply the distribution merge and addition operations to obtain $\mathcal{L}_k$ and $\mathcal{R}_k$. Consequently, since target T is the last node of graph G, $\mathcal{L}_T$ represents the length distribution of longest paths of graph G.

Algorithm: Prob_Longest_Path(G)
Input: G—acyclic directed graph
Output: $\mathcal{D}$—random variable
\\ S is the source node of G
\\ T is the target node of G
\\ In_k is a set of incoming nodes of n_k
1 G = Top_Sort(G);
2 G = Reduce_Transitivity(G);
3 **foreach** node n_k in G with ascending topology order
4 **if** ($S \not\rightarrow n_k$)
$n_i, \ldots, n_j \in In_k$
5 $\mathcal{L}_k = \odot(\mathcal{R}_i, \ldots, \mathcal{R}_j)$;
6 **if** ($T = n_k$)
7 $\mathcal{D} = \mathcal{L}_k$;
8 return $\mathcal{D}$;
9 **else**
10 $\mathcal{R}_k = \mathcal{L}_k \oplus \mathcal{W}_k$;

Fig. 2. The PLP algorithm.

3.2. Reliable Floorplan

In this section, we define a reliability index for both the area and the wirelength. A reliable floorplan should have small a variance of the area and the wirelength. However, the significance of the variance depends on its corresponding mean. We use *Chebyshev's inequality* to facilitate the definition.

The *reliability index* r of a floorplan is defined as we have r confidence that the area or wirelength deviation of the floorplan is within $d = 1\%$ of the area or the wirelength. If X is a random variable with finite sample mean μ and sample variance σ^2, then for any value $d > 0$,

$$P\{|\mathcal{X} - \mu| \geq d\mu\} \leq \frac{\sigma^2}{d^2\mu^2} = 1 - r$$

$$P\left\{\left|\frac{\mathcal{X}}{\mu} - 1\right| < d\right\} > 1 - \frac{\sigma^2}{d^2\mu^2} = r.$$

Then, we have

$$r = 1 - \frac{\sigma^2}{d^2\mu^2}. \quad (8)$$

3.3. The Overall Algorithm

We developed a simulated annealing based algorithm [8] using the sequence pair representation for non-slicing floorplan design with uncertain data. Given an initial solution represented by a sequence pair, the algorithm perturbs the sequence pair to a new one. Then, the algorithm applies the PLP algorithm to evaluate the final enclosing width distribution, $\mathcal{W}$, and the final enclosing height distribution, $\mathcal{H}$. The cost function during the annealing process can be $E[\mathcal{W}]E[\mathcal{H}]$. Since obtaining a reliable floorplan is critical, we add reliability index for the area to the cost function and try to minimize its expected value and variance simultaneously. The *variance* of the area is defined respectively as:

$$\triangle Area_{\mathcal{W},\mathcal{H}} = \sigma_{\mathcal{W}}\sigma_{\mathcal{H}} + \mu_{\mathcal{H}}\sigma_{\mathcal{W}} - \mu_{\mathcal{W}}\sigma_{\mathcal{H}}, \quad (9)$$

where σ and μ denote the standard derivation and the mean of a distribution respectively. The corresponding reliability index is denoted as I_a which is defined as:

$$I_a = 1 - \left(\frac{\triangle Area_{\mathcal{W},\mathcal{H}}}{d\mu_{\mathcal{H}}\mu_{\mathcal{W}}}\right)^2, \quad (10)$$

Then, we use the following cost function for simulated annealing:

$$cost = \beta\frac{E[\mathcal{W}]E[\mathcal{H}]}{Area_{norm}} + (1 - \beta)(1 - I_a), \quad (11)$$

where β is to control the tradeoff between the expected value and the variance of the area.

4. EXPERIMENTAL RESULTS

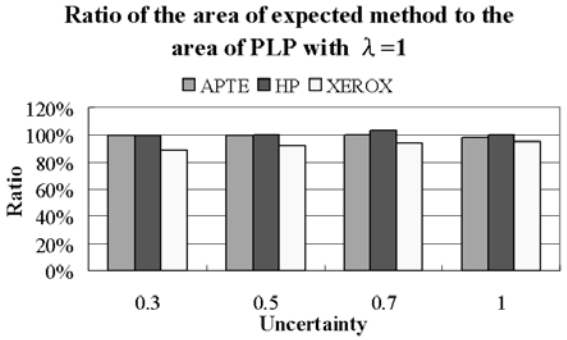

Fig. 3. Ratio of area of the expected value method to the area of PLP method on different uncertainty levels from 0.3 to 1.

In the following, we show the experimental results of the MCNC benchmark. It includes apte, xerox, and hp circuits, and all of them contain interconnect information. However, the modules of MCNC benchmark are deterministic, we need to randomize the dimension of each module.

We compare our results with the expected value method which fills the width (height) of a module by its expected

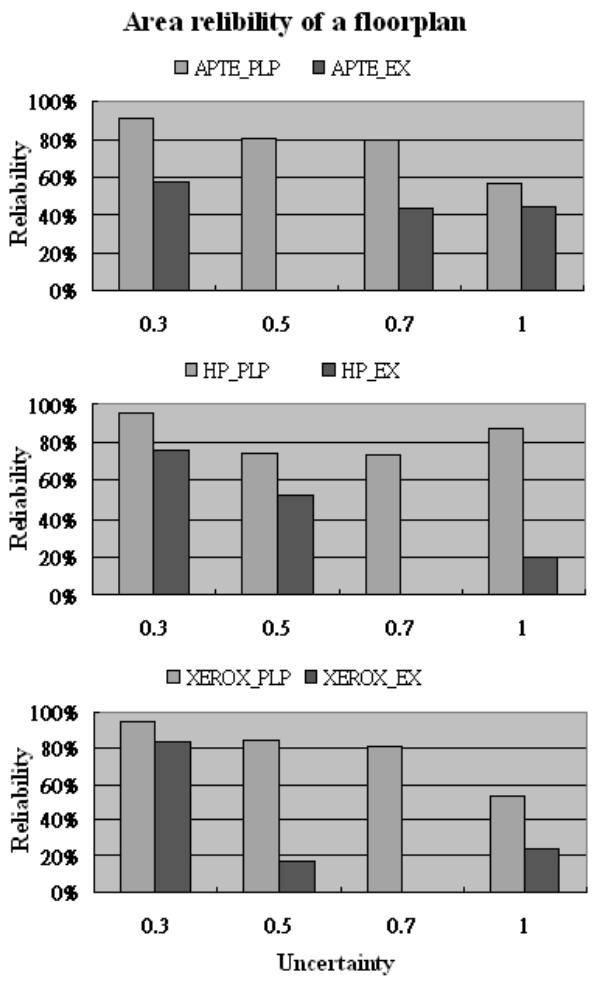

Fig. 4. Comparison of area reliability between the PLP method and the expected value method on different uncertainty levels from 0.3 to 1.

value. To evaluate how well PLP might work in practice, we perform Monte Carlo simulations to draw the true dimensions for each module according to its width and height distributions. By repeating a number of simulations, the statistics of sample area is obtained. In the following, we compare the statistics resulting from the PLP algorithm and the expected value method.

An important parameter in input data is the *uncertainty level*. We say an input data set is $x\%$ uncertain, if $x\%$ of its modules have probabilistic dimensions and others have deterministic dimensions, i.e., the rest have exactly one width and one height value. To demonstrate the performance of PLP to cope with uncertainty effectively, we compare the results with different percentage of modules that have probabilistic dimensions.

Figure 3 shows the ratio of average area obtained by the expected value method to average area obtained by PLP on different uncertainty levels. The result indicates that PLP has similar average area performance with the expected value method. Figure 4 show the area reliability of PLP versus the expected value method on different uncertainty levels ranging from 30% to 100%, where the reliability index denotes the confidence deviations within 1%. For uncertainty levels ranging from 30% to 70%, PLP attains 80% area reliability among most of cases. PLP has the significantly higher area reliability than the expected value method.

5. CONCLUDING REMARK

We proposed a non-slicing floorplanner, called PLP, that can deal with uncertain dimensions of modules. Experimental results show that the PLP have powerful ability to hide the uncertainty and can generate quiet reliable and compact floorplans. The capability of the PLP shows its promise in generating a floorplan in early design process. We propose to explore floorplanning problems for uncertain designs, such as rectilinear and buffer-block planning for interconnect-driven floorplanning in the future.

6. REFERENCES

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