Recent Research and Emerging Challenges in Physical Design for Manufacturability/Reliability *

Chung-Wei Lin[1], Ming-Chao Tsai[2], Kuang-Yao Lee[2], Tai-Chen Chen[1], Ting-Chi Wang[2], and Yao-Wen Chang[1,3]

[1]Graduate Institute of Electronics Engineering, National Taiwan University, Taipei 106, Taiwan

[2]Department of Computer Science, National Tsing Hua University, Hsinchu 300, Taiwan

[3]Department of Electrical Engineering, National Taiwan University, Taipei 106, Taiwan

{enorm,tcchen}@eda.ee.ntu.edu.tw, {d938316, d924347}@oz.nthu.edu.tw, tcwang@cs.nthu.edu.tw, and ywchang@cc.ee.ntu.edu.tw

ABSTRACT

As IC process geometries scale down to the nanometer territory, the industry faces severe challenges of manufacturing limitations. To guarantee yield and reliability, physical design for manufacturability and reliability has played a pivotal role in resolution and thus yield enhancement for the imperfect manufacturing process. In this paper, we introduce major challenges arising from nanometer process technology, survey key existing techniques for handling the challenges, and provide some future research directions in physical design for manufacturability and reliability.

I. INTRODUCTION

As IC process geometries scale down to 90nm and below, the industry faces severe challenges of manufacturing limitations, induced mainly from the lithographic limitation. Because the industry still uses 193nm lithography to print sub-90nm feature size, there are many unwanted effects resulting in large distortions for the shapes on a wafer as shown in Figure 1(a). Consequently, yield and reliability become first-order cost metrics under the imperfect lithographic process.

To improve yield and reliability, resolution enhancement techniques (RETs) [39] are necessary. These techniques include optical proximity correction (OPC), sub-resolution assist feature (SRAF, also called scattering bar), phase-shifting mask (PSM), off-axis illumination (OAI), etc. They can effectively achieve better lithographic printability, but their costs are usually high [30]. For example, OPC may generate a great number of polygons on a mask, while PSM need to use phase shifters at the mask level, both resulting in very high mask costs. Another urgent issue of RETs is that it may be too late to perform RETs after the physical design stage. For example, if there is no enough space among wires after the physical design stage, OPC will probably fail. Therefore, *physical design for manufacturability* is crucial to ensure the success of manufacturing.

Another approach to improve yield and reliability under the imperfect manufacturing process is *physical design for reliability*. For example, wire spreading and widening can reduce the probability of shorts and opens, respectively. Besides, in order to reduce the via failure caused by lithographic distortion, double-via insertion and line-end extension are recommended. Line-end extension is to extend the line ends of metals for a via and can alleviate the via-cut misalignment problem caused by line-end shorting. On the other hand, if one via fails, double-via insertion provides a redundant via which can serve as a fault-tolerant substitute for the failing one. However, if the amount of inserted redundant vias is not well controlled, it may adversely worsen the yield and reliability of the design because the pattern distortion of the vias might become serious. Therefore, via-density check is also suggested to be considered during double-via insertion.

*This work was partially supported by National Science Council of Taiwan under Grant No's NSC 95-2221-E-002-372, NSC 95-2221-E-002-374, NSC 95-2752-E-002-008-PAE, NSC 95-2220-E-007-037, and Ministry of Economic Affairs of Taiwan under Grant No. MOEA 95-EC-17-A-01-S1-031.

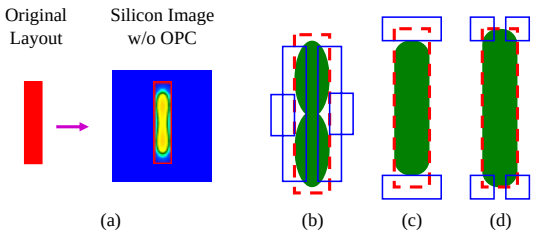

Fig. 1. (a) Optical proximity effects. Three major OPC techniques: (b) Line Biasing, (c) Hammerhead, and (d) Serif.

The remainder of this paper is organized as follows. Section II (Section III) explains the effects and introduces the existing techniques of physical design for manufacturability (reliability). Section IV provides some future research directions in physical design for manufacturability and reliability. Finally, conclusions are made in Section V.

II. PHYSICAL DESIGN FOR MANUFACTURABILITY

To achieve the success of manufacturing, it has been pointed out that layout restrictions are inevitable [24], and additional restricted design rules have been suggested [12, 13, 19, 22, 33], especially for a router [22]. As a relatively new issue, most related works in the literature focus on OPC and PSM, with some other works considering different effects.

A. OPC

OPC is probably the most popular RET. It can deal with some types of image-shape distortions such as line shortening, corner rounding, and line-width variations by adding or subtracting some features as serifs or line segments as shown in Figures 1(b)–(d). However, OPC may generate a great number of polygons with a very high mask cost, and it might fail if there is no enough space among wires after the physical design stage. Therefore, a few existing works targeted on the assurance of OPC success and the reduction of OPC pattern features.

Huang and Wong [17] presented a pioneering work on OPC-friendly maze routing based on the Lagrangian relaxation formulation. The router

is grid-based and considers only two-pin connections. Furthermore, it uses the flat framework and thus handles only hundreds of connections.

Wu et al. [41] formulated two OPC-aware maze routing problems and solved them by modifying the well-known Lee algorithm. In this work, simple OPC costs of routing grid cells are calculated by the estimated light intensity generated by each routed net.

Chen and Chang [5] presented the first multilevel, full-chip gridless detailed router considering the OPC effects. The router integrates global routing, detailed routing, and congestion estimation together at each level of the multilevel routing. It can handle non-uniform wire widths and consider routability and OPC simultaneously. For each line, its OPC cost is defined as the total number of pattern features and applied a modified Dijkstra's shortest path algorithm to optimize the routing and OPC costs simultaneously. Experimental results show that this work not only efficiently obtains significantly better routing solutions with 100% routing completion, but also archives an effective reduction of OPC pattern features.

Mitra et al. [28] developed an RET-aware detailed router to handle full-chip capacity to enhance the overall printability. After the initial routing result, a fast lithography simulation is applied to introduce the lithography hotspot map (LHM). According to the LHM, the router generates routing blockages for the stage of ripup and reroute. After wire spreading, ripup, and reroute, the number of edge placement error (EPE) hotspots is reduced by 40%.

Some OPC related research results also focus on standard-cell characterization and fast simulation. They are highlighted below. Cao et al. [4] suggested using dummy poly insertion to shield inter-cell optical interference. This technique effectively reduces timing variation induced by the deviation of gate dimensions. Since the dummy polys are carefully inserted, it will not create any new transistor on the silicon. Thus, this method incurs no overhead on LVS (layout versus schematic) verification. In this work, they first simulated the images of the modified standard cells. Then they characterized the timing and leakage properties of each cell. Experimental results show that the average timing variation and power leakage variation of these shielded cells are reduced by 11.4% and 8.0% respectively. However, the dummy polys may potentially induce parasitic capacitance and reduce the performance of the transistors.

Pawlowski et al. [31] proposed a cellwise approach to tackle the complicated and time-consuming OPC task. When adjusting the feature geometry of a cell, this method stresses the influence of boundaries of abutted cells in a row. The experimental results show that, compared with a commercial tool, this method has up to 100X speedup and 35X reduction in mask data size.

B. PSM

In addition to OPC, PSM is another popular technique to improve the image quality. It can be categorized into two types: attenuated PSM (AttPSM) and alternative PSM (AltPSM). AttPSM allows small amount (6–10%) of light transmission and forces the phase of the penetrated light changed by 180 degrees in the opaque region of a mask. AltPSM aggressively improves the aerial image which is mainly used in the poly layer and critical metal layers, such as the first metal layer. There are two types of AltPSM: *bright-field* and *dark-field AltPSM*. The design shapes of the bright-field AltPSM are opaque regions of a mask, and it is usually used for the poly layer. The design shapes of the dark-field AltPSM are bright regions of a mask, and it is usually used for metal layers. Although AltPSM can further reduce the *critical dimension* (*CD*), it results in a very strong proximity effect. If some feature patterns are closer than a certain threshold, therefore, they must be assigned to opposite phases. Consequently, it may generate phase-conflict problems. As an example shown in Figure 2, for the horizontal and the vertical segments, the lower right side of the T-junction must be assigned to respective 0- and 180-degree phases for the horizontal and the vertical segments, causing a phase conflict at the corner. Therefore, how to assign phases or modify layouts with no phase conflicts is a main challenge of PSM.

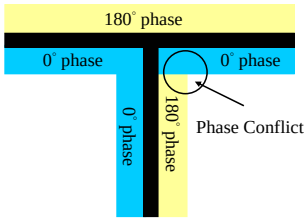

Fig. 2. For the horizontal and the vertical segments, the lower right side of the T-junction must be assigned to respective 0- and 180-degree phases for the horizontal and the vertical segments, causing a phase conflict at the corner.

The problem on AltPSM has been studied to some degree. Berman et al. [2] presented a layout modification and phase-assignment algorithm for dark-field altPSM. The algorithm first constructs a conflict graph according to the dependency of the phase assignment. Then it deletes a set of edges with the minimum total weight to make the graph bipartite, where the weight is an estimated cost measuring the difficulty for layout modification.

Chiang et al. [8] presented a new computationally efficient algorithm to solve the phase-conflict problem for the bright-field PSM. In this work, the phase-conflict problem is formulated as a minimum weighted conflict-cycle removal problem. Although this problem can be solved optimally in polynomial time, this approach incurs some area overhead.

Cao et al. [3] divided the phase-conflict problems into intra-cell compliance and inter-cell composability problems from the viewpoint of cell-library design. In this work, both the problems are formulated as Boolean satisfiability (SAT) problems solved by a SAT solver. The method considers only the problems for cells. However, the inter-cell connections occupying the first metal layer, which may also induce phase conflict, are not considered.

McCullen [27] proposed a phase-correct routing algorithm for the dark-field PSM . During the routing stage, the author solved some phase conflicts by widening the distance between two line ends, or moving the wiring jog to a separate wiring layer which runs orthogonally to the primary wiring direction of the non-jogged portions of the wire.

C. Other Considerations

The use of SRAFs provides a means of recovering the process window for pitches that are not enhanced by OAI. SRAFs are additional long and thin rectangular shapes placed on masks along the length or the extent of main shapes as shown in Figure 3(a). Several existing techniques perform the SRAF placement by a rule-based, a model-based, or a hybrid approaches, but not much work focuses on the two-dimensional optimization. To prevent possible conflicts in a two-dimensional SRAF placement, as shown in Figure 3(b), Mukherjee et al. [29] used the Voronoi diagram as shown in Figure 3(c), and Barnes et al. [1] performed a model-based conflict resolution. On the other hand, Gupta et al. [14] proposed a technique for assist-feature correctness in detailed placement of standard-cell designs, which avoids forbidden pitches and the manufacturing uncertainty, and thus achieves assist-feature compatibility in physical layouts.

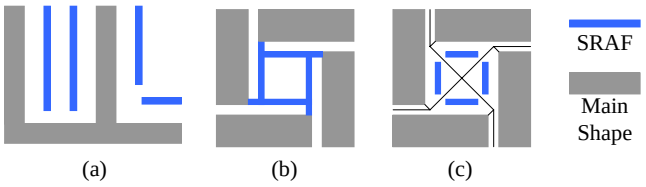

Fig. 3. (a) SRAFs are additional long and thin rectangular shapes placed on masks along the length or the extent of main shapes. (b) Two-dimensional SRAF placement conflicts. (c) The Voronoi diagram to solve the two-dimensional SRAF placement conflicts [29].

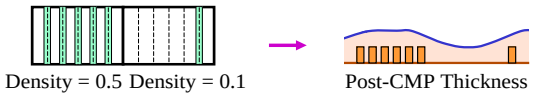

Fig. 4. Large density variations among neighboring subregions lead to post-CMP thickness irregularities.

Besides, Deng et al. [11] presented a method to improve the printability of layout images under OAI by appropriately inserting dummy wire segments in the free space. Although this technique improves the image quality, the dummies introduce undesirable coupling capacitance. This paper tries to trade off the lithography cost and coupling capacitance.

In the modern copper metallization process, another yield loss comes from the chemical-mechanical polishing (CMP) planarization step. The earlier studies for CMP processes have indicated that the post-CMP dielectric thickness is highly correlated to the *variation* of the layout pattern density [37]; larger density variations among neighboring subregions lead to more significant post-CMP thickness irregularities, as shown in Figure 4. Li et al. [23] presented the first full-chip routing system addressing the CMP induced variation. By setting the desired density in the cost function of global routing, the routing results have more balanced interconnect distribution. Cho et al. [9] proposed a pioneering work to consider CMP variation during *global* routing. They empirically developed a predicted CMP density model and showed that the number of inserted dummy features can be predicted by the wire density. Then, they proposed a minimum pin-density global-routing algorithm to reduce the maximum wire density.

III. Physical Design for Reliability

Physical design for reliability has also become more important than ever in the nanometer technology. Here, we focus on the discussions of two popular issues in physical design for reliability: double-via insertion for yield enhancement and the diode/jumper insertion for antenna avoidance.

A. Double-Via Insertion

If a via fails, double-via insertion provides a redundant via which can serve as a fault-tolerant substitute for the failing one. Figure 5 shows an example via doubling from the work [6], where different colors represent wires of different layers, and a yellow square represents a redundant via. In Figure 5, every via is accompanied by a redundant via to make the connection between different layers more reliable.

Xu et al. [42] proposed the first work to consider double-via insertion during maze routing. By assigning double-via costs to the routing graph,

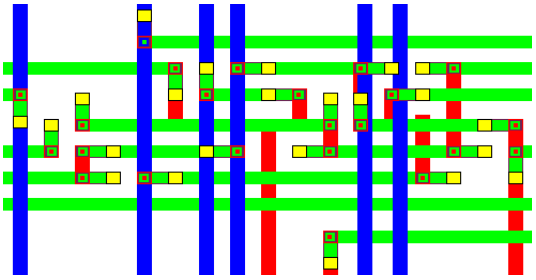

Fig. 5. An example double-via insertion [6], where different colors represent wires of different layers, and a yellow square represents a redundant via.

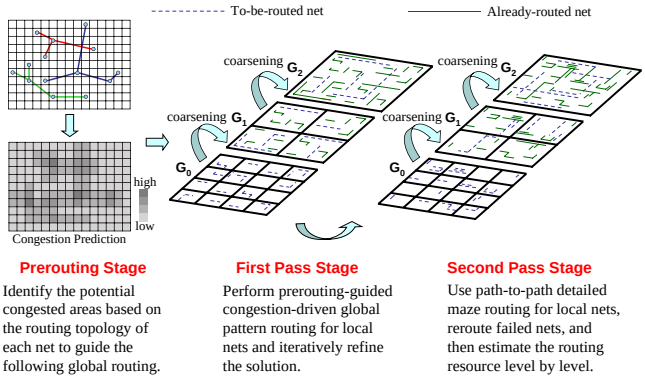

Fig. 6. The two-pass, bottom-up routing framework.

they formulated the problem as a multi-objective maze routing problem and applied Lagrangian relaxation to solve it. However, they only consider the redundant via at the detailed routing stage, their cost modeling for the number of vias is not accurate enough, and the high time complexity of Lagrangian relaxation limits the feasible problem size to be within hundreds of nets.

Yao et al. [43] developed a grid-based router which features via-minimization global routing followed by double-via aware detailed routing. The work claimed that the post-layout double-via insertion problem can be solved by a maximum bipartite matching formulation, which was recently shown to be incorrect for some cases by Lee and Wang in [20].

Lee and Wang [20] formulated the double-via insertion problem as a maximum independent-set (MIS) problem. Since the MIS problem for a general graph is NP-complete, they resorted to heuristics for the problem.

Luo et al. [26] considered the single vias of a design one by one to perform redundant-via insertion, and therefore their approach can get a locally optimal solution. Besides, since the approach might change the routing results of the timing non-critical nets, it may also induce timing violations even if designers prohibit the timing-critical nets from redundant-via insertion.

Chen et al. [6] presented a new full-chip gridless routing system considering double-via insertion for yield enhancement. To fully consider double vias, the router applies a novel two-pass, bottom-up routability-driven routing framework whose flow is shown in Figure 6. In this work, for each net, its cost function is defined as a weighted summation of the number of vias in the net and redundant-via related penalty function for the net. Moreover, a new post-layout double-via insertion algorithm was also proposed to achieve a higher insertion rate. Based on a bipartite graph matching formulation, they developed an optimal double-via in-

sertion algorithm for the cases with up to three routing layers and the stack-via structure, and then extend the algorithm to handle the general cases. Experiment results show that the method significantly improves the via count, the number of dead vias, double-via insertion rates, and running times.

Lee et al. [21] recently addressed the problem of simultaneously performing redundant-via insertion and line-end extension in the post-routing stage under via-density consideration. Via-density rules constrain the maximum and minimum numbers of vias in each layout area of a pre-defined size. A two-stage approach was proposed to solve this problem. In the first stage, the approach ignores the maximum via-density rule and tries to insert redundant vias and line-end extended vias as many as possible. This is done by formulating the problem as a maximum weighted independent-set (MWIS) problem and solved by a heuristic modified from [20] equipped with two speed-up techniques. In the second stage, excess redundant vias are removed from the violating regions such that after the removal, the maximum via-density rule is met while the total number of redundant vias removed is minimized. This density-aware redundant-via removal problem is formulated as a set of smaller zero-one integer linear programming (0-1 ILP) problems, each of which can be solved independently without sacrificing the optimality. This is the first work which concurrently considers redundant-via insertion, line-end extension, and via density.

B. Diode/Jumper Insertion for Antenna Effect

The antenna effect is resulted from the charges collected on the floating interconnects which are connected to only a gate oxide. During the metallization, long floating interconnects act as capacitors and store charges gained from the energy provided by fabrication steps such as plasma etching, CMP, etc. If the collected charges exceed a threshold, Fowler-Nordheim (F-N) tunneling current will discharge through the thin oxide and damage the gate. Nevertheless, the gate damage can be avoided if the collected charges can be released before exceeding the threshold through a low impedance path, such as a diffusion. For example, considering the routing in Figure 7, after manufacturing metal 1 (see Figure 7(b)), the collected charges on the right metal 1 pattern may cause damage to the connected gate oxide. The discharging path is constructed after manufacturing metal 2 (see Figure 7(c)), and thus the charges can be released through the connected diffusion on the left side.

There are three popular solutions including jumper insertion, embedded protection diode, and diode insertion after routing [7]. The difference between diode insertion and jumper insertion lies in the consumed resources of the fixed circuit. For jumper insertion, each jumper needs free spaces to route to the top-metal layer, and it incurs at least two vias for each jumper. For diode insertion, the consumed resources are the free spaces on the substrate. If a violating wire lies above a space that can insert a diode, the diode is directly inserted below the wire. Otherwise, if there is no free space under the wire, extension wires are necessary to connect the violating wire to a diode-insertion space [16].

Most previous works [15, 16, 35, 36, 40] fixed the antenna violations by jumper insertion or diode insertion alone, and thus the interaction between jumper insertion and diode insertion is ignored. For example, Su and Chang in [35] formulated the jumper insertion for antenna avoidance/fixing as a tree-cutting problem. They showed that the tree-cutting problem exhibits the properties of optimal substructures and greedy choices. With these properties, they presented a loglinear-time exact jumper insertion algorithm that uses the minimum number of jumpers to avoid/fix the antenna violations in a routing tree. Both the vias for jumper insertion and the extension wires for diode insertion will increase the driving load of the antenna-violating wire, and thus the incurred RC delay will affect the circuit performance. Therefore, in order

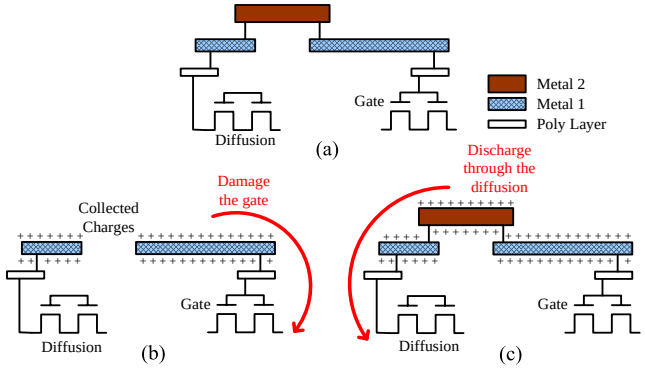

Fig. 7. Illustration of the antenna effect: (a) An example routing. (b) Late stage of metal-1 pattern etching of Figure (a), where the collected charges on the right side of the metal-1 pattern may cause damage to the connected gate oxide. (c) Late stage of metal-2 pattern etching of Figure (a), where all the collected charges can be released through the connected diffusion on the left side.

to minimize the cost of fixing the antenna violations, the interaction between diode insertion and jumper insertion should be considered. Based on a minimum-cost network-flow formulation, Jiang and Chang [18] presented a polynomial-time optimal simultaneous diode/jumper insertion algorithm for antenna violation fixing, which achieves much higher antenna fixing rates than the other works with jumper insertion or diode insertion alone.

IV. Future Research Directions

In this section, we provide some future research directions in physical design for manufacturability and reliability.

1. **OPC-Aware Placement:** Manufacture closure urgently demands lithographically robust layouts. If the final design does not give an optical friendly layout, it will complicate the process of mask synthesis. Since most of the resource in critical layers is occupied by cell structures, placement results directly affect the difficulty of mask design and the final yield. Nowadays, model-based OPC is broadly employed to accurately control the CD of a layout. An OPC corrector iteratively modifies the shapes of features till an aerial image simulator approves the revised layout. However, this correction procedure is sensitive to the initial layout. An OPC-friendly placement can greatly reduce the computational time and the size of mask database (GDSII). Further, the mask turnaround time can be shortened because the simple layout geometry eases the mask writing and inspection processes. Thus, a possible research direction is to consider the OPC issues in the placement stage such that favorable placement results for OPC can be produced.
2. **RET-Aware Routing:** Although RET-aware Routing has been studied to some degree, there is still much room for research in this topic. It is desired to develop a technique that can accurately predict RET behaviors and facilitate the manufacturing process, applying OPC, PSM, or more than one RET at the same time. Further, since the simulation for RET behaviors is usually very time-consuming, the efficiency should always be considered.
3. **PSM-Aware Layout Modification:** Recently the half-node technique has become a popular technique for massively produced designs. For example, if a 90nm design is ported to the 80nm half-node process, the die size can be reduced by 19%, as reported

in [38]. Thus, this technique significantly reduces cost-per-die. However, not all the geometries on a layout can be shrunk down linearly since it may violate design rules. In order to prevent the increase of interconnect resistance, excessively narrowing down wires is also not preferred. Thus, wire spacing is often sacrificed. Since AltPSM can substantially reduce the pitch of a layout, this technique is suitable for the half-node process. Berman et al. [2] proposed an approach to minimize the estimated cost of revising layouts and try to make them comply with the phase-assignment constraints. The method first deletes from the given conflict graph a set of edges with the minimum total cost and then enlarge the spacing corresponding to the chosen edges to remove phase-conflict cycles. However, because of the intrinsic limited resource on silicon, not all these edge deletion operations are allowed to feasibly map back to the replacement of wire segments on the layout. Therefore, it is important to develop automated layout fixers that can simultaneously consider the cost and feasibility when modifying a layout for the half-node technique.

4. **RDR-Aware Routing:** The concept of restricted design rules (RDRs) appears to enhance manufacturability by restricting the layouts that designers produce. Using only regular features in a layout will improve lithographic printability and make RETs easier to implement. However, because over-restricted rules may decrease the performance and increase the chip area, it is difficult to strictly follow these RDRs in practice. Therefore, an appropriate RDR-aware router should follow RDRs in lithographically critical regions but allow some exceptions of RDRs in non-critical regions to optimize the performance and the chip area. For this reason, an analyzer should also be provided to identify the critical regions.
5. **Hybrid OPC Modelling:** There are two general types of OPC systems, rule-based OPC and model-based OPC. A rule-based OPC determines how to apply OPC by given rules, while a model-based one used mathematical models of the fabrication process. There is a trade-off between accuracy and efficiency. A rule-based OPC is usually more efficient but less accurate than a model-based OPC. Thus, a hybrid OPC balancing the two important factors is desired, which can also play an important role to guide an OPC-aware router with sufficient accuracy and efficiency at the same time.
6. **Two-Dimensional SRAF Optimization:** To prevent two-dimensional SRAF placement conflicts, existing works apply the Voronoi diagram [29] or a model-based conflict resolution [1], but there is still no well-formulated problem being proposed to deal with this two-dimensional conflict problem. The challenges of the SRAF placement include the number, sizes, and positions of SRAFs. Moreover, the distances from SRAFs to the main shapes and those between SRAFs are also constrained. Consequently, it is desired to give a formal formulation of the SRAF placement problem and develop an effective and efficient solution for this problem.
7. **Wire-Density Modeling:** For a better CMP process, all existing approaches consider the wire density inside each global-routing tile. Because the topography is a global, long-range phenomenon, handling density only in a global-routing tile may incur large density variations among neighboring tiles, as shown in Figure 8. As a result, the density variations between neighboring subregions are not controlled, and thus the topographical thickness loss still occurs. For example, in Figure 8, there is a subregion with wire density 0.5, and one of its neighboring subregion has wire density 0.1. Consequently, the modeling of wire density should be reconsidered at a more global perspective.
8. **Cost Metric of Wire Density:** To control the wire density, Cho et al. [9] performed a minimum pin-density routing to avoid global-routing paths from passing through over-dense areas, but there are some limitations in this work. As the global-routing instance shown in Figure 9(a), although the routing path passes a region with fewer pins, it may exacerbate the over-dense areas in its adjacent regions. Besides, the pin density is not directly proportional to the wire density as shown in Figure 9(b). Further, most existing try to optimize the wire density for a given window for CMP control. We shall point out that this is not a right metric and a common pitfall for CMP control; instead, it is more desirable to minimize the *variation* of wire density, i.e., the density gradient, for better CMP control.

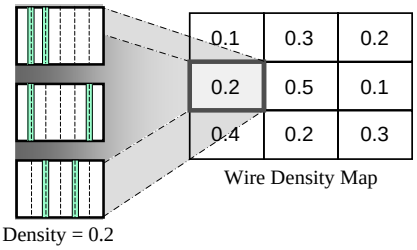

Fig. 8. Density variations among neighboring subregions impact topography, and different wire distributions in a subregion exist even under the same density.

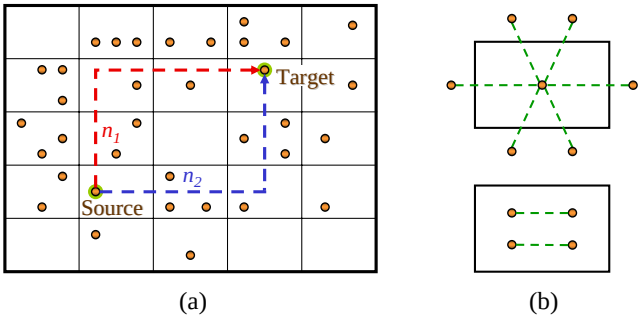

Fig. 9. Disadvantages of minimum pin-density routing. (a) Path n_1 passes fewer pins but tends to exacerbate the over-dense areas in its adjacent regions, whereas path n_2 passes more pins but leads to better balanced wire density. (b) Small pin count may still contribute to large wire density in a global tile.

9. **Timing-Aware Double-Via Insertion:** According to our empirical study and industry experience, it has been observed that the addition of redundant vias could change the timing behavior of a design positively and negatively. In other words, some path delays may increase while some others may decrease. Although Luo et al. [26] has considered the timing issue, they cannot guarantee that the resulting design can still satisfy timing constraints after applying their approach. Therefore, how to tackle the timing issue more accurately during double-via insertion is still worthy for further study.
10. **Multiple-Cut Via Insertion:** For high-activity, high-current, and power nets, more than one redundant via is usually desired to be inserted for them to further enhance the yield and reliability of the vias located on those nets [10, 25, 32, 34]. Therefore, how to efficiently and effectively insert multiple-cut vias for those nets is also an interesting problem. Furthermore, the single vias located on the lower layers generally have smaller dimensions and hence have higher probability of becoming invalid; therefore, the lower-layer

vias should have higher priority for adding redundant vias than the others.

11. **Cost Variation of Jumper Insertion in Different Layers:** As mentioned earlier, jumper insertion reroutes nets to the top-metal layer by using two vias. Previous works for jumper insertion do not consider the cost difference in adding a jumper from a lower metal layer and from a higher metal layer to the top-metal layer. Obviously, the lower jumpers (e.g., from the metal-1 layer to the top-metal layer) consume vias that cross more metal layers and thus should be assigned larger costs than higher jumpers (e.g., from the metal-3 layer to the top-metal layer). For the aforementioned tree-cutting problem for antenna fixing/avoidance, considering the cost variation would incur two independent weights for each tree edge, one for the antenna charge and the other for the jumper cost. The problem can be formulated as to optimize the total jumper cost such that the antenna rules are satisfied. We conjecture this problem to be NP-complete, and thus an effective and efficient heuristic is desired.
12. **Correlation of Diode/Jumper Insertion for Antenna Effect:** There are various consumed resources between diode insertion and jumper insertion, resulting in different design costs. Jiang and Chang [18] defined the cost function composed of the total wire-length of extension wires (for diodes) and the total number of jumpers to minimize the total delay. If the objective is changed or a more precise delay model is used to calculate the induced total delay, the cost function for the optimization problem may be different from that in [18]. Furthermore, new algorithms may be needed to solve the optimization problem.

V. Conclusions

With the imperfect manufacturing process, yield and reliability have become first-order cost metrics. Physical design plays an essential role to ensure the success of manufacturing and improve yield and reliability. Many existing works have shown the effectiveness of physical design for this requirement, but there are still many opportunities for future research to further improve the manufacturability and reliability of the final designs.

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