Thermal-driven Analog Placement Considering Device Matching

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ABSTRACT

With the thermal effect, improper analog placements may degrade circuit performance because the thermal impact from power devices can affect electrical characteristics of the thermally-sensitive devices. There is not much previous work that considers the desired placement configuration between power and thermally-sensitive devices for a better thermal profile to reduce the thermally-induced mismatches. In this paper, we first introduce the properties of a desired thermal profile for better thermal matching of the matched devices. We then propose a thermal-driven analog placement methodology to achieve the desired thermal profile and to consider the best device matching under the thermal profile while satisfying the symmetry and the common-centroid constraints. Experimental results based on real analog circuits show that our approach can achieve the best analog circuit performance/accuracy with the least impact due to the thermal gradient, among existing works.

Categories and Subject Descriptors: B.7.2 [Integrated Circuits]: Design Aids - Layout, Placement and Routing

General Terms: Algorithms, Design, Reliability

Keywords: Analog placement, thermal matching

1. INTRODUCTION

In modern RF or analog and mixed-signal IC design, the thermal issue becomes more and more important during device placement, especially when integrating power amplifiers and other analog or mixed signal circuits into the same chip, such as the RF system [13] shown in Figure 1. The RF system contains power devices in the power amplifiers and thermally-sensitive matched devices which appear in the mixer, the low-pass filter, and other sub-circuits. Generally, the power devices consume much more power than all the other devices and may generate significant heat which may affect the electrical properties of the thermally-sensitive matched devices, such as the saturation current, I_{dsat}, of a MOS transistor. Consequently, it may degrade the circuit performance or even change the whole circuit behavior.

According to [4, 5], the matched devices should be in *symmetric* and/or *common-centroid* placements. Ideally, if the heat of the whole chip is evenly distributed, the devices can be thermally

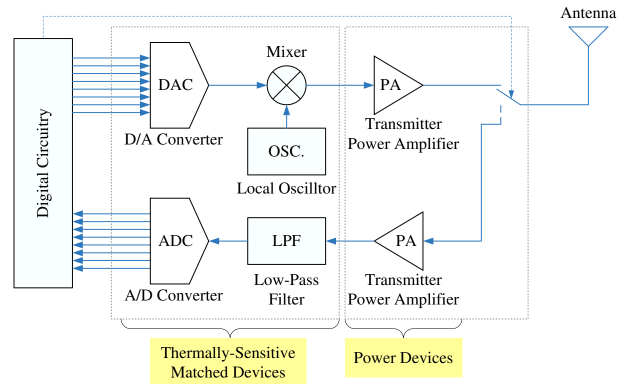
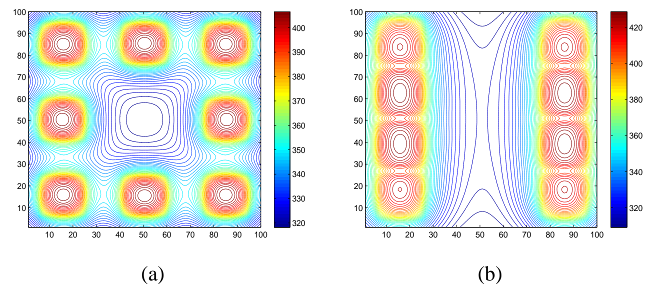


Figure 1: The block diagram of a generic RF system.

matched very well by these techniques. However, the power devices always generate certain thermal gradients on the chip which cause the devices with symmetric and/or common-centroid placements to become mismatched. To consider the thermally induced mismatch, the *thermal profile* of the chip induced by the arrangements of power devices should further be considered together with symmetric and common-centroid placements of thermally-sensitive matched devices in analog layouts. Since the devices other than the power devices in Figure 1 consume much less power, we simply consider them as non-power devices. Figure 2 shows two different thermal profiles based on different arrangements of the power devices in the power amplifiers. For better thermal matching of all thermally-sensitive matched devices, the thermal profile in Figure 2(b) is superior to that in Figure 2(a), which will be further discussed in Section 2.



(a) (b)

Figure 2: Thermal profiles based on two kinds of power device arrangements. (a) The thermal profile where power devices are evenly distributed at four sides of the chip. (b) The thermal profile where power devices are evenly distributed at two opposite sides of the chip.

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1.1 Previous Work

Analog placement considering device matching constraints has been extensively studied based on various floorplan representations, such as the absolute floorplan representation [4, 7], B*-tree [2, 17], hierarchical B*-tree (HB*-tree) [8], sequence pair (SP) [1, 18], transitive closure graphs (TCG) [10, 22], and corner block list (CBL) [11] for symmetry constraints, and CBL and grid-based approaches [14] for common-centroid constraints. Among these works, only [4, 7, 11] addressed thermally constrained symmetric placement.

Cohn et al. [4] introduced a basic placement configuration for thermal device matching, which is to position the power devices along a thermal symmetry line bisecting the chip such that the isothermal contours are symmetric across the symmetry line. The thermally-sensitive matched devices are then placed symmetrically about the power devices to have the same ambient temperature. Consequently, the thermal mismatch between the matched devices is reduced. Although such an approach is very effective, it limits the layout design with only one symmetry line on the chip. Such a configuration for thermal device matching is not applicable to modern RF or analog and mixed-signal design as seen in Figure 1, which contains multiple symmetry groups with different symmetry lines in different sub-circuits.

Both Lampaert et al. [7] and Liu et al. [11, 12] presented their thermally constrained analog placement by the thermal profile computation. During placement iterations, the temperature of all matched devices are calculated based on certain thermal models. The thermally-induced mismatch is then optimized by minimizing the temperature differences between the symmetric devices. Although their approaches do not limit the layout with only one symmetry line, it is time-consuming to calculate the temperature of all matched devices during placement iterations when the number of the matched devices is large. In addition, it is difficult to guarantee that all devices are thermally matched by summing up the temperature differences between symmetric devices in each symmetry group and other placement objectives such as reducing placement area and thermal hot spots [11]. None of the previous works directly optimizes the thermal profile based on the power device arrangement to achieve better thermal matching of the devices.

1.2 Our Contributions

In this paper, we propose the *first* thermal-driven analog placement considering thermal device matching by directly optimizing the thermal profile of analog layouts. We introduce the desired thermal profile and the corresponding placement configuration for better device matching, especially when placing multiple symmetry groups with different symmetry lines. We then present our placement methodology to simultaneously place all devices, including power devices and thermally-sensitive matched devices with either the symmetry or the common-centroid constraint. We adopt a table-lookup approach to speed up the thermal profile computation. The thermal profile is optimized based on coarse-grid and fine-grid thermal tables at different placement stages. Since the objective based on our approach is to generate the desired thermal profile, instead of to minimize the temperature differences between matched devices, the time complexity is only dependent on the number of power devices, but is independent of that of matched devices. Therefore, our approach is more efficient and scalable, which significantly improves the runtime when placing a large number of thermally-sensitive matched devices in modern analog designs. Finally, we propose the *first* thermal-driven common-centroid placement (TCCP) algorithm that considers the best device matching under the desired thermal profile. Experimental results show that our approach can achieve better runtime and the best analog circuit performance/accuracy in the presence of thermal gradients, compared with the previous works.

The remainder of this paper is organized as follows. Section 2 introduces the desired thermal profile for thermal device matching and the corresponding placement configuration. Section 3 presents our thermal-driven analog placement to generate the desired thermal profile based on the placement configuration while considering both symmetry and common-centroid constraints. Section 4 reports the experimental results, and finally Section 5 concludes this paper.

2. THE DESIRED THERMAL PROFILE

Before introducing our thermal-driven analog placement, we shall first consider the desired thermal profiles and the corresponding placement configuration. Inspired by manual layouts, the desired thermal profile should have the following properties:

- Lower temperature at thermal hot spots.
- Smoother thermal gradients at the non-power device areas.
- More separation between power and thermally-sensitive devices.
- More regular isothermal contours in either the horizontal or the vertical direction such that the matched devices can easily be placed along the contours.
- Larger accommodation areas for multiple thermally-sensitive device groups

By comparing both thermal profiles at the non-power device areas in Figure 2, although the one that the power devices are evenly distributed at four sides of the chip has lower temperature at the thermal hot spots, its thermal gradient, isothermal contours, and accommodation area are not as good as the other one that the power devices are evenly distributed at two opposite sides of the chip. Therefore, the thermal profile in Figure 2(b) is more desirable than that in Figure 2(a) when considering thermal matching in analog layouts. Since the isothermal contours in Figure 2(b) are very regular in the vertical direction, the thermally-sensitive matched devices can be placed along the isothermal contours anywhere in the placement area to have the same ambient temperature so that the thermally induced mismatches between the matched devices are reduced. In addition, when placing different symmetry groups in different sub-circuits, they are not necessary to share the common symmetry line bisecting the power devices. Consequently, the area utilization and the interconnecting wire length of the whole analog layout can further be optimized.

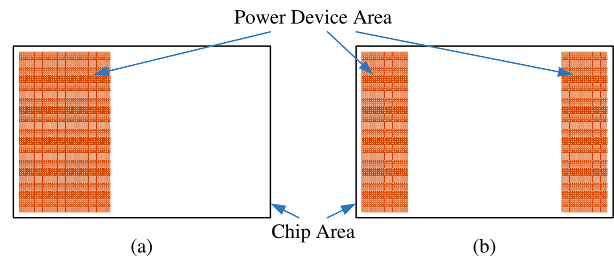


Figure 3: Placement configurations of power device area arrangements. (a) The power device area is arranged at one short side of the chip. (b) The power device areas are arranged at both short sides of the chip.

Based on the desired thermal profile in Figure 2(b), the corresponding placement configuration, especially the arrangement of power device areas, should be considered. According to [5], it is always recommended to place non-power, thermally-sensitive devices as far away from power devices as possible to alleviate thermal impacts from power devices. To allow more separation between power and thermally-sensitive devices on the same chip, the power devices are preferred to be arranged in the rectangular areas located at either one or both short sides of the rectangular chip as shown in Figure 3. The rest of the chip area is reserved for the placement of non-power devices, including the thermally-sensitive matched devices with either the symmetry or the common-centroid constraint. As both arrangements in Figure 3 are preferable, choosing the better arrangement further depends on other factors, such as the reduction of interconnections among devices and/or I/O pins, and the alleviation of thermal hot spots.

3. THERMAL-DRIVEN ANALOG PLACEMENT

We propose our thermal-driven analog placement to fulfill the desired thermal profile and the placement configuration introduced in the previous section by applying the simulated annealing algorithm [6] based on the hierarchical B*-tree (HB*-tree) and automatically symmetric-feasible B*-tree (ASF-B*-tree) floorplan representations [8] due to its efficiency and effectiveness to handle symmetry constraints based on the symmetry-island formulation. **Figure 4 shows a symmetric placement and its corresponding HB*-tree and ASF-B*-tree. Each module node, n_i, corresponds to a module b_i, and the hierarchy node n_{S0} corresponds to the symmetry island of the symmetry group S_0 containing a self-symmetric module, b_3^s, and a symmetry pair, (b_4, b_4'). The ASF-B*-tree represents the symmetric placement of S_0.**

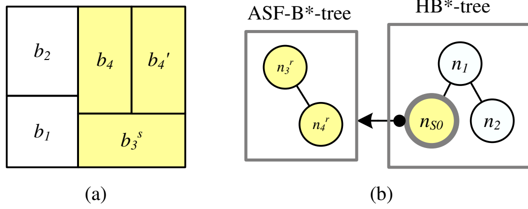


Figure 4: (a) A symmetric placement containing a symmetry group $S_0 = \{b_3^s, (b_4, b_4')\}$, and two non-symmetric modules, b_1 and b_2. (b) The corresponding HB*-tree and ASF-B*-tree of the placement in (a).

In addition to handling symmetry constraints, the HB*-trees can also be hierarchically constructed based on the hierarchical circuit clustering [9] so that the close proximity of devices in the same sub-circuit is preserved during placement. For example, we can use different HB*-trees to model the device placements in different sub-circuits such as those in Figure 1. Each HB*-tree modelling the placements of a sub-circuit is further linked by a hierarchy node in the top-level HB*-tree which models the top-level placement considering the topology among different sub-circuits.

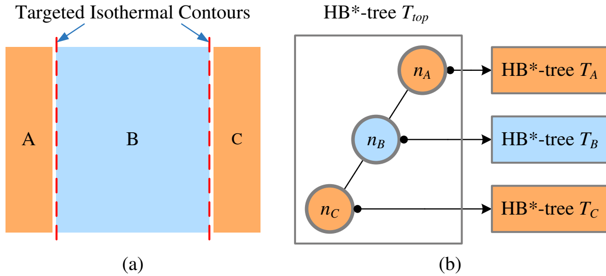


Figure 5: The placement configuration and its corresponding HB*-trees. (a) The placement configuration based on the power area arrangement in Figure 3. (b) The HB*-trees representing the topology among the three regions in (a).

We further extend the HB*-trees to handle the problem of thermal-driven analog placement. Figure 5(a) shows three regions A, B, and C in the whole placement area based on the desired placement configuration in Figure 3(b). The regions A and C are arranged to place power devices, while the region B is arranged to place non-power devices, including all thermally-sensitive matched devices. To represent the placement configuration in Figure 5(a), we consider the fixed structure of the top-level HB*-tree, T_{top}, as shown in Figure 5(b). The placements of power devices in the regions A and C are modelled by the HB*-trees T_A and T_C which are linked by the hierarchy nodes n_A and n_C respectively, while the placement of non-power devices in the region B is modelled by the HB*-tree T_B which is linked by the hierarchy node n_B. During the simulated annealing, a node can be moved from T_A to T_C, or vice versa, to optimize the interconnection wire length. If one of T_A and T_C becomes null, the placement configuration will be automatically reduced to that in Figure 3(a).

Given the following inputs and constraints:

- a set of device modules including power and non-power devices,
- power densities of all power devices,
- the targeted aspect ratio of the placement area,
- symmetry and common-centroid constraints for all matching device groups,

the objective of our thermal-driven analog placement is to obtain a placement P that minimizes the cost function, $\Phi(P)$, defined in Equation (1). In this equation, α, β, γ, and δ are user-specified parameters, A_P is the area of the bounding rectangle for the placement, W_P is the half-perimeter wire length (HPWL), R_P is the difference between the aspect ratio of P and the targeted aspect ratio, and T_P is the thermal cost of P based on the targeted placement configuration, which is further defined in Equation (2).

$$\Phi(P) = \alpha A_P + \beta W_P + \gamma R_P + \delta T_P. \quad (1)$$

$$T_P = (T_{l,max} - T_{l,min}) + (T_{r,max} - T_{r,min}). \quad (2)$$

Based on the desired thermal profile, we consider two targeted straight isothermal contours near the boundaries between the power and non-power device regions as seen in Figure 5(a). In Equation (2), $T_{l,max}$ and $T_{l,min}$ denote the maximum and minimum temperatures at the left targeted isothermal contour in Figure 5(a), while $T_{r,max}$ and $T_{r,min}$ denote the maximum and minimum temperatures at the right targeted isothermal contour. Since the power consumption between power and non-power devices is large in the typical RF system as seen in Figure 1, the heat generated by the non-power devices can hardly affect the thermal profile contributed by the power devices. Therefore, by minimizing the differences between the maximum and minimum temperatures at the same targeted isothermal contour, the desired thermal profiles in Figure 2(b) can be obtained.

3.1 Thermal Profile Computation

To obtain the temperature at each point on the targeted isothermal contours in Figure 5(a), it is required to compute the thermal profile based on a certain thermal model. The previous works [7, 11] compute the thermal profile by calculating approximated thermal equations based on different thermal models. Although it is fast to compute the thermal profile of a certain placement, it becomes inefficient when calculating those equations more than hundreds of thousands times to evaluate the thermal profiles of different placements during the simulated annealing process.

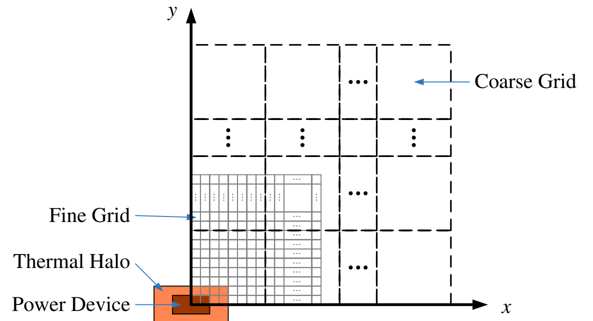


Figure 6: The coarse-grid and fine-grid thermal tables indicating the thermal profile of the power device with different precisions and scales.

Since the temperature at each point in the placement area can be calculated by the superposition of the thermal profiles contributed by all power devices placed at different locations according to [7, 11, 19], we adopt a table-lookup approach by constructing thermal

tables that store the thermal profile of each power device to facilitate the thermal profile computation. The thermal profiles of all power devices are pre-simulated using a thermal simulation tool, such as 3D-Thermal-ADI [19, 20] which is available in the public domain. Given the device area, device location, device power densities, targeted chip area, and other thermal coefficients, it will compute the thermal profile of the corresponding device. After the thermal simulation of all power devices, a *coarse-grid* and a *fine-grid* thermal tables are then constructed for each device to represent its thermal profile with different precisions at different scales as shown in Figure 6. Each grid (i, j) in the thermal table records a certain temperature $T(i, j)$ contributed by the corresponding power device. The coarse-grid thermal table indicates a global thermal profile covering the whole placement area, while the fine-grid thermal table shows the detail thermal profile near the placement of the corresponding power device. The sizes of the thermal tables depend on the trade-off between the memory usage and the precision we need for the thermal profile optimization. By assuming the isomorphic thermal profile of each device in four quadrants and sharing common thermal tables of some identical power devices, the size and the number of the thermal tables can effectively be reduced.

3.2 Thermal Profile Optimization

Based on the thermal tables illustrated in Figure 6, we optimize the thermal profile at three different placement stages. Before the placement process, the thermal halo of each power device is allocated. The global thermal profile optimization is then performed during the simultaneous placement of power and non-power devices. Finally, the detailed thermal profile optimization is processed for local placement refinements of power devices.

3.2.1 Thermal Halo Allocation

Since most of the power devices are arranged in the same power device area, the area is prone to have thermal hot spots. To effectively reduce the temperature at the thermal hot spots, a thermal halo should be added to each power device as shown in Figure 6. The thermal halo covers an area above a certain temperature in the fine-grid thermal table of the power device.

3.2.2 Global Thermal Profile Optimization

During the simulated annealing based on the HB*-trees, the placement of power and non-power devices are simultaneously optimized by minimizing the cost functions in Equations (1) and (2). At this stage, we only consider the coarse-grid thermal tables for the thermal cost in Equation (2) which is obtained by calculating the difference between the maximum and minimum temperatures at the coarse grids passed by the targeted isothermal contour as shown in Figure 7(a).

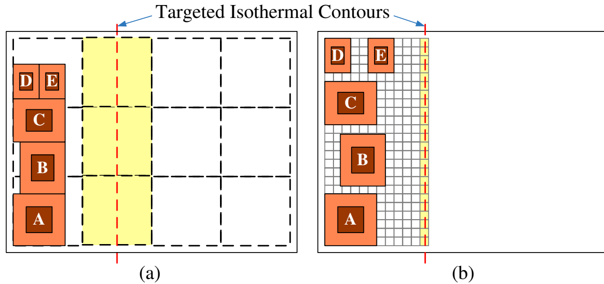


Figure 7: The placement of power devices are optimized based on (a) global and (b) detailed thermal profile optimization.

3.2.3 Detailed Thermal Profile Optimization

Once the placement of the power devices are optimized based on the global thermal profile optimization as seen in Figure 7(a), the detailed thermal profile optimization is further performed to obtain more desirable isothermal contours. We apply both vertical and horizontal local movements for the power devices on the fine grids as shown in Figure 7(b). The thermal cost in Equation (2) is calculated based on the fine-grid thermal tables to minimize the temperature difference among the fine grids passed by the targeted isothermal contour in Figure 7(b).

Since the vertical movement of the power devices does not affect the shape of the isothermal contour very much, we simply evenly distribute the power devices vertically by traversing the vertical constraint graph (VCG) representing the vertical relationship among the power devices, which can be converted from a B*-tree as described in [17].

To minimize the number of power devices that need to be moved during the horizontal local refinement, only those adjacent to the right boundary of the power device area should be considered, which are devices A, B, C, and E in Figure 7(a). These boundary devices can be identified by the contour data structure during packing a B*-tree [3]. By the iterative horizontal movement of the boundary devices, the thermal cost T_P in Equation (2) can further be minimized.

3.3 Thermal-driven Matching Device Placement

We consider the desired thermal profile in Figure 2(b) to place the thermally-sensitive matched devices with either the symmetry or the common-centroid constraint. For a matching device group with the symmetry constraint, the matched devices should be placed on the same isothermal contours to have the same ambient temperature so that the thermally-induced mismatch is minimized. Since the desired thermal profile has regular isothermal contours in either the horizontal or the vertical direction, all the symmetry device groups can simply be placed with their symmetry lines being perpendicular to the isothermal contours. The symmetric placements of all symmetry device groups with different symmetry lines can simultaneously be optimized during the simulated annealing based on the HB*-trees.

For a matching device group with the common-centroid constraint as shown in Figure 8, none of the previous works considers the thermal profile during the common-centroid placement. We propose our algorithm to generate a common-centroid placement for a matching device group while considering the desired thermal profile. Based on our approach, all possible common-centroid placements of each matching group with different aspect ratios are pre-generated, which is the same as the approach in [14]. When integrating the placement with other devices or device groups, a candidate of the pre-generated common-centroid placements is randomly selected during the simulated annealing based on the HB*-trees. The final candidates of all matching groups are simultaneously optimized based on the cost function in Equation (1).

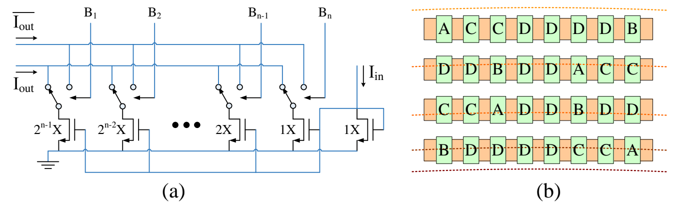


Figure 8: A matching device group with the common-centroid constraint. (a) A matching device group in the binary weighted current network. (b) A common-centroid placement of the matching device group in (a) containing four MOS devices, A, B, C, and D, having 4, 4, 8, and 16 sub-devices respectively. The dotted lines denote the isothermal contours.

Given a common-centroid device group G_{cc} containing q devices, i.e. $G_{cc} = \{b_1, b_2, \ldots, b_q\}$, and each device b_j has n_{b_j} sub-devices, to better match the device layouts, the size of all the sub-devices should be identical. Besides, in G_{cc}, the relationship between any two sub-device numbers n_{b_j} and n_{b_k} of devices b_j

and b_k is usually the ratio of power of two, i.e. $n_{b_j} = 2^l \times n_{b_k}$, where l is an integer. Furthermore, the sub-devices are preferred to be regularly placed in a two-dimensional array as shown in Figure 8(b). To minimize the thermal mismatch among the q devices in G_{cc}, we need to evenly distribute the sub-devices of each device along the direction of the thermal gradient.

Figure 8(b) shows the common-centroid placement of the 3-bit binary weighted current network illustrated in Figure 8(a). Device A denotes the MOS transistor connected to I_{in}, and devices B, C, D denote the MOS transistors connected to the control signals of B_3, B_2, and B_1, which have 4, 4, 8, and 16 sub-devices respectively. The isothermal contours, i.e. the dotted lines, are in the horizontal direction, implying that the direction of the thermal gradient is vertical. In the following, we simply consider the direction of the row (column) of the 2D array to be the same as that of the thermal gradient (contours).

To assign the sub-devices into a k-row 2D array while minimizing the thermal mismatch, the sub-devices of each device should be equally divided by k and assigned into one of the rows. For some cases, if the sub-device number of a device is not dividable with respect to the row number, we allow the sub-device number in each row with ± 1 tolerance. It should be noted that even the sub-device numbers of a device assigned to different rows are not equal, the sub-device number in the ith row should be the same as that in the $(k-i+1)^{th}$ row, or the symmetric row. Therefore, the common-centroid placement must be feasible. In Figure 8(b), the respective sub-device numbers of devices A, B, C, and D in each row are 1, 1, 2, 4 after the even assignment.

Once the sub-devices of each device are evenly assigned into rows, we should consider the diffusion-sharing for MOS transistors. We construct the diffusion graph of the sub-circuit in each row, and then find the Eulerian trail on the diffusion graph [15]. After the Eulerian trails are found, the sub-devices on the same Eulerian trail are merged. Considering the first row in Figure 8(b), there are three Eulerian trails, $C-C$, $D-D$, and $D-D$. Consequently, the six devices are merged into three sub-device groups, and the sub-devices in the symmetric row are also merged accordingly.

After considering the diffusion sharing, the column position of each sub-device or sub-device group in each row is assigned in a random order while keeping the symmetric row in the reverse order. Figure 8(b) shows the final common-centroid placement that minimizes the mismatch between the four devices due to the thermal gradient. The algorithm of the k-row thermal-driven common-centroid placement (namely, k-row TCCP) is summarized in Algorithm 1.

Algorithm 1 k-row TCCP

1: **for all** q devices in G_{cc} **do**
2: Evenly assign the sub-devices into k rows with the same number in $row[i]$ and $row[k-i+1]$;
3: **end for**
4: **for** i = 1 to $\lceil k/2 \rceil$ **do**
5: Merge the diffusion of the sub-devices in $row[i]$ and $row[k-i+1]$ based on the same Eulerian trails;
6: Place the (merged) sub-devices in $row[i]$ in a random order;
7: Place the (merged) sub-devices in $row[k-i+1]$ in the reverse order of that in $row[i]$;
8: **end for**

4. EXPERIMENTAL RESULTS

We implemented our placement algorithm in the C++ programming language on a Dual 2.8GHz Intel Pentium4 PC under the Linux operation system. We performed two sets of experiments: (1) one is based on the analog placement benchmarks in [2, 8, 17] consisting of analog designs, biasynth_2p4g and lnamixbias_2p4g, with different numbers of symmetry groups, and (2) the other is based on the real analog circuit, the binary weighted current network shown in Figure 8(a), containing a large common-centroid device group in which each device has different numbers of sub-devices of uniform sizes.

In the first set of the experiments, we compared our approach that optimizes the desired thermal profile with the other one that minimizes the temperature differences between devices of each symmetry pair. Both approaches applied the simulated annealing algorithm based on the HB*-trees and the cost function in Equation (1), while the later one applied a different thermal cost function T_P of placement P defined in Equation (3), which is the summation of the temperature difference of m symmetry pairs. **In Equation (3), T_{b_i} denotes the temperature of the device b_i, and $T_{b_{i,sym}}$ corresponds the temperature of the symmetric device of b_i.**

$$T_P = \sum_{i=1}^{m} |T_{b_i} - T_{b_{i,sym}}|. \tag{3}$$

Table 1 lists the names of the benchmark circuits ("Circuit"), the numbers of modules ("# of Mod."), the numbers of symmetry modules ("# of Sym. Mod."), the numbers of power device modules ("# of Power Mod."), the total module areas ("Mod. Area"), and the maximum temperature of the whole chip ("T_{Max}"), the maximum temperature difference of each symmetry pair ("Max ΔT_{sym}"), the total areas ("Area") and the runtimes ("Time") for both approaches, the temperature difference optimization ("Temperature Diff. Opt.") and the thermal profile optimization ("Thermal Profile Opt.").

Since there was no power device specified in the original benchmarks, we simply selected 11 devices in biasynth_2p4g and 10 devices in lnamixbias_2p4g as the power devices, and simulated the thermal profile of each device to obtain its thermal table. Compared with the approach based on the temperature difference optimization, our proposed approach results in less than one quarter temperature difference of the matched devices in a symmetry pair and 5.28X faster running time with comparable maximum chip temperature and total chip area. Figure 9 shows the resulting placement of lnamixbias_2p4g and its corresponding thermal profile. The devices in red color are the power devices, and those in other colors denote the symmetric devices.

In the second set of the experiments, we evaluated the thermally-induced mismatch within a common-centroid placement under the desired thermal profile by performing HSPICE simulation with pre-assigned temperature for each sub-device. The temperature of each sub-device in the common-centroid group can be extracted according to its location in the thermal profile once the whole common-centroid device group is placed at a certain position in region B in Figure 5(a). After performing HSPICE simulation, the temperature-dependent electrical parameters of each device were measured. Since our experiment is based on the binary weighted current network in Figure 8(a), which is commonly used in data converter systems, we measured the drain current I_D of each MOS transistor. For an n-bit data converter system, the I_D linearity may change maximally by $\pm\frac{1}{4}$LSB over the full temperature range to maintain monotonicity of the system, where LSB stands for the least significant bit in data converters [16]. If the difference between the ideal I_D and the real one, I'_D, is larger than $\pm\frac{1}{4}$LSB, the D/A converter will fail. If the thermally-induced mismatch value, σ, of a common-centroid placement shown in Equation (4) is less than one, the circuit is within the tolerance of the accuracy; otherwise, the circuit will fail.

$$\sigma = \frac{|I'_D - I_D|}{\frac{1}{4}LSB}. \tag{4}$$

Therefore, we compared the σ value of the resulting common-centroid placement based on our k-row TCCP algorithm with that based on the grid-based approach in [14] under the same ambient temperature or the same location in the thermal profile.

Table 2 lists the names of the benchmark circuits ("Circuit"), the numbers of devices ("# of Dev."), the number of sub-devices in each device ("# of Sub-devices"), and the σ values based on the grid-based approach [14] and our k-row TCCP algorithm. Methods 1–3 give three different assignments of the positions of the sub-devices based on the grid-based approach [14]. For Method 1 (Method 2), the devices containing the most (least) sub-devices were assigned first, so they were placed close to the centroid. For Method 3, the sub-devices were assigned in a random order. The results show

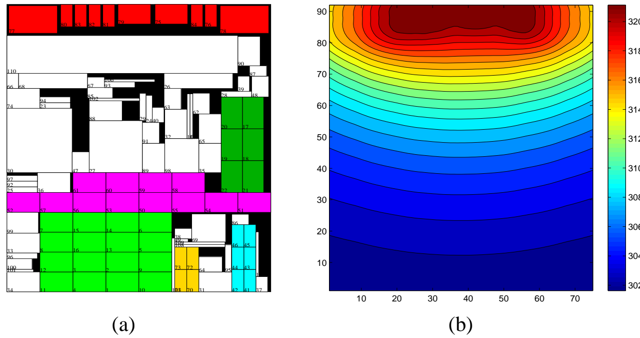
Table 1: Comparisons of the maximum temperature difference of each symmetry pair, area utilization, and CPU times for the approaches based on the temperature difference optimization and our thermal profile optimization.

Circuit	# of Mod.	# of Sym. Mod.	# of Power Mod.	Mod. Area ($10^3 \mu m^2$)	Temperature Diff. Opt.				Thermal Profile Opt. (This Work)			
					T_{Max} (K)	Max ΔT_{sym} (K)	Area ($10^3 \mu m^2$)	Time (s)	T_{Max} (K)	Max ΔT_{sym} (K)	Area ($10^3 \mu m^2$)	Time (s)
biasynth_2p4g	65	8+12+5	11	4.70	318.18	0.91	5.42	1524	321.10	0.22	5.47	385
lnamixbias_2p4g	110	16+6+6+12+4	10	46.00	322.58	2.66	56.71	5340	322.09	0.62	55.87	809
Comparison					1.00	4.21	1.00	5.28	1.00	1.00	1.00	1.00

Table 2: Comparisons of the circuit accuracy due to thermally-induced mismatches for common-centroid placements based on the grid-based approach and our k-row TCCP algorithm. The numbers in bold font mean that the circuits are within the tolerance of the accuracy.

Circuit	# of Dev.	# of Sub-devices	σ value			
			The grid-based approach [14]			TCCP
			Method 1	Method 2	Method 3	
bwcn_4bit	5	{4, 4, 8, 16, 32}	**0.06784**	**0.07040**	**0.04480**	**0.00128**
bwcn_5bit	6	{4, 4, 8, 16, 32, 64}	**0.26624**	**0.28416**	**0.00512**	**0.00512**
bwcn_6bit	7	{4, 4, 8, 16, 32, 64, 128}	1.06496	1.13664	**0.73728**	**0.04096**
bwcn_7bit	8	{4, 4, 8, 16, 32, 64, 128, 256}	4.24960	4.50560	**0.06144**	**0.20480**
bwcn_8bit	9	{4, 4, 8, 16, 32, 64, 128, 256, 512}	16.9984	18.14528	11.81696	**0.43008**

that our k-row TCCP algorithm obtained accurate results for all the bwcn circuits. The results based on "Method 3" are not as good as ours when the device/sub-device number in the common centroid group becomes larger. Both Methods 1 and 2 have very poor performance against the impact from the thermal gradient since only small circuits behave accurately. Therefore, our approach is the most effective one that considers the thermal gradient. The runtime of each approach is less than one second on a Dual 2.8GHz P4 PC.



(a) (b)

Figure 9: (a) The resulting placement of lnamixbias_2p4g. (b) The corresponding thermal profile.

5. CONCLUSIONS

In this paper, we have addressed the thermal issue in analog placement and studied the thermal-driven analog placement problem. We have proposed our algorithms to simultaneously optimize the placements of power and non-power devices to generate a desired thermal profile for thermally-sensitive matched devices. We have also proposed our analog placement methodology that considers the best device matching under the thermal profile while satisfying the symmetry and the common-centroid constraints. Experimental results based on the analog benchmark circuits and the real analog circuit show that our approach can achieve the best analog circuit performance/accuracy with the least impact due to the thermal gradient.

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