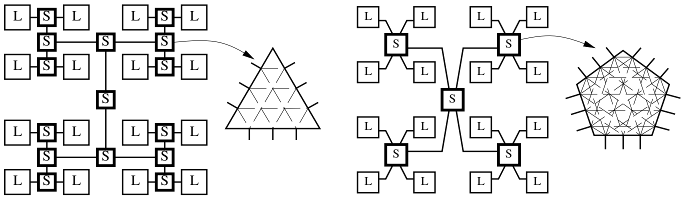
Generic Universal Switch Blocks *

Michael Shyu, Yu-Dong Chang, Guang-Ming Wu, and Yao-Wen Chang
Department of Computer and Information Science, National Chiao Tung University, Hsinchu 300, Taiwan

Abstract

A switch block M with W terminals on each side is said to be *universal* if every set of nets satisfying the dimension constraint (i.e., the number of nets on each side of M is at most W) is simultaneously routable through M [2]. In this paper, we present an algorithm to construct N-sided universal switch blocks with W terminals on each side. Each of our universal switch blocks has $\binom{N}{2}W$ switches and *switch-block flexibility* $N-1$ (i.e., $F_S = N-1$). We prove that no switch block with less than $\binom{N}{2}W$ switches can be universal. Further, the decomposition property of a universal switch block provides a key insight into its layout implementation with a smaller silicon area. We also compare our universal switch blocks with others of the topology associated with Xilinx XC4000-type FPGAs. Experimental results demonstrate that our universal switch blocks improve routability at the chip level.

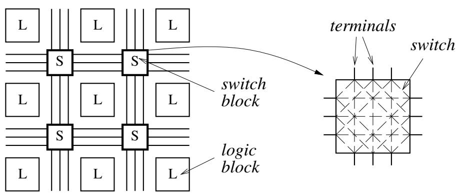


(a) (b) (c) (d)

Figure 2: Two HFPGA architectures. (a–b) A 2-HFPGA and its 3-sided switch block. (c–d) A 4-HFPGA and its 5-sided switch block.

1 Introduction

A conventional FPGA (see Figure 1(a)) consists of an array of logic blocks that can be connected by routing resources [1]. The logic blocks contain combinational and sequential circuits which are used to implement logic functions. The routing resources consist of wire segments and switch blocks. The intersection of a horizontal and a vertical channel is referred to as a switch block; the switch block serves to connect wire segments, and this requires using programmable switches inside it. Figure 1(b) illustrates a switch block in which the programmable switches, denoted by dashed lines between terminals, are shown.



(a) (b)

Figure 1: A conventional FPGA and its switch block. (a) A conventional FPGA architecture. (b) A conventional 4-sided switch block.

A *hierarchical FPGA* (*HFPGA*) (see Figures 2(a) and (c)) has a hierarchical interconnection structure [4, 5, 6]. An HFPGA can be hierarchically constructed by connecting logic blocks into clusters. First, k logic blocks are connected with a switch block. This step forms a one-level HFPGA. Then k clusters are recursively connected together as a *supercluster*. As k clusters are connected into a supercluster, the number of levels of the hierarchy will be increased by one. It is called a k-*HFPGA* if a cluster has k subclusters [6]. For example, Figure 2(a) is a four-level 2-HFPGA, and Figure 2(c) is a two-level 4-HFPGA.

In an HFPGA, the switch blocks are not the same as the conventional 4-sided switch blocks. For a k-HFPGA, each switch block, except the top-level one, is connected with k logic blocks and another switch block; therefore, the switch block can be considered a $(k+1)$-sided polygonal block. For example, the switch block of 2-HFPGA is 3-sided (see Figure 2(b)) and the switch block of 4-HFPGA is 5-sided (see Figure 2(d)). Therefore, switch blocks could have arbitrary numbers of sides, and it is significant to consider the design and analysis of switch blocks with multiple sides.

For the work on conventional switch blocks (4-sided blocks), Rose and Brown in [7] defined the flexibility of a switch block, represented by F_S, as the number of programing switches between a terminal and others. They investigated the effects of different switch-block flexibilities on routing and suggested that $F_S = 3$ should often be sufficient for high routability. Chang, Wong, and Wong first presented a class of universal switch blocks in [2]. A switch block M with W terminals on each side is said to be *universal* if every set of nets satisfying the dimension constraint (i.e., the number of nets on each side of M is at most W) is simultaneously routable through M [2]. They proved that each of the universal switch blocks can accommodate significantly more routing instances than the Xilinx XC4000-type one of the same size. Recently, a report on the layout implementations of the universal switch blocks and the XC4000-type ones has also concluded that the universal switch blocks need smaller silicon areas—the decomposition property of the universal switch blocks makes their layout very regular and compact [10].

In this paper, we present an algorithm to construct generic universal switch blocks with multiple sides. Each of our universal switch blocks has $\binom{N}{2}W$ switches and *switch-block flexibility* $N-1$ (i.e., $F_S = N-1$). We prove that no switch block with less than $\binom{N}{2}W$ switches can be universal. Further, the decomposition property of a universal switch block provides a key insight into its layout implementation with a smaller silicon area [10]. We also compare our universal switch blocks with others of the topology associated with Xilinx XC4000-type FPGAs. Experimental results demonstrate that our universal switch blocks improve routability at the chip level.

The remainder of this article is organized as follows. Section 2 introduces some notation and definitions. Section 3 proposes an algorithm to construct generic universal switch blocks with multiple sides. Section 4 shows our experimental results.

2 Preliminaries

An *NSB* is an N-sided switch block with W terminals on each side of the block. We represent an NSB by $M_{N,W}(T,S)$, where T is the set of terminals, and S the set of programming switches. Label the terminals $t_{1,1}, t_{1,2}, \ldots, t_{1,W}$, $t_{2,1}, t_{2,2}, \ldots, t_{2,W}$, $\ldots$, $t_{N,1}, t_{N,2}, \ldots, t_{N,W}$ starting from the first terminal on one side and proceeding clockwise. Figures 3(a) and (b) show the examples of $M_{3,3}(T,S)$ and $M_{5,3}(T,S)$, respectively. Let $T_i = \{t_{i,1}, \ldots, t_{i,W}\}$ and $S_i = \{(t_{m,n}, t_{u,v})|$ there exists a programmable switch between terminals $t_{m,n}$ and $t_{u,v}$, $t_{m,n} \in T_i$ or $t_{u,v} \in T_i, m < u\}$ for $1 \leq i \leq N$. Let $L_{i,W}(T_i, S_i)$ denote the terminals of side i and all switches connected with these terminals. Therefore, $S = \cup_{i=1}^{N} S_i$, $T = \cup_{i=1}^{N} T_i$, and $M_{N,W}(T,S) = \cup_{i=1}^{N} L_{i,W}(T_i, S_i)$. For convenience, we often refer to $M_{N,W}(T,S)$ and $L_{i,W}(T_i,S_i)$ simply as $M_{N,W}$ and $L_{i,W}$, respectively, omitting T and S, if there is no ambiguity about T and S, or T and S are not of concern in the context.

In an NSB, the switches are electrically *non-interacting* unless they share a

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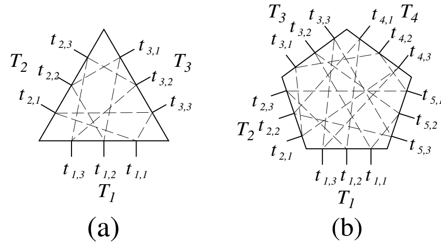


Figure 3: Two examples of N-sided switch blocks. (a) A 3-sided switch block ($M_{3,3}(T, S)$). (b) A 5-sided switch block ($M_{5,3}(T, S)$).

terminal. A *connection* is an electrical path between two terminals (say $t_{m,n}$ and $t_{u,v}$) on different sides of a switch block. If the switch $(t_{m,n},\ t_{u,v})$ is programmed to be "ON," then a connection between its two terminals is established. Because each connection is characterized by two sides of a block, we can classify all connections passing through a switch block into a number of categories. For an NSB, connections can be of $\binom{N}{2}$ types. Figures 4(a) and (b) show the type definitions of a 3-sided and a 5-sided switch blocks, respectively.

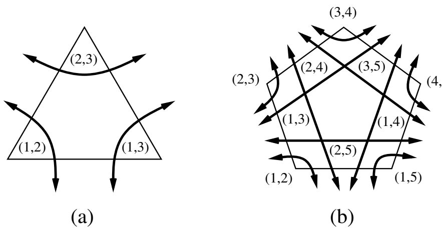


Figure 4: Examples of types definitions. (a) Three types of connections in a 3-sided switch block. (b) Ten types of connections in a 5-sided switch block.

A *routing requirement vector* (*RRV*) $\vec{n}$ for an NSB is an $\binom{N}{2}$-tuple $(n_{1,2},\ n_{1,3},\ \ldots,\ n_{1,N},\ n_{2,3},\ \ldots,\ n_{2,N},\ \ldots,\ n_{N-1,N})$, where $n_{i,j}$ is the number of type-(i, j) connections required to be routed through an NSB, $0 \leq n_{i,j} \leq W$ for $1 \leq i < j \leq N$. An RRV $\vec{n}$ is said to be *routable* on an NSB $M_{N,W}$ if there exists a routing for $\vec{n}$ on $M_{N,W}$. For example, in a 3-sided switch block, Figure 5(a) shows a routing instance with four nets corresponding to the RRV $(1, 2, 1)$, and Figures 5(b) and (c) show two switch blocks with the same flexibility ($F_S = 2$). The RRV $(1, 2, 1)$ is routable on the switch block shown in Figure 5(b), and a routing solution is illustrated by the thick lines. In Figure 5(c), however, there is always one net that cannot be routed into M_b. Thus the RRV $(1, 2, 1)$ is not routable on the switch block shown in Figure 5(c).

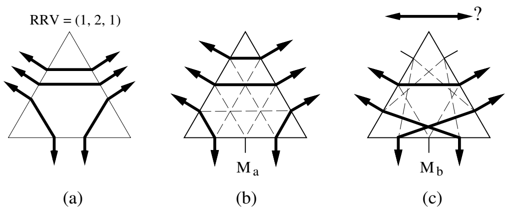


Figure 5: An example of routing on two 3-sided switch blocks of the same size and flexibility. (a) A routing instance $(1, 2, 1)$. (b) $(1, 2, 1)$ is routable on M_a. (c) $(1, 2, 1)$ is not routable on M_b.

The *routing capacity* of a switch block M is referred to as the number of distinct routable vectors on M; that is, the routing capacity of M is the cardinality $|\{\vec{n}|\vec{n}$ is routable on $M\}|$. A switch block M with W terminals on each side is called *universal* if every set of nets satisfying the dimension constraint (i.e., the number of nets on each side of M is at most W) is simultaneously routable through M [2]. The dimension constraint can be denoted by an N-tuple $\vec{D}_{N,W} = (W, W, \ldots, W)$. For an RRV $\vec{n}$, its *dimension requirement vector* (*DRV*) $\vec{d}$ is an N-tuple $(d_1,\ d_2,\ \ldots,\ d_N)$ (i.e., the routing requirements on sides $1, 2, \ldots, N$ are $d_1, d_2, \ldots, d_N$, respectively), where $d_i = \sum_{1 \leq j \leq N} n_{i,j}$ for $1 \leq i \leq N, n_{i,j} = n_{j,i}$ and $n_{i,i} = 0$. Let the DRV of an RRV $\vec{n}$ be $\vec{d}$. We have the following definition.

Definition 1 *A switch block $M_{N,W}$ is called universal if $\vec{d} \leq \vec{D}_{N,W}$ is the necessary and sufficient condition for $\vec{n}$ to be routable on $M_{N,W}$.*

Note that the number of nets routed through each side of a switch block can not exceed W; therefore, a universal switch block has the maximum routing capacity.

3 Universal Switch Blocks

To identify a universal switch block, we first consider the clique-based one associated with the Xilinx XC4000-series FPGAs. Figure 5(c) and Figures 6(a) and (b) show three such clique-based switch blocks of three, four, and five sides, respectively. Nevertheless, as shown in Figure 5(c), it is obvious that the clique-based switch blocks are not universal since the RRV $(1, 2, 1)$ which satisfies the dimension constraint is not routable on the 3-sided clique-based switch block of size three.

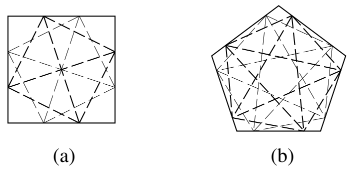


Figure 6: Clique-based switch blocks. (a) 4-sided. (b) 5-sided.

In the following, we consider a type of switch blocks that can be shown to be universal later.

3.1 Symmetric Switch Blocks

Algorithm: Symmetric_Switch_Block(N, W)
Input: N—number of sides;
W—number of terminals on each side.
Output: $M_{N,W}(T, S)$—the N-sided symmetric switch block of size W;
T: set of terminals; S: set of switches.
/* See Figure 3 for the terminal labeling. */

```
T ← t_{i,j},   ∀i = 1, 2, ..., N,   ∀j = 1, 2, ..., W;
S ← ∅;
for k = 1 to ⌊W/2⌋ do
    for i = 1 to N do
        for j = 1 to N do
            if i ≠ j
                S ← S ∪ {(t_{i,k}, t_{j,W−k+1})};
if W is odd
    for i = 1 to N do
        for j = 1 to N do
            if i ≠ j
                S ← S ∪ {(t_{i,⌈W/2⌉}, t_{j,⌈W/2⌉})};
Output M_{N,W}(T, S).
```

Figure 7: Algorithm for constructing an N-sided SSB of size W.

Let N ($N = 2, 3, 4, 5, \ldots$) be the number of sides of a switch block and W the size of the switch block. Algorithm Symmetric_Switch_Block shown in Figure 7 constructs a switch block $M_{N,W}$. We refer to the topology of the switch block constructed by the algorithm as the *symmetric topology* and the switch block as the *symmetric switch block (SSB)*. Figure 8 shows three examples of SSBs. For an SSB, it has a flexibility (F_S) of $N - 1$; thus, the total number of switches used in the SSB is $\frac{N \times W \times F_S}{2} = \frac{N(N-1)}{2} W = \binom{N}{2} W$. Note that the SSB shown in Figure 8(b) is a universal switch block proposed in [2]. For the SSBs, we have the following properties.

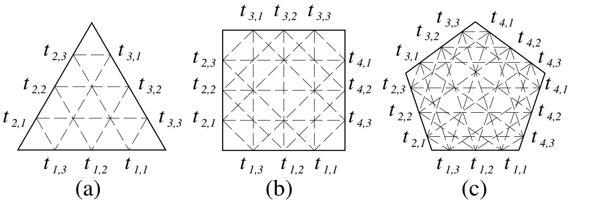


Figure 8: Three SSBs ($W = 3$). (a) 3-sided SSB. (b) 4-sided SSB. (c) 5-sided SSB.

Lemma 1 *(Decomposition Property) An SSB can be partitioned into* $\lfloor W/2 \rfloor$ *symmetric sub-blocks of size two and* $(W \bmod 2)$ *symmetric sub-block(s) of size one.*

Lemma 2 *(Reduction Property)* $M_{N,W}$ *is an SSB, where* $N \geq 3$*, so is* $M_{N-1,W} = M_{N,W} \setminus L_{i,W}, 1 \leq i \leq N$.

Figure 9 illustrates the decomposition property. Note that the sub-blocks of each of the SSBs are non-interacting to each other, thus each sub-block can be considered independently. Lemma 1 is not only an important property in the proof of the universality of SSBs, but also the key to the layout implementation of an SSB with a smaller silicon area—the symmetric sub-block of size two is a building block for a larger SSB (see Figure 9), which can make the layout of an SSB very regular and compact [10]. Figure 10 illustrates the reduction property; after removing one side i (terminals and switches) from an SSB $M_{5,2}$, the remainder is an SSB $M_{4,2}$.

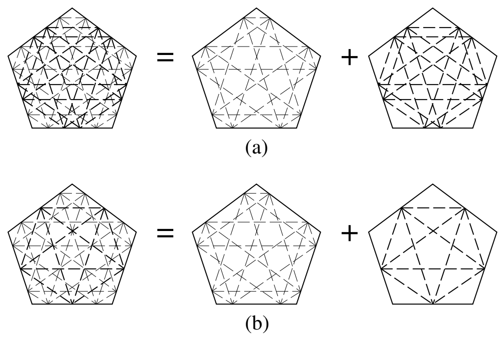


Figure 9: Two 5-sided SSBs and their sub-blocks. (a) Decomposition when $W = 4$. (b) Decomposition when $W = 3$.

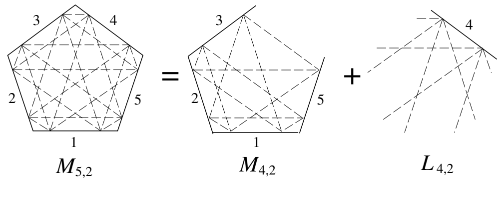


Figure 10: Reduction of a 5-sided SSB.

3.2 Universality of Symmetric Switch Blocks

Let $R(N, W)$ denote the set of all RRVs that satisfy the dimension constraint for an N-sided switch block of size W. We shall prove that each RRV in $R(N, W)$ is routable on our SSBs. The size of $R(N, W)$, however, grows dramatically with N and W. (Specifically, the cardinality of $R(N, W)$ grows in $O(W^{\binom{N}{2}})$.) It is thus desired to identify "critical" RRVs in $R(N, W)$.

3.2.1 Minimal Dominating Set of RRVs

For each $\vec{m}, \vec{n} \in R(N, W)$, $\vec{n}$ is said to *dominate* $\vec{m}$ if $\vec{n} \geq \vec{m}$, i.e., $n_{i,j} \geq m_{i,j}, i, j = 1, 2, \ldots, N$. Any RRV $\vec{m}$ is routable on a switch block $M_{N,W}$ if there exists another RRV $\vec{n}$ that is routable on $M_{N,W}$ and $\vec{n} \geq \vec{m}$ [9]. We have the following definition.

Definition 2 *A subset* $R_d(N, W)$ *of* $R(N, W)$ *is a dominating set of* $R(N, W)$ *if* $\forall \vec{m} \in R(N, W)$, $\exists \vec{n} \in R_d(N, W)$ *such that* $\vec{n} \geq \vec{m}$*. A dominating set* $R_d(N, W)$ *is minimal if* $\forall \vec{n_i}, \vec{n_j} \in R_d(N, W), i \neq j$, $\vec{n_i} \not\geq \vec{n_j}$ *and* $\vec{n_j} \not\geq \vec{n_i}$.

An RRV $\vec{\gamma} \in R(N, W)$ is called a *maximal RRV* (*MRRV*) if there exists no other RRV in $R(N, W)$ that dominates $\vec{\gamma}$. The following lemma is the key to find the minimal dominating set of $R(N, W)$. It is clear that $\Gamma(N, W) = \{\vec{\gamma} | \ \vec{\gamma} \ is \ an \ MRRV \ in \ R(N, W)\}$ is the minimal dominating set of $R(N, W)$. Then we can rewrite Definition 1 as follows:

Lemma 3 *A switch block* $M_{N,W}$ *is universal iff* $\vec{\gamma}$ *is routable on* $M_{N,W}, \forall \vec{\gamma} \in \Gamma(N, W)$.

Based on Lemma 3, we shall focus our discussions on $\Gamma(N, W)$. We have the following lemma associated with MRRVs.

Lemma 4 *When an MRRV* $\vec{\gamma} \in \Gamma(N, W)$ *is routed on an* N*-sided switch block of size* W*, all unused terminals, if any, are on the same side and the number of unused terminals* $\phi_{unused} = 2k + (N \ mod \ 2)(W \ mod \ 2)$*, where* $k = 0, 1, 2, \ldots,$ *or* $\lfloor W/2 \rfloor$.

We first consider the MRRVs in $\Gamma(N, 2)$. By Lemma 4, we can classify the MRRVs into two types. One type is that all terminals are used (i.e., $\phi_{unused} = 0$), and we call it a *complete MRRV* (see Figure 11 (a)). The other type is that two terminals on some side are unused (i.e., $\phi_{unused} = 2$), and we call it a *degenerate complete MRRV* (see Figure 11 (c)).

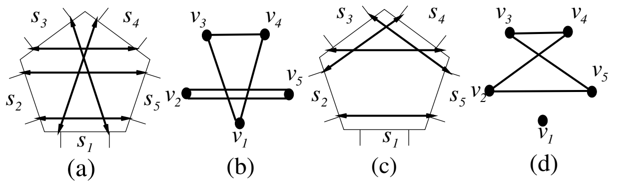


Figure 11: Two routing examples of MRRVs in $\Gamma(5, 2)$. (a–b) A complete routing example and its corresponding RRG. (c–d) A degenerate complete routing example and its corresponding RRG.

For an RRV $\vec{n}$, we construct an undirected *routing requirement graph* (*RRG*) G [3]. Each vertex v_i in $V(G)$ represents one side s_i of $\vec{n}$. If there is a routing requirement between two different sides s_i and s_j, we introduce an edge between vertices v_i and v_j. For a complete MRRV in $\Gamma(N, 2)$, since all terminals are used, the degree of each vertex in the corresponding RRG is two (see Figure 11 (b)). For a degenerate MRRV in $\Gamma(N, 2)$, since all terminals are used except two terminals on some side, say side s_i, the degree of each vertex in the corresponding RRG is two except that the degree of v_i is zero (see Figure 11 (d)). We refer to an RRG with the degree of each vertex two as a *2-RRG*. A cycle in an RRG is called a *routing requirement cycle* (*RRC*). Two routing cycles C_i and C_j are *disjoint* if $V(C_i) \cap V(C_j) = \emptyset$. A *disjoint routing requirement cycle set* (*DRRCS*) Δ is a set of disjoint RRCs. We proceed to prove the universality of SSBs. Based on the reduction property of SSBs (Lemma 2), we have the following lemma by induction.

Lemma 5 *Given a DRRCS* Δ*, where* $\sum |V(C_i)| = N, \forall C_i \in \Delta$*. The RRV corresponding to* Δ *is routable on the SSB* $M_{N,2}$.

For example, in Figure 11, the corresponding RRVs of DRRCSs $\{< v_1, v_3, v_4 >, < v_2, v_5 >\}$, and $\{< v_2, v_3, v_4, v_5 >\}$ are both routable on an SSB $M_{5,2}$.

3.2.2 Proof of Universality

Before proving the universality of generic SSBs, we first consider the universality of SSBs of size one and that of size two. Based on the definition of SSBs and Lemma 5, we have the following lemmas.

Lemma 6 *The* N*-sided SSBs of size one are universal.*

Lemma 7 *The* N*-sided SSBs of size two are universal.*

Based on Lemmas 6 and 7 and the decomposition property of SSBs, we have the following theorem by induction.

Theorem 1 *The N-sided SSBs of size W are universal.*

We have shown the universality of our generic symmetric switch blocks in Theorem 1, i.e., our generic symmetric switch blocks provide the maximum routing capacity. Next we shall show that our generic SSBs use the minimum number of switches. We have the following theorem.

Theorem 2 *No NSB of size W with less than $\binom{N}{2}W$ switches can be universal.*

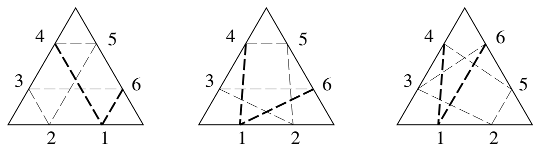
As mentioned in Subsection 3.1, the total number of switches used in an N-sided SSB of size W is $\binom{N}{2}W$. Thus, our SSBs are the "cheapest" universal ones, i.e., it uses the minimum number of switches to provide the maximum routing capacity. Note that the $\binom{N}{2}W$ requirement is quite small, compared to a fully connected switch block which has $\binom{N}{2}W^2$ switches.

3.3 Isomorphism of Switch Blocks

In order to identify, not only a single, but also a whole class of universal switch blocks, we apply the terminology *isomorphism* used in [2]. Here gives its definition.

Definition 3 *Two NSBs $M_{N,W}(T,S)$ and $M'_{N,W}(T',S')$ are isomorphic if there exists a bijection $f\colon\ T \rightarrow T'$ such that $(t_{m,n}, t_{u,v}) \in S$ iff $(f(t_{m,n}), f(t_{u,v})) \in S'$, and for any two terminals $t_{m,n}, t_{u,v} \in T_p$ iff $f(t_{m,n}), f(t_{u,v}) \in T_q$, where $p, q = 1, 2, \ldots, N$.*

In other words, $M_{N,W}(T,S)$ and $M'_{N,W}(T',S')$ are isomorphic if we can relabel the terminals of M to be the terminals of M', maintaining the corresponding switches in M and M'; and for terminals on the same side of M, their corresponding terminals are also on the same side of M'. Figure 12 shows three 3-sided isomorphic switch blocks on which their corresponding terminals are indicated by the same number. For any two isomorphic switch blocks, we have the following theorem.



(a) (b) (c)

Figure 12: (a) A 3-sided SSB. (b–c) Two 3-sided isomorphic switch blocks of (a).

Theorem 3 *Any two isomorphic switch blocks have the same routing capacity.*

Corollary 3.1 *For any two isomorphic switch blocks $M_{N,W}$ and $M'_{N,W}$, $M_{N,W}$ is universal iff $M'_{N,W}$ is universal.*

By Corollary 3.1, we can obtain a whole class of universal switch blocks by performing isomorphism operations on an SSB.

4 Experiments and Results

In our experiments, we implemented a maze router on 4-HFPGAs to explore the effects of switch-block architectures on routing. The router was written in the C language and ran on a SUN Ultra workstation.

We generated connections with lengths based on the *geometric distribution function* because it closely relates to most industrial circuit configurations (e.g., the benchmark circuits in [7, 8, 9]). (Note that no industrial benchmarks for HFPGAs are available.) The geometric distribution function is given as follows:

$$P(p,k) = p(1-p)^{k-1}, \qquad 0 \le p \le 1, \quad k = 1, 2, \ldots,$$

where k is related to connection length and p is a user specified parameter. In the experiments, we randomly generated a set of benchmark circuits with several distinct numbers of connections (from 300 to 800) on a three-level 4-HFPGA (64 logic blocks) based on the geometric distribution function with p = 1.0, 0.9, 0.8, and 0.7. The 5-sided switch blocks used in the experiments were the universal and the clique-based (Xilinx-like) ones with the same number of switches. We assume that all pins of a logic block can be connected to any terminals on the adjacent side of the switch block, and each terminal on a switch block connects to only one terminal on the adjacent side of another switch block.

The quality of a switch block was evaluated by the area performance of the detailed router. We determined the minimum number of tracks (W) required for 100% routing completion for each circuit, using the two kinds of switch blocks. Because net ordering often affects the performance of a maze router, we routed the benchmark circuits by using the following three net-ordering schemes to avoid possible biases: (1) original net order in the benchmark circuits, (2) longest net first, and (3) shortest net first. Also, since our main goal is to make fair comparisons for various switch-block architectures, no rip-up and reroute phase was incorporated in the maze router.

The experimental results are shown in Table 1, where the numbers 300, 400, . . ., 800 indicate the numbers of connections in benchmark circuits. The results show that our universal switch blocks usually outperform the clique-based (Xilinx-like) ones in the chip-level area performance.

5 Conclusions

We have proposed algorithms to construct a class of generic universal switch blocks. Our universal switch blocks not only have the maximum routing capacities but also use the minimum numbers of switches. Further, the decomposition property of a universal switch block provides a key insight into its layout implementation with a smaller silicon area. Experimental results show that our universal switch blocks usually outperform the clique-based (Xilinx-like) ones in the chip-level area performance.

p	net ord.	SW	minimum number of tracks for 100% routing						
			300	400	500	600	700	800	sum
1.0	-	U	19	23	29	34	34	37	176
	-	C	20	25	31	35	37	38	186
0.9	O	U	21	23	27	32	38	41	182
		C	21	25	27	34	40	43	190
	L	U	20	23	27	34	39	42	185
		C	20	24	28	34	41	44	191
	S	U	20	22	27	31	38	42	180
		C	21	23	27	33	41	42	187
0.8	O	U	21	24	30	33	38	38	184
		C	22	24	32	36	39	42	195
	L	U	21	24	29	32	36	40	182
		C	23	26	30	34	40	42	195
	S	U	26	28	31	39	41	47	212
		C	27	30	33	42	43	49	224
0.7	O	U	20	24	28	33	38	43	186
		C	22	24	31	37	39	46	199
	L	U	20	22	29	32	37	43	183
		C	21	24	31	36	39	46	197
	S	U	26	31	39	44	50	>50	>240
		C	26	31	40	49	>50	>50	>245

Table 1: Minimum number of tracks needed for routing completion.

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