RLC COUPLING-AWARE SIMULATION FOR ON-CHIP BUSES AND THEIR ENCODING FOR DELAY REDUCTION

Shang-Wei Tu
Dept. of EE
National Chiao Tung University,
Hsinchu, Taiwan, R.O.C.
kuma@athena.ee.nctu.edu.tw

Jing-Yang Jou
Dept. of EE
National Chiao Tung University,
Hsinchu, Taiwan, R.O.C.
jyjou@faculty.nctu.edu.tw

Yao-Wen Chang,
Dept. of EE
National Taiwan University,
Taipei, Taiwan, R.O.C.
ywchang@cis.nctu.edu.tw

ABSTRACT

Inductance effects of on-chip interconnects have become more and more significant in today's high-speed digital circuits, especially for global interconnects such as signal buses. However, most existing works consider only RC effects, e.g., the worst-case switching pattern resulting from coupling capacitance, to develop their encoding schemes to reduce bus delay. In this paper, we first show that the worst-case switching patterns that incur the largest bus delay are quite different while considering RC and RLC effects. The finding implies that existing encoding schemes based on the RC model might not improve or even worsen the bus delay when inductance effects become dominant. We then propose a bus-invert method to reduce the worst-case on-chip bus delay with the dominance of the inductance coupling effect. Simulation results show that our encoding method can significantly reduce the worst coupling delay of a bus.

1. INTRODUCTION

The trend of technology scaling (shrinking feature sizes) and the increase of clock frequencies are predicted to continue. With aggressive scaling of transistor gate lengths, interconnect delay increasingly dominates chip performance in deep-submicron designs [15, 17]. Further technology scaling in deep-submicron indicates that interconnect delay will continue to dominate overall chip performance. Therefore, it is crucial to optimize or reduce interconnect delay and noise for improving circuit performance.

As the process technology advances and the clock frequency increases over GHz, the inductance effects of on-chip interconnect structures have become increasingly significant [15]. Further, the use of new dielectric materials (ultra-low-k or extreme low-k materials [15]) and the continuing increase of clock frequencies will cause inductance effects much worse than capacitance effects in the near future.

On-chip inductance effects in high-performance circuit designs might impact interconnect in many ways. The performance of a circuit will be reduced due to the increase of wire delay [4, 10]. The long-range inductive crosstalk can cause serious signal integrity related problems [7, 10]. Signal overshoots and undershoots due to wire inductance may damage devices. Finally, inductance in power and ground grids can increase the noise in the supply and ground voltages when large currents flow. This is also known as the *ground-bounce* problem. Therefore, inductance effects cannot be neglected in today's high-performance circuit designs, especially for global interconnects such as clock wires and signal buses.

Most existing works focus on reducing the effects resulting from coupling capacitance on the bus structure. There is not much work in the literature considering inductance effects on the bus structure to develop encoding schemes to reduce bus delay. Victor and Keutzer proposed some data encoding techniques (*unpruned code with memory, pruned code with memory,* and *memoryless code*) to eliminate crosstalk delay due to capacitive coupling [18]. Baek et al. [1] proposed a bus encoding scheme called *LESS (low energy set scheme)* to minimize the coupling capacitance effects. Considering coupling *RC* effects, Hirose and Yasurra [9] proposed a bus delay reduction technique by intentionally skewing signal transition timing of adjacent wires. Based on an RC model, Sotiriadis and Chandrakasan considered coupling effects and developed an encoding scheme [16].

Since most of previous works consider only capacitance effects on the bus structure to reduce delay, the worst-case switching pattern which incurs the largest delay is when adjacent wires simultaneously switch in opposite transition directions. However, considering the *RLC* circuit model for the bus structure, we find that the worst-case switching pattern with the largest on-chip bus delay is when all wires simultaneously switch in the same direction. In contrast, this worst-case pattern is the best-case pattern of a coupling *RC* model. Further, the best-case switching pattern with the *RLC* model is that the central wire of the bus switches in a different direction from all other wires that all switch in the same direction. However, this best-case pattern is just the worst-case pattern with the *RC* model. See **Figure 1** for examples of the worst- and the best-case switching patterns on a 5-bit bus. Hence, as inductance cannot be neglected in today's high-performance circuit design, it is very important to consider *RLC* effects to develop the encoding schemes to reduce bus delay.
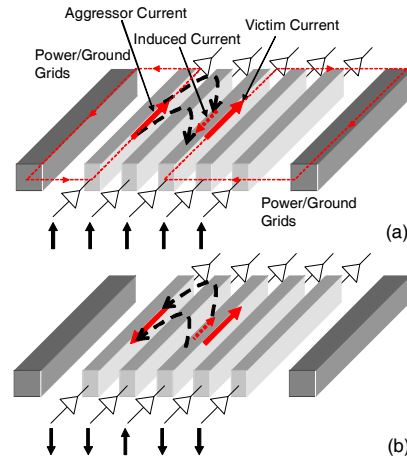

Figure 1: An *LC* cross-coupled 5-bit bus structure. (a) The switching pattern of the worst-case delay in the RLC model. (b) The switching pattern of the best-case delay in the RLC model. (↑: switch from "0" to "1". ↓: switch from "1" to "0".)

With the findings of the best- and worst-case patterns, we propose a new encoding scheme for on-chip buses to minimize coupling delay with the dominance of inductance effects. The key idea is that inductance coupling effects should be alleviated by transforming the data sequences transmitting through on-chip buses. However, the architectures of the encoder and decoder should be of low complexity so that the power and delay overheads due to the codec circuitry can be compensated by the significant reduction of bus delay.

The rest of this paper is organized as follows. Section 2 first describes the parameters and the assumptions used in our study for the bus structure and then gives the working flow. Section 3 gives simulations by using the *RLC* model. The method and circuitry of our encoding (decoding) scheme is described in Section 4, and simulation results are shown in Section 5. Finally, Section 6 concludes the paper and discusses our future work.

2. PRELIMINARY

In this work, we used the bus structure shown in **Figure 1** to conduct our simulations. We assume that all drivers (receivers) have a uniform size and all signal wires have a uniform width, spacing, and length. The length, width, and pitch of the signal wire were 2000μm, 0.8μm, and 2μm, respectively. The respective width and pitch of the power/ground

were 2μm and 13μm. The heights of all wires are set to 2μm. The signal rise/fall time was set to 100ps. With these feasible parameters [5, 6, 15], we used the famous 3D field-solver FastCap [13] to extract the self and coupling capacitance and FastHenry [11] to extract the resistance, self inductance, and coupling inductance. Then with these extracted *RLC* parameters, we constructed the coupling *RLC* and *RC* circuit models. Both circuit models were constructed as π-segments using series resistance (or series resistance and inductance for *RL*) and shunt capacitance. Finally, the circuits were simulated by using HSPICE. The overall flowchart is illustrated in **Figure 2**. In our simulations, we assumed that synchronous latches are located at the transmitter side. Thus all the signals switch at the same time on the buses, which is a very common assumption for buses [12].
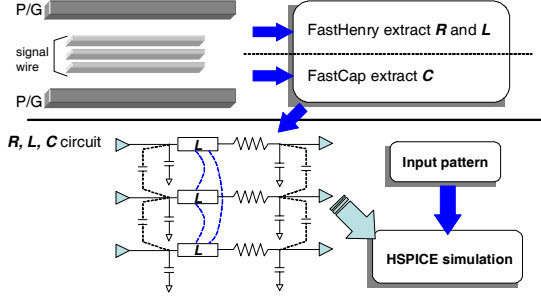

Figure 2: Working flow.

Unlike [8] which assumes that aggressors can switch at arbitrary moments and victims are quiet, we assume that all signal wires only switch at the same time and may have arbitrary switching patterns, i.e., switching high or switching low. In addition, [8] tries to find the switching pattern and switching time resulting in the worst-case noise (*WCN*) defined as the maximum crosstalk noise peak on a quiet victim net. However, our work tries to find the simultaneously switching pattern that causes the maximum transition delay on a switching victim. Therefore, our wok is significantly different from [8].

3. SIMULATIONS WITH THE *RLC* CIRCUIT MODEL

Table 1: Simulation results of a 5-bit bus considering *RLC* effects. (V$_{dd}$ = 1.2V)

Switching pattern	50% delay of the central wire (ps)	Delay comparison with that of 00↑00	Max swing (V)	Noise (% of Vdd)
↑↑↑↑↑	97	51.56%	1.71	42.50%
↑↓↑↑↑	88	37.50%	1.47	22.50%
↑↓↑↑↓	63	-1.56%	1.31	9.20%
↑↓↑↓↑	75	17.19%	1.17	-2.50%
↑↓↑↓↓	51	-20.31%	1.04	-13.33%
↓↑↑↑↑	78	21.88%	1.56	30.00%
↓↑↑↑↓	55	-14.06%	1.4	16.67%
↓↑↑↓↓	45	-29.69%	1.13	-5.83%
↓↓↑↑↑	66	3.13%	1.33	10.83%
↓↓↑↓↓	37	-42.19%	0.903	-24.75%
00↑00	64	0.00%	1.31	9.17%

In this section, we first simulate all switching patterns on the 5-bit bus structure considering the *RLC* effects of bus interconnects, and then increase wire capacitance to see whether the worst-case switching pattern will change or not as the wire capacitance becomes dominant. The simulation results of the extracted *RLC* circuit model for the 5-bit bus are shown in **Table 1**. From **Table 1**, we observe that the worst-case switching pattern changes from *↓↑↓* (for the *RC* circuit model) to ↑↑↑↑↑ and the best-case switching pattern changes from *↑↑↑* (for the *RC* circuit model) to ↓↓↑↓↓. Therefore, the worst-case and best-case switching patterns are completely different considering *RC* and *RLC* effects. Therefore, as the process technology keeps shrinking and the clock frequency continues increasing, it is very important to consider *RLC* effects on the bus structure to derive encoding schemes to reduce bus delay. Otherwise, the encoding schemes might not improve or even worsen the on-chip bus delay because of the redundant logics and wires.

Further, we also observe that the largest overshoot noise occurs for the pattern ↑↑↑↑↑, as shown in **Table 1**.

Why does the worst-case switching pattern ↑↑↑↑↑ result in the largest bus delay when considering *RLC* effects on the 5-bit bus. Theoretically speaking, this is mainly due to the two factors: (1) Inductance becomes dominant due to higher frequency and longer interconnects. Since the *significant frequency f$_s$* [3] is defined as *f$_s$= 0.35/t$_r$* where *t$_r$* is the signal transition time. Hence, the frequency of interest is 3.5 GHz as the rise time is set to 100 ps. Therefore, for the simulations when the wire length is 2000 μm and the frequency is 3.5 GHz, the inductance effects are much more significant than the capacitance effects. (2) It is also due to the long-range effect of inductance. From *Faraday's Law* [2], as shown in Equation (1), the electromotive force induced in a closed circuit is equal to the negative rate of increase of the magnetic flux linking the circuit. We have

$$V_j = -\frac{d\Phi_{ij}}{dt} \text{ with } \Phi_{ij} = \int_{S_j} \vec{B}_i \cdot d\vec{s}_j \tag{1}$$

where V_j is the electromotive force induced in circuit loop j due to the time-varying current I_i in circuit loop i. Here, Φ_{ij} is the magnetic flux in loop j due to the current I_i in loop i, $\vec{B}_i$ is the magnetic flux density arising from current I_i in loop i, and S_j represents the surface bounded by the loop j. The orientation of $\vec{B}_i$ can be determined from the *right-hand rule*. Therefore, as shown in **Figure 1(a)**, the increasing current of the leftmost aggressor wire will induce a downward increasing magnetic field on the victim wire. For simplicity, the aggressor and the victim loops are also shown in **Figure 1(a)** (dotted loops). Therefore, the mutual flux *Φ* is positive and also increases with time because of the same direction of the resulting magnetic flux density $\vec{B}$ and the victim loop $\vec{s}$; in other words, $\vec{B} \cdot d\vec{s}$ is also positive. In conclusion, from Equation (1), the induced voltage on victim loop is negative; that is, the induced current on the victim wire flows in the reverse direction of the victim current. Hence, while all neighboring wires simultaneously switch in the same direction as the victim wire does, they will all induce a current of the different direction on the victim wire as shown in **Figure 1(a)**. Therefore, the charge current of the victim wire will be reduced. This implies that the charging time (delay) will increase due to the long-range coupling. We can conclude that as the inductance of wires becomes more significant than the capacitance, the worst-case switching pattern with the maximum delay is when all wires simultaneously switch in the same direction. Meanwhile, these patterns will also result in the largest noise between each other.

4. THE BUS-INVERT SCHEME

Inspired by Stan's low-power *bus-invert* method [14] for reducing the transition activities to reduce the bus transition power, we propose a *bus-invert* method to reduce the on-chip bus delay due to coupling effects while inductance effects dominate. Our bus-invert method inverts the input data when the number of bits switching in the same direction is more than half of the number of signal bits. The remaining problem is how to implement the coding architecture with low complexity. For the implementation, we propose an encoder architecture shown in **Figure 3**.

There are three types of possible signal transitions: type I: ↑ (switching from "0" to "1"), type II: ↓ (switching from "1" to "0"), and type III: 0 (no switching). If we refer to $x_i(n)$ as an input signal and to $x_i(n-1)$ as its previous input signal, then type I is $(x_i(n), x_i(n-1)) = (1, 0)$, type II is $(x_i(n), x_i(n-1)) = (0, 1)$, and type III is $(x_i(n), x_i(n-1)) = (0, 0)$ or $(1, 1)$. With the input $x_i(n)$ and $x_i(n-1)$, the codeword generator generates $(q_L, q_H) = (0, 1)$ for type I, $(1, 0)$ for type II, and $(0, 0)$ for type III. Then all q_L's are inputs to the majority voter (L) and all q_H's to the majority voter (H). Finally, from the output of the majority voter L or H, we can detect if the number of type I or II transitions is more than half of the number of signal bits. If one of the majority voters' outputs is high, the input signal should be inverted. The majority voters can be implemented by using either a tree of full-adders or resistors combined with a voltage comparator [14].
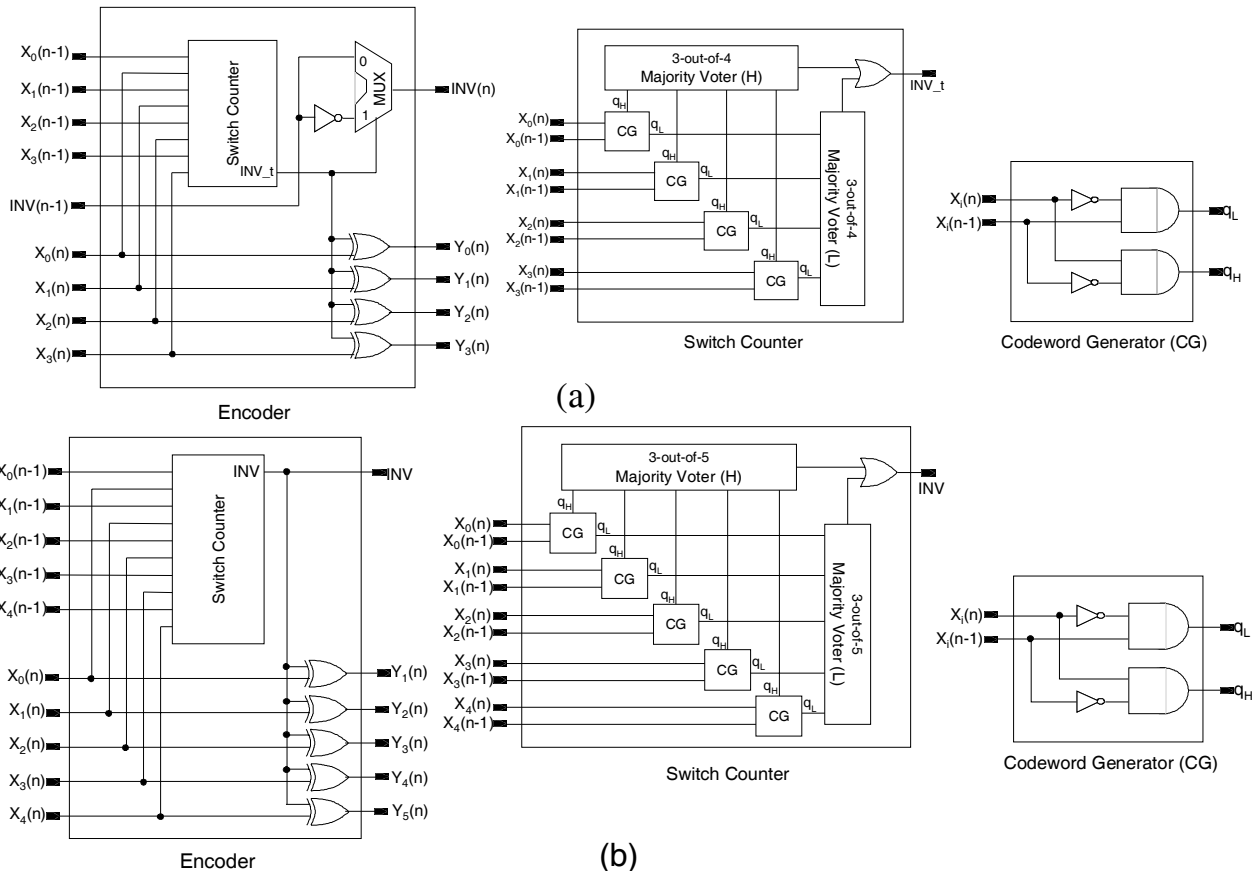
Figure 3: (a) A 4-bit bus encoder for the *bus-invert* scheme. (b) A 5-bit bus encoder for the *bus-invert* scheme.

Since the additional *invert* line will contribute to transitions, it should also be considered. Let N be the total number of signal bits of a bus excluding the *invert* line. The output of the majority voter is asserted when $\lceil (N+1)/2 \rceil$ inputs are high. If N is odd, the example encoder architecture is just as that shown in **Figure 3(b)**. Hence, after encoding, the worst-case switching pattern occurs when $(N+1)/2$ signal bits switching in the same direction, where N is odd. If N is even, the encoder architecture is somewhat different as that shown in **Figure 3(a)**. The major differences are that we need an extra input $INV(n\text{-}1)$ for our encoder and $INV(n) = INV(n\text{-}1)$' or $INV(n\text{-}1)$ depending on if INV_t is high or low. Hence, after encoding, the worst-case switching pattern is that $N/2$ signal bits switch in the same direction, where N is even.

The circuitry of the receiver is relatively simple because it only needs to conditionally invert the receiving data to get a correct data value. If N is odd, the receiving data need to be inverted only when the *invert* line is high. If N is even, the receiving data need to be inverted only when the *invert* line has a transition.

5. SIMULATION RESULTS

With the parameters given in Section 2, we conducted our simulations by varying bus signal bits with or without using the proposed *bus-invert* method. The simulation results are shown in **Figures 4** and **5**.

From **Figure 4**, we observe that coupling inductance has greater impacts on bus delay as the number of bus bit lines increases. For a tight *LC* cross-coupled bus, as shown in **Figure 4**, the increase (%) of the worst-case switching delay grows about linearly with the number of bus bit lines. Hence, for a high-frequency, tight *LC* cross-coupled bus, the delay due to signals simultaneously switching in the same direction should be considered.

As shown in **Figure 5**, our encoding method can significantly reduce the worst-case switching delay. Besides, our encoding method can obtain an even better reduction rate as the number of bus bit lines increases. We also compare our method with the conventional shield insertion technique

which inserts one shielding wire in the middle of the bus. As Shown in **Figure 5**, our method outperforms the conventional shield insertion technique when the number of bus bit lines is greater than 4. However, since the encoder architectures for even-bit and odd-bit buses are slightly different, the delay reductions are also slightly different. For an N-bit bus, if N is odd, the worst-case switching pattern after encoding is $(N+1)/2$ signal bits (including the INV line) switching in the same direction. For N is even, the worst-case pattern after encoding is that only $N/2$ signal bits (including the INV line) switch in the same direction. Hence, the reduction of worst-case delay for even-bit buses is more significant than that of odd-bit buses when the number of bits is larger than 5 (see **Figure 5**). We should also note that for the 2-bit bus, our encoding method will worsen the worst-case delay because the additional INV line will introduce large additional coupling to the victim line. In other words, the worst-case delay after encoding for 2 bit lines plus one INV line will be larger than that for 2 bit lines alone.
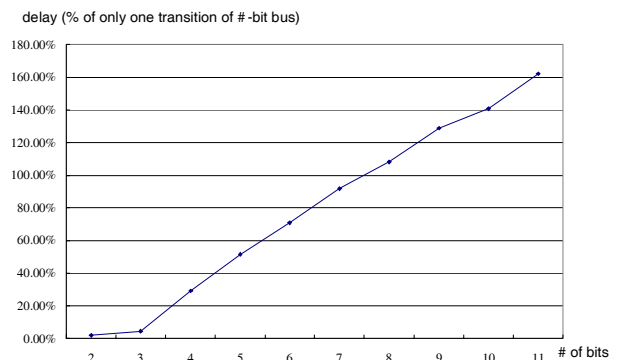

delay (% of only one transition of #-bit bus)

Figure 4: The worst-case #-bit bus delay (% of the delay of only one transition pattern of the #-bit bus) with # varying from 2 to 11.
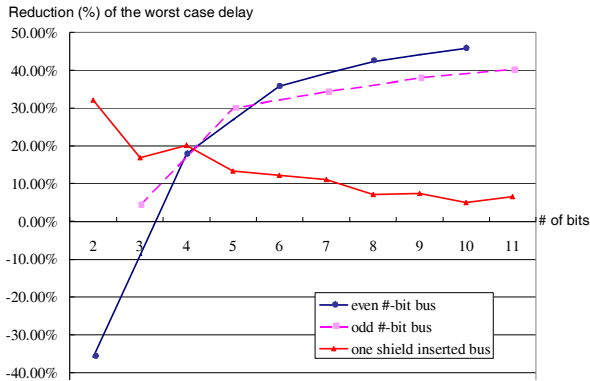
Reduction (%) of the worst case delay

Figure 5: The reduction of worst-case delay for a #-bit bus by using the *bus-invert* method and the shield insertion technique with the # varying from 2 to 11.

Although our bus-invert method is mainly intended for delay reduction, it is also effective for inductive noise reduction. As shown in **Table 2**, the average reduction of maximum noise is about 17%, which is about the same as the well-known shield insertion technique. Further, our method has the side effects of reducing ground-bounce noise (not included in **Table 2**) because the worst-case ground-bounce noise occur when all signal wires switch in the same direction (large charging or discharging current changes)---our method can avoid such a worst-case configuration while the shield insertion technique cannot.

Table 2: Reduction of worst-case noise by using the bus-invert method and one shield insertion for bus widths ranging from 2 to 11.

#-bit bus	Max swing (V)	Max swing after one shield insertion (V)	Noise reduction (%)	Max swing after encoding (V)	Noise reduction (%)
2	1.59	1.24	22.01%	1.33	19.55%
3	1.63	1.35	17.18%	1.44	13.19%
4	1.67	1.35	19.16%	1.41	18.44%
5	1.71	1.41	17.54%	1.47	16.33%
6	1.72	1.42	17.44%	1.47	17.01%
7	1.74	1.44	17.24%	1.49	16.78%
8	1.74	1.48	14.94%	1.46	19.18%
9	1.76	1.45	17.61%	1.51	16.56%
10	1.75	1.52	13.14%	1.49	17.45%
11	1.76	1.49	15.34%	1.52	15.79%
Average noise reduction			17.16%		17.03%

Since previous works of encoding for bus delay reduction such as [1, 17, 20] only consider coupling capacitance, the real worst-case pattern due to coupling *LC* might happen with their encoding. Besides, they might use more than one additional line in their encoding scheme when the number of bit lines is more than 8. Therefore, their encoding schemes might not be suitable for the high-performance bus applications when inductance effects become significant.

6. CONCLUSION & DISCUSSIONS

In this paper, we have shown that the inductance effects have changed the worst-case switching pattern with the maximum bus delay. For a 5-bit bus structure, the worst-case switching pattern is *↓↑↓* or *↑↓↑* considering *RC* effects, but the worst-case pattern changes to ↑↑↑↑↑ or ↓↓↓↓↓ considering *RLC* effects. Hence, we shall consider both the *RC* and the *RLC* effects to derive effective encoding schemes for bus delay optimization.

We have also conducted simulations considering *RLC* effects on the bus structure when wire capacitance becomes dominant. We have observed that the worst-case switching pattern is also different from the one considering *RC* effects. The difference is due to long-range inductive coupling.

We have also proposed a *bus-invert* method to reduce the worst-case on-chip bus delay with the dominance of inductance coupling effect. Simulation results have shown that our encoding method can significantly

reduce the worst coupling delay of a bus. In the future, we intend to develop a more sophisticated bus-invert scheme to further reduce the inductive coupling delay.

Our encoding scheme is recommended for the cases when buses or parallel signal wires are about thousands of μm long and work above GHz frequencies. At such working frequencies, the gate delay overhead of our encoder should be small enough. If we choose the full-adder tree to implement the majority voter, the delay of majority voter is $O(log_3 N)*(full\text{-}adder\ delay)$, where N is the total number of signal bits of a bus. In other words, if N is very large, our encoder may cause timing violations. To solve this problem, we can divide the original bus into sub-buses by inserting ground wires between sub-buses. Hence, the overall problem is a gate delay (and thus process) dependent optimization problem. Therefore, we shall solve this problem in our future work.

7. REFERENCES

[1] K. H. Baek, K. W. Kim, and S. M. Kang, "A Low Energy Encoding Technique for Reduction of Coupling Effects in SOC Interconnects," *Proc. 43rd IEEE Midwest Symp. Circuits Syst.*, pp. 80-83, 2000.

[2] D. K. Cheng, *Field and Wave Electromagnetics*, 2nd Ed., Addison-Wesley, 1989.

[3] C. K. Cheng, J. Lillis, S. Lin, and N. Chang, *Interconnect Analysis and Synthesis*, John Wiley & Sons, Inc., 2000.

[4] M. H. Chowdhury, Y. I. Ismail, C. V. Kashyap, and B. L. Krauter, "Performance Analysis of Deep Sub micron VLSI Circuits in the Presence of Self and Mutual Inductance," *IEEE Int. Symp. Circuits Syst.*, pp. 197-200, 2002.

[5] M. A. Elgamel and M. A. Bayoumi, "Interconnect Noise Analysis and Optimization in Deep Submicron Technology," *IEEE Circuits Syst. Magazine*, pp. 6-17, 2003.

[6] R. Escovar and R. Suaya, "Optimal Design of Clock Trees for Multigigahertz Applications," *IEEE Trans. Computer-Aided Design of Integrated Circuits Syst.*, pp. 329-345, 2004.

[7] L. He and K. M. Lepak, "Simultaneous Shield Insertion and Net ordering for Capacitive and Inductive Coupling Minimization," *Int. Symp. Physical Design*, pp. 55−60, 2000.

[8] J. Chen and L. He, " Determination of Worst-Case Crosstalk Noise for Non-Switching Victims in GHz+ Interconnects," *Proc. Asia and South Pacific Design Automation Conf.*, pp. 162-167, 2003.

[9] K. Hirose and H. Yasuura, "A Bus Delay Reduction Technique Considering Crosstalk," *Proc. Design, Automation and Test in Europe Conf. and Exhib.*, pp. 441-445, 2000.

[10] Y. I. Ismail, "On-Chip Inductance Cons and Pros," *IEEE Trans. VLSI Syst.*, pp. 685-694, 2002.

[11] M. Kamon, M. J. Tsuk, and J. K. White, "FastHenry: a Multipole-accelerated 3D Inductance Extraction Program," *IEEE Trans. Computer-Aided Design*, pp. 1750−1758, 1994.

[12] H. Kriplani, F. N. Najm, and I. N. Hajj, "Pattern Independent Maximum Current Estimation in Power and Ground Buses of CMOS VLSI Circuits: Algorithms, Signal Correlations, and Their Resolution," *IEEE Trans. Computer-Aided Design of Integrated Circuits Syst.*, pp. 998-1012, 1995.

[13] K. Nabors and J. White, "FastCap: A Multipole Accelerated 3-D capacitance extraction program," *IEEE Trans. Computer-Aided Design*, pp. 1447-1459, 1991.

[14] M. R. Stan and W. P. Burleson, "Bus-Invert Coding for Low-Power I/O," *IEEE Trans. VLSI Syst.,* vol. 3, Mar. 1995.

[15] Semiconductor Industry Association, *International Technology Roadmap for Semiconductors*, 2003.

[16] P. P. Sotiriadis and A. P. Chandrakasan, "Reducing Bus Delay in Submicron Technology Using Coding," *Proc. Asia and South Pacific Design Automation Conf.*, pp. 109-114, 2001.

[17] L. Trevillyan, D. Kung, R. Puri, L. N. Reddy, and M. A. Kazda, "An Integrated Environment for Technology Closure of Deep-Submicron IC Designs," *IEEE Design and Test of Comput.*, pp. 14-22, 2004.

[18] B. Victor and K. Keutzer, "Bus Encoding to Prevent Crosstalk Delay," *Int. Conf. Computer-Aided Design*, pp. 57-63, 2001.