Generic Universal Switch Blocks

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Abstract—A switch block M with W terminals on each side is said to be *universal* if every set of nets satisfying the dimension constraint (i.e., the number of nets on each side of M is at most W) is simultaneously routable through M [2]. In this paper, we present an algorithm to construct N-sided universal switch blocks with W terminals on each side. Each of our universal switch blocks has $\binom{N}{2}W$ switches and *switch-block flexibility* $N-1$ (i.e., $F_S = N-1$). We prove that no switch block with less than $\binom{N}{2}W$ switches can be universal. We also compare our universal switch blocks with others of the topology associated with Xilinx XC4000-type FPGAs. To explore the area performance of the universal switch blocks, we develop a detailed router for hierarchical FPGAs (HFPGAs) with 5-sided switch blocks. Experimental results demonstrate that our universal switch blocks improve routability at the chip level. Based on extensive experiments, we also provide key insights into the interactions between switch-block architectures and routing.

Index Terms—Analysis, architecture, design, digital, gate array, programmable logic array.

1 Introduction

A conventional FPGA (see Fig. 1a) consists of an array of logic blocks that can be connected by routing resources [1]. The logic blocks contain combinational and sequential circuits which are used to implement logic functions. The routing resources consist of wire segments and switch blocks. The intersection of a horizontal and a vertical channel is referred to as a switch block; the switch block serves to connect wire segments and this requires using programmable switches inside it. Fig. 1b illustrates a switch block in which the programmable switches, denoted by dashed lines between terminals, are shown.

The studies by [5], [12] have proposed a new routing architecture called an *8-way mesh*. (See Fig. 2a for the architecture.) Similar to a conventional architecture, an 8-way mesh structure also consists of a two-dimensional array of logic blocks. However, unlike the conventional architecture, the pins of a logic block in an 8-way mesh are directly connected to their nearest four switch blocks in diagonal directions. A switch block used in the 8-way mesh is then not only connected by its four nearest neighboring switch blocks, but also by the four diagonal neighboring logic blocks. Thus, the switch blocks used in 8-way mesh FPGAs are 8-sided. (See Fig. 2b for an 8-sided switch block.) A topology of the architecture similar to the 8-way mesh architecture for interchip routing was also studied in [4].

A *hierarchical FPGA* (*HFPGA*) (see Fig. 3a and Fig. 3c) has a hierarchical interconnection structure [6], [3], [8]. An HFPGA can be hierarchically constructed by connecting logic blocks into clusters. First, k logic blocks are connected with a switch block. This step forms a one-level HFPGA. Then, k clusters are recursively connected together as a *supercluster*. As k clusters are connected into a supercluster, the number of levels of the hierarchy will be increased by one. It is called a *k-HFPGA* if a cluster has k subclusters [8]. For example, Fig. 3a is a four-level 2-HFPGA and Fig. 3c is a two-level 4-HFPGA.

In an HFPGA, the switch blocks are not the same as the conventional 4-sided switch blocks. For a k-HFPGA, each switch block, except the top-level one, is connected with k logic blocks and another switch block; therefore, the switch block can be considered a $(k+1)$-sided polygonal block. For example, the switch block of 2-HFPGA is 3-sided (see Fig. 3b) and the switch block of 4-HFPGA is 5-sided (see Fig. 3d). Therefore, switch blocks could have arbitrary numbers of sides and it is significant to consider the design and analysis of switch blocks with multiple sides.

For the work on conventional switch blocks (4-sided blocks), Rose and Brown in [10] defined the flexibility of a switch block, represented by F_S, as the number of programing switches between a terminal and others. They investigated the effects of different switch-block flexibilities on routing and suggested that $F_S = 3$ should often be sufficient for high routability. Chang et al. first presented a class of universal switch blocks in [2]. A switch block M with W terminals on each side is said to be *universal* if every set of nets satisfying the dimension constraint (i.e., the number of nets on each side of M is at most W) is simultaneously routable through M [2]. They proved that each of the universal switch blocks can accommodate significantly more routing instances than the Xilinx XC4000-type one of the same size. Recently, a report on the layout implementations of the universal switch blocks and the XC4000-type ones has also concluded that the universal switch blocks need smaller silicon areas—the *decomposition property*[1] of the universal switch blocks makes their layout very regular and compact [14].

In this paper, we present an algorithm to construct generic universal switch blocks with multiple sides. Each of our universal switch blocks has $\binom{N}{2}W$ switches and *switch-block flexibility* $N-1$ (i.e., $F_S = N-1$). We prove that no switch block with less than $\binom{N}{2}W$ switches can be universal.

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1. A formal definition of the decomposition property will be given in Section 3.1.

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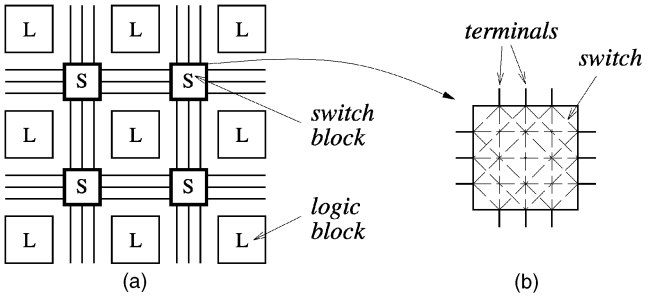

Fig. 1. A conventional FPGA and its switch block. (a) A conventional FPGA architecture. (b) A conventional 4-sided switch block.

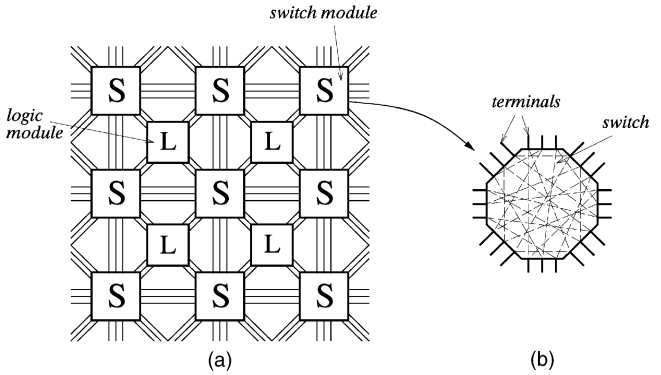

Fig. 2. An 8-way mesh FPGA and its switch block. (a) The architecture of an 8-way mesh. (b) The switch block used in (a).

We also compare our universal switch blocks with others of the topology associated with Xilinx XC4000-type FPGAs. To explore the area performance of the universal switch blocks, we develop a detailed router for 4-HFPGA. We model an HFPGA as a graph and apply a graph-search technique to HFPGA routing. Experimental results demonstrate that our universal switch blocks improve routability at the chip level. Based on extensive experiments, we also provide key insights into the interactions between switch-block architectures and routing.

The remainder of this article is organized as follows: Section 2 introduces some notation and definitions. Section 3 proposes an algorithm to construct generic universal switch blocks with multiple sides. Section 4 presents a graph modeling of HFPGAs and a graph-search technique for HFPGA routing. Section 5 shows our experimental results and discusses the interactions between the universal switch-block architectures and routing.

2 Preliminaries

An *NSB* is an N-sided switch block with W terminals on each side of the block. We represent an NSB by $M_{N,W}(T,S)$, where T is the set of terminals and S the set of programming switches. Label the terminals

$$t_{1,1}, t_{1,2}, \ldots, t_{1,W}, t_{2,1}, t_{2,2}, \ldots, t_{2,W}, \ldots, t_{N,1}, t_{N,2}, \ldots, t_{N,W},$$

starting from the first terminal on one side and proceeding clockwise. Fig. 4a and Fig. 4b show the examples of $M_{3,3}(T,S)$ and $M_{5,3}(T,S)$, respectively. Let $T_i = \{t_{i,1}, \ldots, t_{i,W}\}$ and $S_i = \{(t_{m,n}, t_{u,v})|$, there exists a programmable switch between terminals $t_{m,n}$ and $t_{u,v}$, $t_{m,n} \in T_i$ or $t_{u,v} \in T_i, m < u\}$ for $1 \le i \le N$. Let $L_{i,W}(T_i, S_i)$ denote the terminals of side i and all switches connected with these terminals. Therefore, $S = \cup_{i=1}^{N} S_i$, $T = \cup_{i=1}^{N} T_i$, and $M_{N,W}(T,S) = \cup_{i=1}^{N} L_{i,W}(T_i, S_i)$. For convenience, we often refer to $M_{N,W}(T,S)$ and $L_{i,W}(T_i,S_i)$ simply as $M_{N,W}$ and $L_{i,W}$, respectively, omitting T and S, if there is no ambiguity about T and S or T and S are not of concern in the context.

In an NSB, the switches are electrically *noninteracting* unless they share a terminal. A *connection* is an electrical path between two terminals (say $t_{m,n}$ and $t_{u,v}$) on different sides of a switch block. If the switch ($t_{m,n}$, $t_{u,v}$) is programmed to be "ON," then a connection between these two terminals is established. Because each connection is characterized by two sides of a block, we can classify all connections passing through a switch block into a number of categories. For an NSB, connections can be of $\binom{N}{2}$ types. Fig. 5a and Fig. 5b show the type definitions of 3-sided and 5-sided switch blocks, respectively.

A *routing requirement vector* (*RRV*) $\vec{n}$ for an NSB is an $\binom{N}{2}$-tuple $(n_{1,2}, n_{1,3}, \ldots, n_{1,N}, n_{2,3}, \ldots, n_{2,N}, \ldots, n_{N-1,N})$, where $n_{i,j}$ is the number of type-(i,j) connections required to be routed through an NSB, $0 \le n_{i,j} \le W$ for $1 \le i < j \le N$. An RRV $\vec{n}$ is said to be *routable* on an NSB $M_{N,W}$ if there exists a routing for $\vec{n}$ on $M_{N,W}$. For example, in a 3-sided switch block, Fig. 6a shows a routing instance with four nets corresponding to the RRV $(1,2,1)$, and Fig. 6b and Fig. 6c show two switch blocks with the same flexibility ($F_S = 2$). The RRV $(1,2,1)$ is routable on the switch block shown in Fig. 6b and a routing solution is illustrated by the thick lines. In Fig. 6c, however, there is always one net that cannot be routed into M_b. Thus, the RRV $(1,2,1)$ is not routable on the switch block shown in Fig. 6c.

The *routing capacity* of a switch block M is referred to as the number of distinct routable vectors on M; that is, the routing capacity of M is the cardinality $|\{\vec{n}|\vec{n} \text{ is routable on } M\}|$. A switch block M with W terminals on each side is called *universal* if every set of nets satisfying the dimension constraint (i.e., the number of nets on each side of M is at most W) is simultaneously routable through M. The dimension constraint can be denoted by an N-tuple $\vec{D}_{N,W} = (W, W, \ldots, W)$. For an RRV $\vec{n}$, its *dimension requirement vector* (*DRV*) $\vec{d}$ is an N-tuple $(d_1, d_2, \ldots, d_N)$ (i.e., the routing requirements on sides $1, 2, \ldots, N$ are $d_1, d_2, \ldots, d_N$, respectively), where $d_i = \sum_{1 \le j \le N} n_{i,j}$ for $1 \le i \le N, n_{i,j} = n_{j,i}$ and $n_{i,i} = 0$.

Note that RRVs and DRVs correspond to different concepts. An RRV, an $\binom{N}{2}$-tuple, is used to characterize nets routed through *a switch block*; however, a DRV, an N-tuple, is used to characterize nets routed through *each side* of a switch block. An RRV $\vec{n}$ satisfies the dimension constraint of size W if its DRV $\vec{d} \le \vec{D}_{N,W}$ (i.e., $d_i \le W$ for $1 \le i \le N$). Let the DRV of an RRV $\vec{n}$ be $\vec{d}$. We have the following definition.

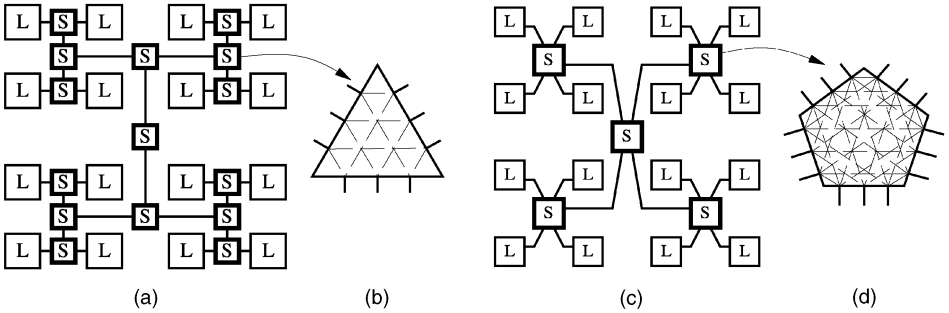

Fig. 3. Two HFPGA architectures. (a) A four-level 2-HFPGA. (b) A 3-sided switch block in the 2-HFPGA. (c) A two-level 4-HFPGA. (d) A 5-sided switch block in the 4-HFPGA.

Definition 1. *A switch block $M_{N,W}$ is called universal if $\vec{d} \leq \vec{D}_{N,W}$ is the necessary and sufficient condition for $\vec{n}$ to be routable on $M_{N,W}$.*

Note that the number of nets routed through each side of a switch block cannot exceed W; therefore, a universal switch block has the maximum routing capacity.

3 Universal Switch Blocks

To identify a universal switch block, we first consider the clique-based one used in the Xilinx XC4000-series FPGAs. Fig. 6c and Fig. 7a and Fig. 7b show three such clique-based switch blocks of three, four, and five sides, respectively. Nevertheless, as shown in Fig. 6c, it is obvious that the clique-based switch blocks are not universal since the RRV $(1, 2, 1)$ which satisfies the dimension constraint is not routable on the 3-sided clique-based switch block of size three.

In the following, we consider a type of switch blocks which can be shown to be universal later.

3.1 Symmetric Switch Blocks

Let N ($N = 2, 3, 4, 5, \ldots$) be the number of sides of a switch block and W the size of the switch block. Algorithm Symmetric_Switch_Block, shown in Fig. 8, constructs a switch block $M_{N,W}$. We refer to the topology of the switch block constructed by the algorithm as the *symmetric topology* and the switch block as the *symmetric switch block*. Fig. 9 shows three examples of symmetric switch blocks. For a symmetric switch block, it has a flexibility (F_S) of $N - 1$; thus, the total number of switches used in the symmetric switch block is $\frac{N \times W \times F_S}{2} = \frac{N(N-1)}{2} W = \binom{N}{2} W$. For example, the total number of switches used by the 3-sided symmetric switch block, the square symmetric switch block, and the 5-sided symmetric switch block are $3W$, $6W$, and $10W$, respectively. Note that the switch block shown in Fig. 9b is a universal switch block proposed in [2].

For the symmetric switch blocks, we have the following properties:

Lemma 1 (Decomposition Property). *A symmetric switch block can be partitioned into $\lfloor W/2 \rfloor$ symmetric subblocks of size two and $(W \bmod 2)$ symmetric subblock(s) of size one.*

Proof. Consider Algorithm Symmetric_Switch_Block(N, W). For each k in line 3, we construct a symmetric subblock of size two in lines 4-6. Therefore, we have $\lfloor W/2 \rfloor$ subblocks of size two after $\lfloor W/2 \rfloor$ iterations (see line 3). Further, all these symmetric switch blocks of size two constructed in lines 4-6 have the same topology. Lines 7-10, just for an odd W, construct a clique of N vertices (i.e., a subblock of size one) from the middle terminal of each side of the switch block. Thus, we have (W mod 2) such subblock of size one (see lines 7-10). □

Lemma 2 (Reduction Property). *$M_{N,W}$ is a symmetric switch block, where $N \geq 3$, so is*

$$M_{N-1,W} = M_{N,W} \setminus L_{i,W}, 1 \leq i \leq N.$$

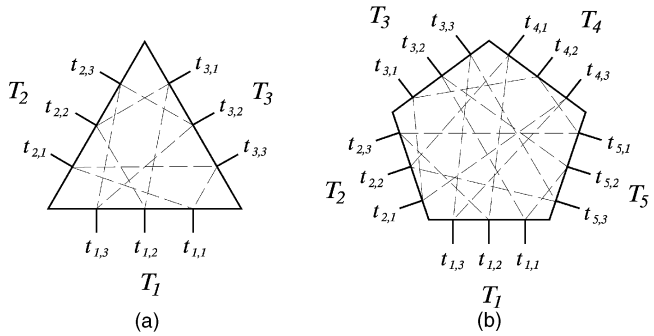

Fig. 4. Two examples of N-sided switch blocks. (a) A 3-sided switch block ($M_{3,3}(T, S)$). (b) A 5-sided switch block ($M_{5,3}(T, S)$).

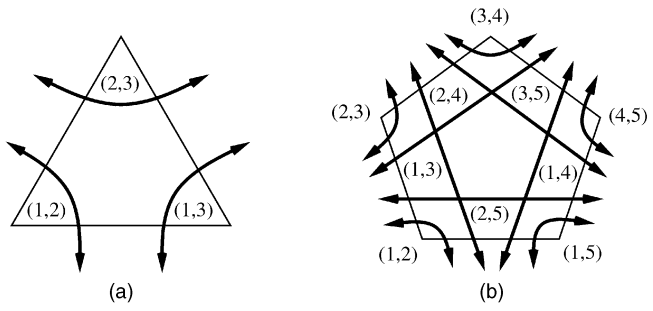

Fig. 5. Examples of types definitions. (a) Three types of connections in a 3-sided switch block. (b) Ten types of connections in a 5-sided switch block.

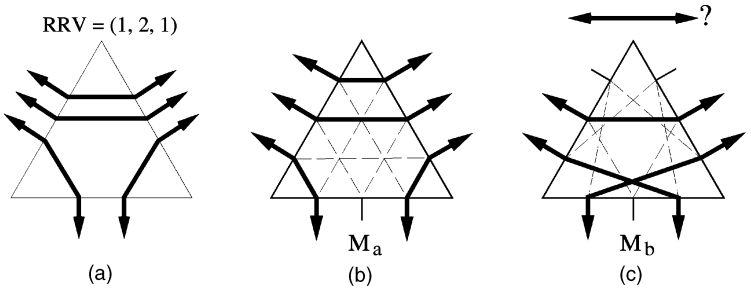

Fig. 6. An example of routing on two 3-sided switch blocks of the same size and flexibility. (a) A routing instance $(1,2,1)$. (b) $(1,2,1)$ is routable on M_a. (c) $(1,2,1)$ is not routable on M_b.

Fig. 10 illustrates the decomposition property. Note that the subblocks of each of the symmetric switch blocks are noninteracting to each other, thus each subblock can be considered independently. Lemma 1 is not only an important property in the proof of the universality of symmetric switch blocks, but is also the key to the layout implementation of a symmetric switch block with a smaller silicon area—the symmetric subblock of size two is a building block for a larger symmetric switch block (see Fig. 10), which can make the layout of a symmetric switch block very regular and compact [14]. Fig. 11 illustrates the reduction property; after removing one side i (terminals and switches) from a symmetric switch block $M_{5,2}$, the remainder is a symmetric switch block $M_{4,2}$.

3.2 Universality of Symmetric Switch Blocks

Let $R(N,W)$ denote the set of all RRVs that satisfy the dimension constraint for an N-sided switch block of size W. We can rewrite Definition 1 as follows:

Definition 2. *A switch block $M_{N,W}$ is universal iff $\vec{n}$ is routable on $M_{N,W}$ for each $\vec{n} \in R(N,W)$.*

We shall prove that each RRV in $R(N,W)$ is routable on our symmetric switch blocks. The space of $R(N,W)$, however, grows dramatically with N and W. (Specifically, the cardinality of $R(N,W)$ grows in $O(W^{\binom{N}{2}})$.) It is thus desirable to identify "critical" RRVs in $R(N,W)$.

3.2.1 Minimal Dominating Set of RRVs

For each $\vec{m}, \vec{n} \in R(N,W)$, $\vec{n}$ is said to *dominate* $\vec{m}$ if and only if $\vec{n} \geq \vec{m}$, i.e., $n_{i,j} \geq m_{i,j}, i,j = 1,2,\ldots,N$. Any RRV $\vec{m}$ is routable on a switch block $M_{N,W}$ if there exists another RRV $\vec{n}$ that is routable on $M_{N,W}$ and $\vec{n} \geq \vec{m}$ [13]. We have the following definition.

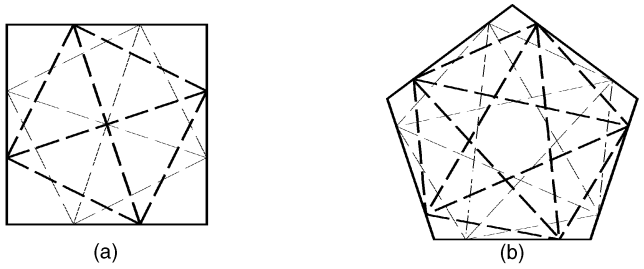

Fig. 7. Clique-based switch blocks. (a) A 4-sided one. (b) A 5-sided one.

Definition 3. *A subset $R_d(N,W)$ of $R(N,W)$ is a dominating set of $R(N,W)$ if $\forall \vec{m} \in R(N,W)$, $\exists \vec{n} \in R_d(N,W)$ such that $\vec{n} \geq \vec{m}$. A dominating set $R_d(N,W)$ is minimal if $\forall \vec{n_i}, \vec{n_j} \in R_d(N,W), i \neq j$, $\vec{n_i} \not\geq \vec{n_j}$ and $\vec{n_j} \not\geq \vec{n_i}$.*

Similarly to [13], we have the following lemma.

Lemma 3. *The minimal dominating set of $R(N,W)$ is unique.*

Proof. Suppose that $R_{d1}(N,W)$ and $R_{d2}(N,W)$ are two different minimal dominating sets of $R(N,W)$. Consider the case when $R_{d1}(N,W) \not\subset R_{d2}(N,W)$. In this case, there exists an $\vec{n}$ such that $\vec{n} \in R_{d1}(N,W)$ and $\vec{n} \notin R_{d2}(N,W)$. Since $R_{d2}(N,W)$ is a dominating set, there exists a $\vec{m} \in R_{d2}(N,W)$ such that $\vec{m} \geq \vec{n}$. Since $R_{d1}(N,W)$ is also a dominating set, there exists a $\vec{p} \in R_{d1}(N,W)$ such that $\vec{p} \geq \vec{m}$ and, thus, $\vec{p} \geq \vec{n}$; a contradiction. Similarly, there is a contradiction in the case when $R_{d2}(N,W) \not\subset R_{d1}(N,W)$. Hence, the minimal dominating set of $R(N,W)$ is unique. □

An RRV $\vec{\gamma} \in R(N,W)$ is called a *maximal RRV* (*MRRV*) if there exists no other RRV in $R(N,W)$ that dominates $\vec{\gamma}$. The following lemma is the key to find the minimal dominating set of $R(N,W)$.

Lemma 4. *$\Gamma(N,W) = \{\vec{\gamma} \mid \vec{\gamma}$ is an MRRV in $R(N,W)\}$ is the minimal dominating set of $R(N,W)$.*

Proof. $\Gamma(N,W)$ is a dominating set since, for any RRV $\vec{n} \in R(N,W)$, there exists an MRRV $\vec{\gamma} \in \Gamma(N,W)$ such that $\vec{\gamma} \geq \vec{n}$. $\Gamma(N,W)$ is minimal since, for any two MRRVs in $\Gamma(N,W)$, they cannot be dominated by each other. □

Lemma 5. *A switch block $M_{N,W}$ is universal iff $\vec{\gamma}$ is routable on $M_{N,W}, \forall \vec{\gamma} \in \Gamma(N,W)$.*

Proof. For each $\vec{n} \in R(N,W)$, there exists $\vec{\gamma} \in \Gamma(N,W)$ that dominates $\vec{n}$. Since $\vec{\gamma}$ is routable on $M_{N,W}$, $\vec{n}$ is also routable on $M_{N,W}$. Hence, $M_{N,W}$ is universal. On the other hand, if $M_{N,W}$ is universal, each $\vec{\gamma} \in \Gamma(N,W) \subset R(N,W)$ is routable on $M_{N,W}$. □

3.2.2 Disjoint Routing Requirement Cycle Set

Based on Lemma 5, we shall focus our discussions on $\Gamma(N,W)$. If we can prove that each MRRV in $\Gamma(N,W)$ is routable on our symmetric NSB of size W, by Lemma 5, our

Algorithm: Symmetric_Switch_Block(N, W)
Input: N—number of sides of the polygonal switch block;
W—number of terminals on each side of the switch block.
Output: $M_{N,W}(T, S)$—the N-sided symmetric switch block of size W;
T: set of terminals; S: set of switches.
/* See Figure 4 for the terminal labeling. */

```
1   T ← t_{i,j},   ∀i = 1,2,...,N,   ∀j = 1,2,...,W;
2   S ← ∅;
3   for k = 1 to ⌊W/2⌋ do
4       for i = 1 to N do
5           for j = 1 to N do
6               if i ≠ j
7                   S ← S ∪ {(t_{i,k}, t_{j,W−k+1})};
8   if W is odd
9       for i = 1 to N do
10          for j = 1 to N do
11              if i ≠ j
12                  S ← S ∪ {(t_{i,⌈W/2⌉}, t_{j,⌈W/2⌉})};
13  Output M_{N,W}(T, S).
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Fig. 8. Algorithm for constructing an N-sided symmetric switch block of size W.

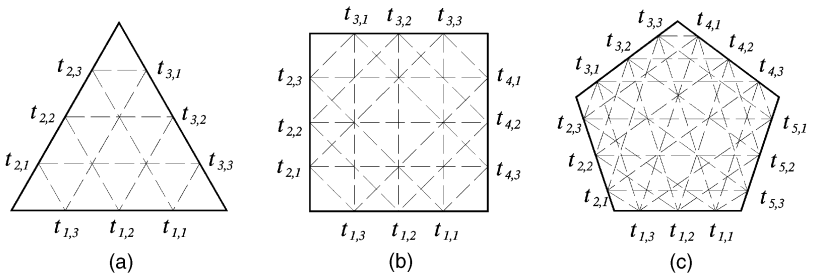

Fig. 9. Three symmetric switch blocks ($W = 3$). (a) A 3-sided symmetric switch block. (b) A square symmetric switch block. (c) A 5-sided symmetric switch block.

symmetric switch blocks are universal. Hence, the MRRV plays a very important role in our proof for universal switch blocks. We have the following lemma associated with MRRVs.

Lemma 6. *When an MRRV $\vec{\gamma} \in \Gamma(N, W)$ is routed on an N-sided switch block of size W, all unused terminals, if any, are on the same side and the number of unused terminals $\phi_{unused} = 2k + (N\ 2)(W\ mod\ 2)$, where $k = 0, 1, 2, \ldots,$ or $\lfloor W/2 \rfloor$.*

Proof. If there are two unused terminals on the different sides (say side i and side j, $i < j$), we can increase $\gamma_{i,j}$ by 1 without violating the dimension constraint, which implies that $\vec{\gamma}$ is not maximal; a contradiction. Hence, all unused terminals, if any, must be on the same side.

The total number of terminals is $\phi_{total} = NW$. Assume that there are ϕ_{used} used terminals; obviously, ϕ_{used} is even since each switch is incident on two terminals and $\phi_{total} - \phi_{used} \leq W$ since all unused terminals, if any, must be on the same side. If N or W is even, ϕ_{total} is even. We have $\phi_{unused} = \phi_{total} - \phi_{used} = 2k$, where $k = 0, 1, 2, \ldots,$ or $\lfloor W/2 \rfloor$. If N and W are both odd, ϕ_{total} is odd. We have $\phi_{unused} = \phi_{total} - \phi_{used} = 2k + 1$, where $k = 0, 1, 2, \ldots,$ or $\lfloor W/2 \rfloor$. Hence, $\phi_{unused} = 2k + (N \bmod 2)(W \bmod 2)$, where $k = 0, 1, 2, \ldots,$ or $\lfloor W/2 \rfloor$. □

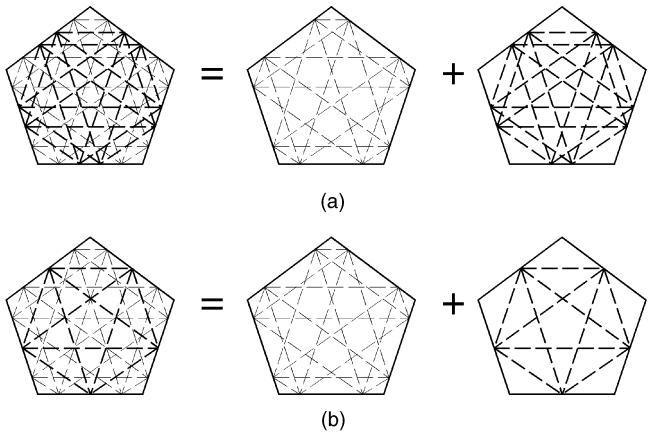

Fig. 10. Two 5-sided symmetric switch blocks and their subblocks. (a) Decomposition of the symmetric switch block of $W = 4$. (b) Decomposition of the symmetric switch block of $W = 3$.

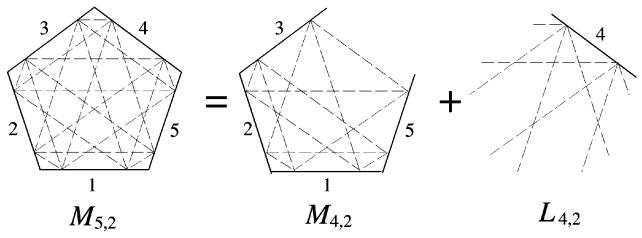

Fig. 11. Reduction of a 5-sided symmetric switch block.

We first consider the MRRVs in $\Gamma(N, 2)$. By Lemma 6, we can classify the MRRVs into two types. One type is that all terminals are used (i.e., $\phi_{unused} = 0$) and we call it a *complete MRRV* (see Fig. 12a). The other type is that two terminals on some side are unused (i.e., $\phi_{unused} = 2$) and we call it a *degenerate complete MRRV* (see Fig. 12c).

For an RRV $\vec{n}$, we introduce an undirected *routing requirement graph* (*RRG*) G. Each vertex v_i in $V(G)$ represents one side s_i of $\vec{n}$. If there is a routing requirement between two different sides s_i and s_j, we introduce an edge between vertices v_i and v_j. For a complete MRRV in $\Gamma(N, 2)$, since all terminals are used, the degree of each vertex in the corresponding RRG is two (see Fig. 12b). For a degenerate MRRV in $\Gamma(N, 2)$, since all terminals are used except two terminals on some side, say side s_i, the degree of each vertex in the corresponding RRG is two except that the degree of v_i is zero (see Fig. 12d). We refer to an RRG with the degree of each vertex two as a *2-RRG*. A cycle in an RRG is called a *routing requirement cycle* (*RRC*). Two routing cycles C_i and C_j are *disjoint* if $V(C_i) \cap V(C_j) = \emptyset$. A *disjoint routing requirement cycle set* (*DRRCS*) Δ is a set of disjoint RRCs. We have the following lemmas associated with DRRCS.

Lemma 7. *A connected 2-RRG forms a cycle.*

Proof. Since the graph is connected and the degree of each vertex is even, there exists a Eulerian circuit. Since the degree of each vertex is 2, the Eulerian circuit forms a cycle. □

Lemma 8. *A 2-RRG G can be divided into a DRRCS Δ such that* $\cup C_i = G, \sum |V(C_i)| = |V(G)|, \forall C_i \in \Delta$.

Proof. An RRG G can be divided into k ($k \geq 1$) connected components $C_1, C_2, \ldots, C_k$, where

$$\cup C_i = G, \sum |V(C_i)| = |V(G)|$$

and

$$V(C_i) \cap V(C_j) = \emptyset, i, j = 1, 2, \ldots, k, i \neq j.$$

Let $\Delta = \{C_1, C_2, \ldots, C_k\}$. By Lemma 7, each component C_i forms a cycle. Since $V(C_i) \cap V(C_j) = \emptyset, i, j = 1, 2, \ldots, k, i \neq j$, Δ is a DRRCS.□

For example, in Fig. 12b, the DRRCS is

$$\{< v_1, v_3, v_4 >, < v_2, v_5 >\}.$$

Lemma 9 (MRRV Decomposition Property). *In an RRG G with the degree of each vertex larger than two, there exists a DRRCS Δ such that*

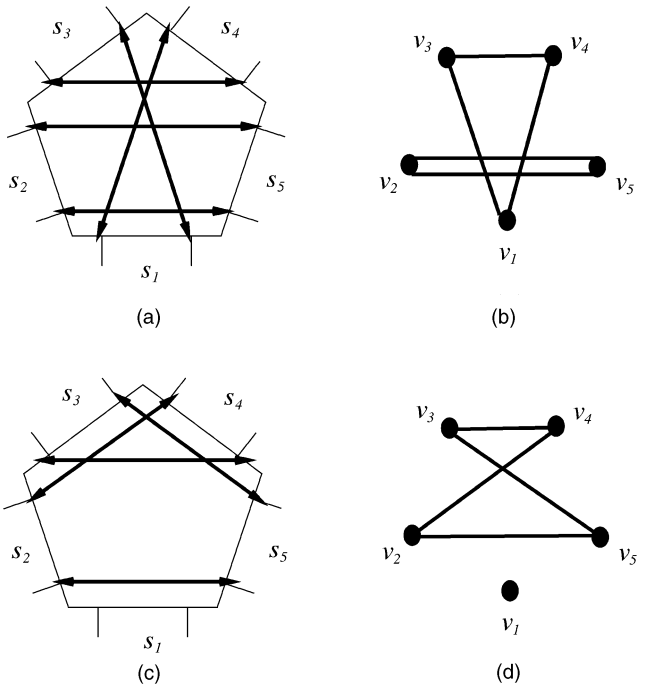

Fig. 12. Two routing examples of MRRVs in $\Gamma(5, 2)$ and their corresponding RRGs. (a) A complete routing example. (b) The corresponding RRG of (a). (c) A degenerate complete routing example. (d) The corresponding RRG of (c).

$$\cup C_i \subset G, \sum |V(C_i)| = |V(G)|, \forall C_i \in \Delta.$$

Proof. Since the degree of each vertex in G is larger than 2, there exists a 2-RRG $G' \subset G$, where $|V(G')| = |V(G)|$. By Lemma 8, there exists a DRRCS Δ such that $\cup C_i = G' \subset G, \sum |V(C_i)| = |V(G')| = |V(G)|, \forall C_i \in \Delta$. □

By Lemmas 7 and 8, an RRG constructed by a DRRCS is a 2-RRG. Thus, we shall focus our discussions on the relation between DRRCSs and symmetric switch blocks of size two.

3.2.3 Proof of Universality

We proceed to prove the universality of symmetric switch blocks. Based on the reduction property of symmetric switch blocks (Lemma 2), we have the following lemma by induction.

Lemma 10. *Given a DRRCS Δ, where $\sum |V(C_i)| = N, \forall C_i \in \Delta$. The RRV corresponding to Δ is routable on the symmetric switch block $M_{N,2}$.*

Proof. We can prove this lemma by induction. When $N = 2$, by the definition of symmetric switch blocks, this lemma holds. Assume that the lemma holds for $N < k$. When $N = k$, assume there are p disjoint RRCs in $\Delta = \{C_1, C_2, \ldots, C_p\}$. Let the RRV corresponding to Δ be $\vec{\gamma}$. There are two cases for p. In case 1, when $p > 1$, then $|V(C_1)| < k$. Let $\Delta = \Delta_1 \cup \Delta_2$, where $\Delta_1 = \{C_1\}$ and $\Delta_2 = \{C_2, C_3, \ldots, C_p\}$. Let the RRVs corresponding to Δ_1 and Δ_2 be $\vec{\gamma'}$ and $\vec{\gamma''}$, respectively, where $\vec{\gamma} = \vec{\gamma'} + \vec{\gamma''}$. Since $|V(C_1)| < k$, $\vec{\gamma'}$ is routable on the symmetric switch block $M_{|V(C_1)|,2}$ and must be routable on $M_{k,2}$. $\vec{\gamma'}$ thus can first be routed on $M_{k,2}$. Let $M_{k-|V(C_1)|,2} = M_{k,2} \setminus \{L_{s_i,2}|$,

each side s_i used by $\vec{\gamma}'$}. By Lemma 2, $M_{k-|V(C_1)|,2}$ is still a symmetric switch block. Since

$$\sum |V(C_i)| = k - |V(C_1)| < k, \forall C_i \in \Delta_2,$$

$\vec{\gamma}''$ is routable on $M_{k-|V(C_1)|,2}$. Hence, $\vec{\gamma}$ is routable on $M_{k,2}$ in case 1. In case 2, when $p = 1$, there is only one RRC in Δ and $|V(C_1)| = k$. Let the RRC sequence be $< v_{i_1}, v_{i_2}, \ldots, v_{i_k} >$. By the definition of symmetric switch block, the RRC sequence can be successfully routed by using k switches

$$(t_{s_{i_1},1}, t_{s_{i_2},2}), (t_{s_{i_2},1}, t_{s_{i_3},2}), \ldots, (t_{s_{i_{k-1}},1}, t_{s_{i_k},2}), (t_{s_{i_k},1}, t_{s_{i_1},2}).$$

Therefore, $\vec{\gamma}$ is routable on $M_{k,2}$ in case 2. □

Before proving the universality of generic symmetric switch blocks, we first consider the universality of symmetric switch blocks of size one and that of size two. Based on the definition of symmetric switch blocks and Lemma 10, we have the following lemmas.

Lemma 11. *The N-sided symmetric switch blocks of size one are universal.*

Proof. For an RRV $\vec{n} \in R(N, 1)$, let the corresponding RRG of $\vec{n}$ be G. Since there is only one terminal on each side, the routing requirements in $\vec{n}$ correspond to pairs of vertices in G, where all vertices are distinct. Let the pairs of vertices be $(v_{i_1}, v_{i_2}), (v_{i_3}, v_{i_4}), \ldots, (v_{i_{2k-1}}, v_{i_{2k}})$, where $2k \leq N$. By the definition of symmetric switch blocks, the routing requirements of $\vec{n}$ can be successfully routed by using k switches

$$(t_{s_{i_1},1}, t_{s_{i_2},1}), (t_{s_{i_3},1}, t_{s_{i_4},1}), \ldots, (t_{s_{i_{2k-1}},1}, t_{s_{i_{2k}},1}).$$

Therefore, the N-sided symmetric switch blocks of size one are universal. □

Lemma 12. *The N-sided symmetric switch blocks of size two are universal.*

Proof. By Lemma 6, there are two types of MRRVs in $\Gamma(N, 2)$: One is the complete MRRV; the other is the degenerate complete MRRV. For a complete MRRV $\vec{\gamma} \in \Gamma(N, 2)$, the corresponding RRG is a 2-RRG. By Lemmas 8 and 10, $\vec{\gamma}$ is routable on the symmetric switch block $M_{N,2}$. For a degenerate complete MRRV $\vec{\gamma} \in \Gamma(N, 2)$, the degree of each vertex in its corresponding RRG G is two except one vertex, say v_i, with the degree zero. Then, $G' = G \setminus \{v_i\}$ is a 2-RRG. Let the MRRV corresponding to G' be $\vec{\gamma}' \in \Gamma(N-1, 2)$. For a symmetric switch block $M_{N,2}$, by Lemma 2, $M_{N-1,2} = M_{N,2} \setminus L_{s_i,2}$ is still a symmetric switch block. By Lemmas 8 and 10, $\vec{\gamma}'$ is routable on $M_{N-1,2}$ and must be routable on $M_{N,2}$. Since the degree of v_i is zero, i.e., there is no routing requirement on side s_i, $\vec{\gamma}'$ and $\vec{\gamma}$ have the same routing requirements. $\vec{\gamma}$ is thus routable on $M_{N,2}$. The degenerate complete MRRV is thus routable on the symmetric switch block of size two. Therefore, by Lemma 5, the symmetric switch blocks of size two are universal. □

Based on Lemmas 11 and 12 and the decomposition property of symmetric switch blocks, we have the following theorem by induction.

Theorem 1. *The N-sided symmetric switch blocks of size W are universal.*

Proof. We can prove this lemma by induction. By Lemma 12, the symmetric switch block $M_{N,2}$ is universal. Assume that the symmetric switch block $M_{N,W}$ is universal for $W < k$, where $k \geq 3$. Now, we shall prove the universality of the symmetric switch block $M_{N,k}$. By Lemma 6, there are two types of MRRVs in $\Gamma(N, W)$: One is $0 \leq \phi_{unused} \leq 1$; the other is $2 \leq \phi_{unused} \leq W$. By Lemma 1, we can decompose $M_{N,k}$ into two universal switch blocks $M_{N,2}$ and $M_{N,k-2}$. For the first type MRRV $\vec{\gamma} \in \Gamma(N, k)$, let the DRV of $\vec{\gamma}$ be $\vec{d}$, where $\vec{d} \leq \vec{D}_{N,k}$. Since $\phi_{unused} \leq 1$, the degree of each vertex in the RRG of $\vec{\gamma}$ is larger than 2. By Lemmas 9 and 10, there exists a DRRCS Δ ($\sum |V(C_i)| = N$) in which the corresponding RRV for Δ is routable on $M_{N,2}$ and can first be routed on $M_{N,2}$. Then, $\vec{\gamma}$ is reduced to $\vec{\gamma}'$, where the DRV of $\vec{\gamma}'$ is $\vec{d}' = \vec{d} - \vec{D}_{N,2}$. It is clear that $\vec{d}' \leq \vec{D}_{N,k-2}$, i.e., $\vec{\gamma}'$ satisfies the dimension constraint of size $k-2$. Then, $\vec{\gamma}'$ is routable on $M_{N,k-2}$. Hence, the first type MRRVs are routable on $M_{N,k}$.

For the other type MRRV $\vec{\gamma} \in \Gamma(N, k)$, let the DRV of $\vec{\gamma}$ be $\vec{d}$, where $\vec{d} \leq \vec{D}_{N,k}$. Suppose the side with unused terminals is s_j. Let the RRG of $\vec{\gamma}$ be G and $G' = G \setminus \{v_j\}$. Since $T_{unused} \geq 2$, the number of terminals on each side connected to side s_j is at most $k-2$. Hence, the degree of each vertex in G' is larger than 2. By Lemmas 9 and 10, there exists a DRRCS Δ ($\sum |V(C_i)| = N-1$) in which the corresponding RRV for Δ is routable on $M_{N-1,2}$ and must be routable on $M_{N,2}$. Then, the RRV corresponding to Δ can first be routed on $M_{N,2}$ and $\vec{\gamma}$ is reduced to $\vec{\gamma}'$, where the DRV of $\vec{\gamma}'$ is $\vec{d}'$ and $d'_i = d_i - 2$ for $1 \leq i \leq k$ except $d'_{s_j} = d_{s_j}$. Since $\phi_{unused} \geq 2$, $d'_{s_j} = d_{s_j} \leq k-2$. It is clear that $\vec{d}' \leq \vec{D}_{N,k-2}$, i.e., $\vec{\gamma}'$ satisfies the dimension constraint of size $k-2$. Then, $\vec{\gamma}'$ is routable on $M_{N,k-2}$. Hence, the other type MRRVs are routable on $M_{N,k}$. By Lemma 5, the symmetric switch block $M_{N,k}$ is universal, implying that the N-sided symmetric switch blocks of size W are universal. □

We have shown the universality of our generic symmetric switch blocks in Theorem 1, i.e., our generic symmetric switch blocks provide the maximum routing capacity. Next, we shall show that our generic symmetric switch blocks use the minimum number of switches. We have the following theorem.

Theorem 2. *No NSB of size W with less than $\binom{N}{2}W$ switches can be universal.*

Proof. By Definition 1, an RRV with only one nonzero component W, such as

$$(W, 0, \ldots, 0), (0, W, 0, \ldots, 0), \ldots, (0, 0, \ldots, 0, W),$$

is routable on a universal NSB. Hence, it needs at least W noninteracting switches for each type of connections to construct a universal NSB. Since there are $\binom{N}{2}$ types of

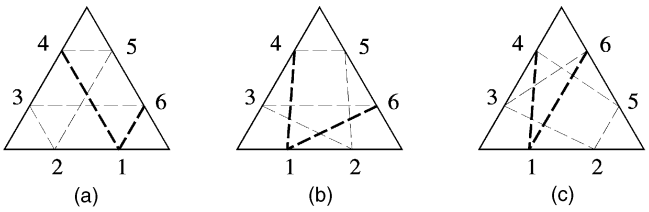

Fig. 13. (a) A 3-sided symmetric switch block. (b), (c) Two 3-sided isomorphic switch blocks of (a).

connections in an NSB, the least number of switches needed to construct a universal NSB is $\binom{N}{2}W$. □

As mentioned in Section 3.1, the total number of switches used in an N-sided symmetric switch block of size W is $\binom{N}{2}W$. Thus, our symmetric switch blocks are the "cheapest" universal ones, i.e., it uses the minimum number of switches to provide the maximum routing capacity. Note that the $\binom{N}{2}W$ requirement is quite small compared to a fully connected switch block which has $\binom{N}{2}W^2$ switches.

3.3 Isomorphism of Switch Blocks

In order to identify not only a single, but also a whole class of universal switch blocks, we apply the terminology *isomorphism* used in [2]. Here, we give its definition.

Definition 4. *Two NSBs $M_{N,W}(T,S)$ and $M'_{N,W}(T',S')$ are isomorphic if there exists a bijection $f: T \rightarrow T'$ such that $(t_{m,n}, t_{u,v}) \in S$ iff $(f(t_{m,n}), f(t_{u,v})) \in S'$ and for any two terminals $t_{m,n}, t_{u,v} \in T_p$ iff $f(t_{m,n}), f(t_{u,v}) \in T_q$, where $p, q = 1, 2, \ldots, N$.*

In other words, $M_{N,W}(T,S)$ and $M'_{N,W}(T',S')$ are isomorphic if we can relabel the terminals of M to be the terminals of M', maintaining the corresponding switches in M and M' and, for terminals on the same side of M, their corresponding terminals are also on the same side of M'. Fig. 13 shows three 3-sided isomorphic switch blocks on which their corresponding terminals are indicated by the same number. For any two isomorphic switch blocks, we have the following theorem.

Theorem 3. *Any two isomorphic switch blocks have the same routing capacity.*

Proof. If $M_{N,W}(T,S)$ and $M'_{N,W}(T',S')$ are isomorphic, we can relabel the types of connections and have the same switch-connection configuration with respect to each type (see Fig. 14 for illustration). Let $\vec{n'}$ be a permutation of $\vec{n}$ so that $\vec{n}$ and $\vec{n'}$ correspond to the original and new definitions of the types of connections, respectively. It is obvious that $\vec{n}$ is routable on $M_{N,W}(T,S)$ if and only if $\vec{n'}$ is routable on $M'_{N,W}(T',S')$; thus, $M_{N,W}(T,S)$ and $M'_{N,W}(T',S')$ have the same routing capacity. □

Corollary 3.1. *For any two isomorphic switch blocks $M_{N,W}(T,S)$ and $M'_{N,W}(T',S')$, $M_{N,W}(T,S)$ is universal iff $M'_{N,W}(T',S')$ is universal.*

By Corollary 3.1, we can obtain a whole class of universal switch blocks by performing isomorphism operations on a symmetric switch block.

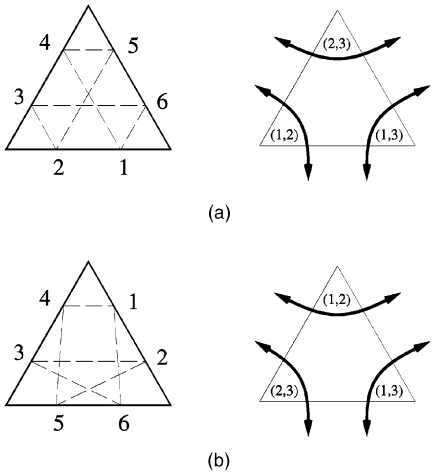

Fig. 14. (a) A switch block and the original type definition. (b) An isomorphic switch block of (a) and its new type definition.

4 Graph Modeling for Detailed Routing

To explore the area performance of switch blocks, we develop a detailed router for 4-HFPGAs. We first model a 4-HFPGA as a graph and apply a graph-search technique to 4-HFPGA routing. For the purpose of easier illustrations, in

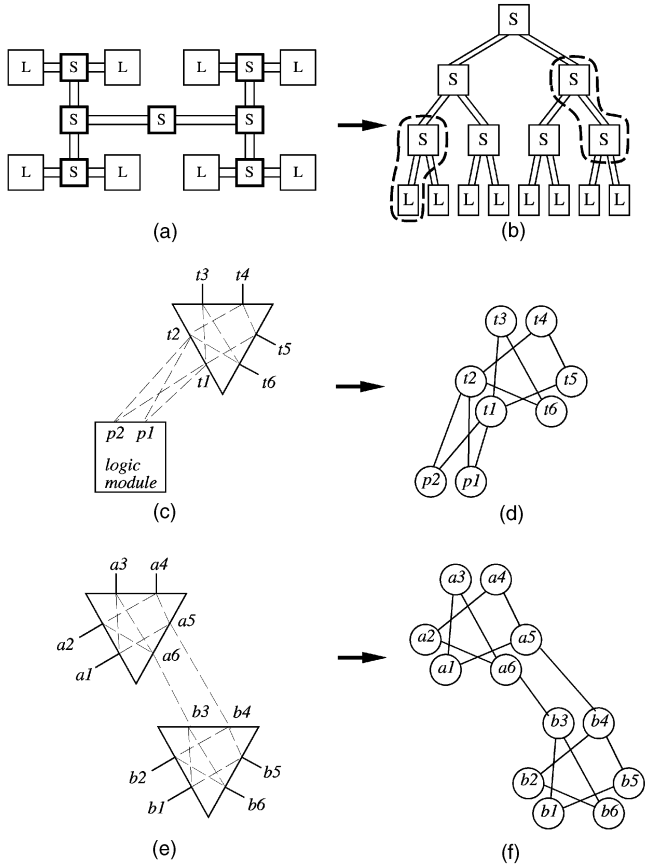

Fig. 15. The graph modeling. (a) A 2-HFPGA architecture. (b) The tree corresponding to (a). (c) The switch connections inside a switch block and that between a logic block and a switch block. (d) The graph corresponding to (c). (e) The switch connections inside switch blocks and that between two switch blocks. (f) The graph corresponding to (e).

TABLE 1
Minimum Number of Tracks Needed for Routing Completion in Situation 1)

p	Net order	Architecture of switch block	Minimum number of tracks for 100% routing								
			100	200	300	400	500	600	700	800	total
1.0	-	Universal	8	15	19	23	29	34	34	37	199
	-	Clique	8	15	20	25	31	35	37	38	209
0.9	Original net order	Universal	7	13	21	23	27	32	38	41	202
		Clique	7	13	21	25	27	34	40	43	210
	Longest net first	Universal	7	12	20	23	27	34	39	42	204
		Clique	7	14	20	24	28	34	41	44	212
	Shortest net first	Universal	7	14	20	22	27	31	38	42	201
		Clique	8	15	21	23	27	33	41	42	210
0.8	Original net order	Universal	9	13	21	24	30	33	38	38	206
		Clique	10	13	22	24	32	36	39	42	218
	Longest net first	Universal	9	13	21	24	29	32	36	40	204
		Clique	9	14	23	26	30	34	40	42	217
	Shortest net first	Universal	9	14	26	28	31	39	41	47	235
		Clique	10	14	27	30	33	42	43	49	248
0.7	Original net order	Universal	8	15	20	24	28	33	38	43	209
		Clique	9	15	22	24	31	37	39	46	223
	Longest net first	Universal	8	14	20	22	29	32	37	43	205
		Clique	8	15	21	24	31	36	39	46	220
	Shortest net first	Universal	10	21	26	31	39	44	50	>50	>271
		Clique	11	21	26	31	40	49	>50	>50	>278

this section, we use a 2-HFPGA as an example to demonstrate the graph modeling.

For a 2-HFPGA (see Fig. 15a), we first transform it into a tree architecture (see Fig. 15b). There are three situations for switch connections: 1) the switch connections inside a switch block (see Fig. 15a and Fig. 15c), 2) those between a logic block and a switch block (see Fig. 15c), and 3) those between two switch blocks (see Fig. 15e). We use a vertex to represent a switch-block terminal or a logic-block pin. If there is a switch connected between two terminals in a switch block or between two switch blocks, or between a logic-block pin and a terminal, we introduce an edge between the two corresponding vertices.

For Situation 1), Fig. 15c shows the switch connections inside a switch block of size two. We introduce a vertex for each terminal ($t_1, t_2, \ldots, t_6$ in Fig. 15d) and an edge for each corresponding pair of terminals ($(t_1, t_3), (t_1, t_5), \ldots, (t_4, t_5)$ in Fig. 15d). For Situation 2), we introduce an edge for a connection between a logic-block pin and a terminal on the adjacent side of a switch block. Fig. 15c shows the modeling for the case when the switch connections between a logic block and a switch block are fully connected. We introduce two vertices p_1 and p_2 for the two pins of the logic block. Since both p_1 and p_2 can be connected to t_1 and t_2, we construct the edges (p_1, t_1), (p_1, t_2), (p_2, t_1), and (p_2, t_2) in Fig. 15d). For Situation 3), we introduce an edge for a connection between two adjacent switch blocks. Fig. 15e shows the modeling for the case when each terminal on a switch block connects to only one terminal on the adjacent side of another switch block. We construct two edges (a_5, b_4) and (a_6, b_3) in Fig. 15f).

Based on the graph modeling, we may formulate the routing problem as finding a set of disjoint trees, one tree for a net and each tree connecting all terminals of a net. Any graph search-based algorithm such as a maze router can be used for detailed routing.

5 Experiments and Results

5.1 Area Performance

In our experiments, we implemented a maze router based on the graph modeling mentioned in the preceding section to explore the effects of switch-block architectures on routing. The router was written in the C language and ran on a SUN Ultra workstation.

We generated connections with lengths based on the *geometric distribution function* because it closely relates to most industrial circuit configurations (e.g., the benchmark circuits in [10], [13], [11]). (Note that no industrial benchmarks for HFPGAs are available.) The geometric distribution function is given as follows:

$$P(p,k) = p(1-p)^{k-1}, \qquad 0 \le p \le 1, \quad k = 1, 2, \ldots,$$

where k is related to connection length and p is a user specified parameter. In the experiments, we randomly generated a set of benchmark circuits on a three-level 4-HFPGA (64 logic blocks) based on the geometric distribution function with p = 1.0, 0.9, 0.8, and 0.7. The 5-sided switch blocks used in the experiments were the universal and clique-based (Xilinx-like) ones with the same number of switches. We assume that all pins of a logic block can be connected to any terminals on the adjacent side of the switch block and each terminal on a switch block connects to only one terminal on the adjacent side of another switch block.

The quality of a switch block was evaluated by the area performance of the detailed router. We determined the minimum number of tracks (W) required for 100 percent routing completion for each circuit, using the two kinds of

TABLE 2
Minimum Number of Tracks Needed for Routing Completion in Situation 2)

p	Net order	Architecture of switch block	Minimum number of tracks for 100% routing								
			100	200	300	400	500	600	700	800	total
1.0	-	Universal	6	14	19	22	30	33	34	37	195
	-	Clique	6	14	18	22	30	33	34	36	193
0.9	Original net order	Universal	7	12	19	21	26	31	37	40	193
		Clique	7	12	19	22	27	32	38	41	198
	Longest net first	Universal	7	12	19	21	26	31	37	40	193
		Clique	7	12	19	22	27	32	38	41	198
	Shortest net first	Universal	6	13	20	23	27	30	37	40	198
		Clique	6	13	20	22	27	30	38	39	197
0.8	Original net order	Universal	9	13	20	23	29	32	35	37	198
		Clique	10	13	20	25	30	32	36	39	205
	Longest net first	Universal	9	13	20	23	29	32	36	38	200
		Clique	10	13	20	25	32	32	39	39	210
	Shortest net first	Universal	10	14	22	29	32	36	42	47	232
		Clique	10	13	22	28	33	38	43	48	235
0.7	Original net order	Universal	9	14	18	21	27	31	35	41	196
		Clique	9	14	19	23	30	33	38	44	210
	Longest net first	Universal	9	14	18	21	28	31	36	41	195
		Clique	9	14	19	23	30	33	38	44	210
	Shortest net first	Universal	10	20	27	31	40	50	>50	>50	>278
		Clique	9	21	25	34	41	>50	>50	>50	>280

switch blocks. Because net ordering often affects the performance of a maze router, we routed the benchmark circuits by using the following three net-ordering schemes to avoid possible biases: 1) original net order in the benchmark circuits, 2) longest net first, and 3) shortest net first. Also, since our main goal is to make fair comparisons for various switch-block architectures, no rip-up and reroute phase was incorporated in the maze router.

In our maze router, we used a shortest-path algorithm to find a routing path for a net. During the process of the shortest-path algorithm, the algorithm chose an unmarked vertex with minimum-cost value for further processing. However, there may be more than one vertex with the minimum-cost value. For the set M_c of the vertices with the minimum cost, we can randomly choose one vertex from the set M_c or just choose the first vertex in the set.

In the experiments, we also considered the constraint for the number of switches inside a switch block used by a net. With the switch-number constraint, a net can use exactly one switch when it passes through a switch block. Without

TABLE 3
Minimum Number of Tracks Needed for Routing Completion in Situation 3)

p	Net order	Architecture of switch block	Minimum number of tracks for 100% routing								
			100	200	300	400	500	600	700	800	total
1.0	-	Universal	6	14	18	22	28	33	34	36	191
	-	Clique	6	14	18	22	30	33	34	36	193
0.9	Original net order	Universal	6	12	19	21	26	31	36	40	191
		Clique	7	12	19	22	27	32	38	41	198
	Longest net first	Universal	6	12	19	21	26	31	36	40	191
		Clique	7	12	19	22	27	32	38	41	198
	Shortest net first	Universal	6	12	19	22	26	30	36	40	191
		Clique	6	12	19	21	26	29	38	39	190
0.8	Original net order	Universal	9	12	19	23	29	32	35	37	196
		Clique	10	13	20	25	32	32	39	39	210
	Longest net first	Universal	9	12	19	23	29	32	36	37	197
		Clique	10	13	20	25	32	32	39	39	210
	Shortest net first	Universal	9	13	21	29	27	33	42	47	221
		Clique	10	13	22	28	33	38	43	48	235
0.7	Original net order	Universal	9	14	18	21	27	31	35	40	195
		Clique	9	14	19	23	30	33	38	44	210
	Longest net first	Universal	9	14	18	21	28	31	36	40	197
		Clique	9	14	19	23	30	33	38	44	210
	Shortest net first	Universal	10	18	27	30	40	50	>50	>50	>265
		Clique	9	21	25	34	41	>50	>50	>50	>280

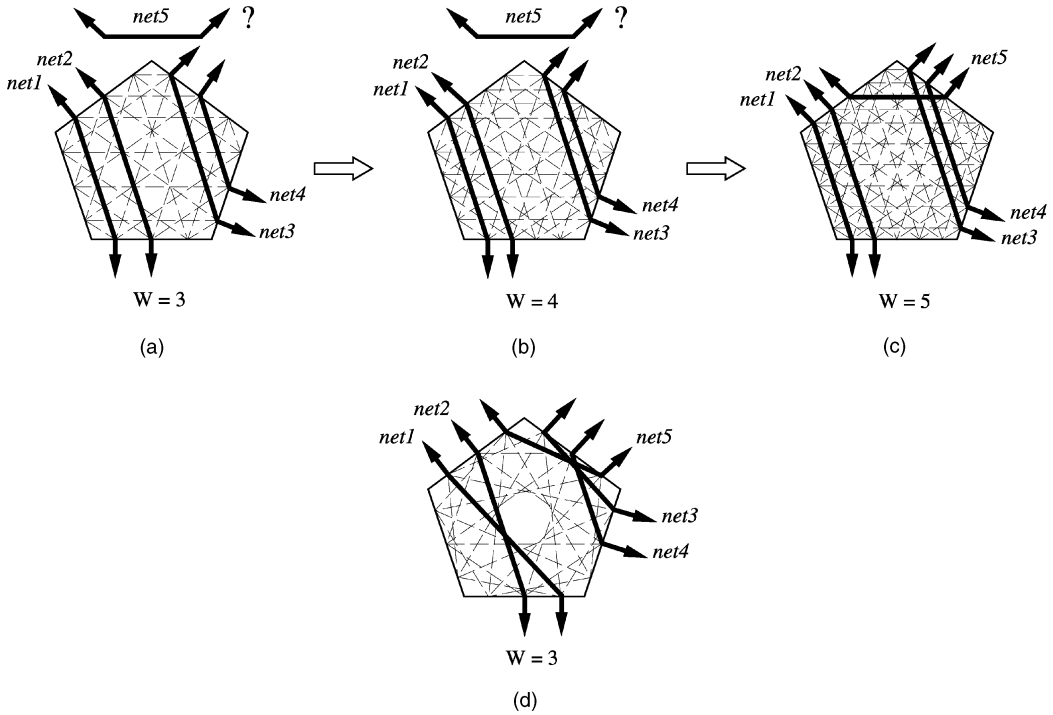

Fig. 16. The example of the blocking anomaly in universal switch-block architectures. Suppose we are to route $net1 - net5$ *sequentially* after $net1 - net4$ have been routed. (a) $net5$ cannot be routed on a symmetric switch block of $W = 3$. (b) $net5$ still cannot be routed after increasing W by one. (c) $net5$ finally can be routed when W is increased to five. (d) The blocking anomaly does not affect the routing in clique-based switch-block architectures.

the switch-number constraint, the number of switches used by a net for passing through a switch block is not limited. Thus, our experiments are classified into three categories by the following situations:

1. Randomly extract a minimum-cost vertex and route a net with the switch-number constraint.
2. Extract the first minimum-cost vertex and route a net with the switch-number constraint.
3. Extract the first minimum-cost vertex and route a net without the switch-number constraint.

The experimental results of Situations 1), 2), and 3) are shown in Tables 1, 2, and 3, respectively. The results show that, no matter in which situation and with which net-ordering scheme, our universal switch blocks usually outperform the clique-based (Xilinx-like) ones in the chip-level area performance.

5.2 Interactions between Switch-Block Architectures and Routing

We explore the interactions between our universal switch-block architectures and routing. We are interested, however, in the case of Situation 2), with $p = 1.0$, in which the total number of tracks needed for the universal switch blocks and the clique-based ones are 195 and 193, respectively—a 1 percent increase in area for the universal switch blocks. In the situation, the router always chose the first minimum-cost vertex and this selection may block subsequent routing nets. Fig. 16a, Fig. 16b, and Fig. 16c illustrate the situation. Fig. 16a shows a 5-sided universal switch block of size three. Suppose we have routed $net1 - net4$ and are routing $net5$. Satisfying the dimension constraint, $net5$ still cannot be routed on the 5-sided switch block. (Note that the universality concept is for routing nets *simultaneously*, but, in this case, we routed the nets *sequentially*.) If we increase W by one and reroute all nets *sequentially*, $net5$ still cannot be routed on the 5-sided switch block of size four (see Fig. 16b). This is because the router always chose the first minimum-cost vertex in the shortest-path algorithm; thus, the terminals on one side would be selected by nets based on the physical order of the terminals. This phenomenon is called *blocking anomaly*. The blocking anomaly introduced by always choosing the first minimum-cost vertex is not favorable to our universal switch blocks, but does not affect the routing in clique-based switch blocks (see Fig. 16d). Therefore, the 1 percent increase in area is caused by the biased router, but not the quality of switch-block architectures. The blocking anomaly is also associated with the switch-number constraint for routing *on a switch block*. In our experiments for Situation 3), when a net was routed without the switch-number constraint, the blocking anomaly did not affect the routing on our universal switch blocks. It is thus significant to consider the interactions between architectures and CAD [11], [15]—even with a best architecture, unsuitable (or biased) routers might offset the advantages of the architecture. Based on our studies, we have four suggestions to avoid the blocking anomaly in our universal switch-block architectures: 1) do not *fix* the scenario for selecting terminals for routing based on their physical order, 2) consider an appropriate switch-number constraint, 3) increase the switch connections between two adjacent

switch blocks to facilitate track permutations, and 4) use a concurrent (nonsequential) router such as hierarchical routers [9], [7] to route all nets simultaneously.

6 Conclusions

We have proposed algorithms to construct a class of generic universal switch blocks. Our universal switch blocks not only have the maximum routing capacities, but also use the minimum numbers of switches. Further, the decomposition property of a universal switch block provides a key insight into its layout implementation with a smaller silicon area. We also developed a maze router for 4-HFPGAs for experimentation. Experimental results show that our universal switch blocks usually outperform the clique-based (Xilinx-like) ones in the chip-level area performance. We further explored the interactions between the universal switch-block architectures and routing. It is significant to consider architectures and CAD simultaneously—even with a best architecture, unsuitable (or biased) routers might offset the advantages of the architecture.

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