Universal Switch Blocks for Three-Dimensional FPGA Design *

Guang-Ming Wu, Michael Shyu, and Yao-Wen Chang
Department of Computer and Information Science
National Chiao Tung University
Hsinchu, Taiwan ROC

Abstract

In this paper, we consider the switch-block design problem for three-dimensional FPGAs. A three-dimensional switch block M with W terminals on each face is said to be universal *if every set of nets satisfying the dimension constraint (i.e., the number of nets on each face of M is at most W) is simultaneously routable through M. In this paper, we present a class of universal switch blocks for three-dimensional FPGAs. Each of our switch blocks has $15W$ switches and* switch-block flexibility *5 (i.e., $F_S = 5$). We prove that no switch block with less than $15W$ switches can be universal. We also compare our switch blocks with others of the topology associated with those used in the Xilinx XC4000 FPGAs. Experimental results demonstrate that our universal switch blocks improve routabilty at the chip level. Further, the decomposition property of the universal switch block provides a key insight into its layout implementation with a smaller silicon area.*

Index Terms—Analysis, Design, Gate-array, Programmable-logic-array

1 Introduction

A conventional FPGA (see Figure 1(a)) consists of an array of logic blocks that can be connected by routing resources [2]. The logic blocks contain circuits used to implement logic functions. The routing resources consist of wire segments and switch blocks. An intersection of a horizontal and a vertical channels is referred to as a switch block; the switch block serves to connect wire segments, and this requires using programmable switches inside it. Figure 1(b) illustrates a switch block in which the programmable switches, denoted by dashed lines between terminals, are shown.

For the work on conventional switch blocks (4-sided blocks), Rose and Brown defined the flexibility of a switch block, represented by F_S, as the number of programming switches between a terminal and others [8]. They investigated the effects of different switch-block flexibilities on routing and suggested that $F_S = 3$ often be sufficient for high routability. Chang, Wong, and Wong first presented a class of *universal switch blocks* [3]. A switch block M with W terminals on each side is said to be *universal* if every set of nets satisfying the dimension constraint (i.e., the number of nets on each side of M is at most W) is simultaneously routable through M [3]. They proved that each of the universal switch blocks can accommodate significantly more

*This work was partially supported by the National Science Council of Taiwan ROC under Grant No. NSC-87-2215-E-009-041.

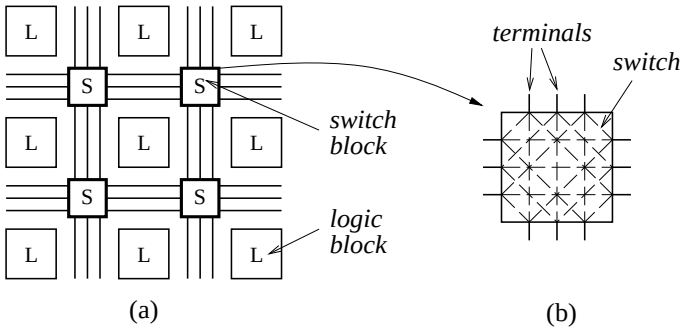

Figure 1: A conventional FPGA and its switch block. (a) A conventional FPGA architecture. (b) A conventional 4-sided switch block.

routing instances than the Xilinx XC4000-type one of the same size. Recently, a report on the layout implementations of the universal switch blocks and the XC4000-type ones has also showed that the universal switch blocks consume a smaller silicon area [11]. Another switch-module architecture called *switch matrices* was modeled and investigated by Zhu, Wong, and Chang [13] and Sun, Wang, Wong, and Liu [9]. Chang, Wong, and Wong later proposed a network-flow based algorithm for switch-matrix design. Wu and Chang recently showed the nonexistence of universal switch *matrices* and presented a class of quasi-universal switch matrices with almost the same routing capacity as universal switch *blocks* [12]. MCM fabrication techniques for multiple FPGAs have been studied recently [1, 5].An MCM-based field programmable architecture for prototyping large designs using multiple FPGAs was proposed in [6]. A three-dimensional (3D) FPGA architecture by stacking together a number of two-dimensional (2D) FPGAs was studied in [1]. A three-dimensional FPGA architecture (see Figure 2(a)) is a generalization based on the conventional 2D FPGA; it stacks a number of 2D FPAG blocks together by MCM fabrication techniques, where each logic block has six adjacent neighbors, as opposed to four in the 2D case [1]. The 3D switch blocks are not the same as the conventional switch blocks (see Figure 2(b)). Each switch block is connected with six adjacent switch blocks. Therefore, they enable each channel segment to connect to some subset of the channel segments incident on the other five faces of the 3D switch block. This unique architecture motivates our study of the 3D switch blocks.

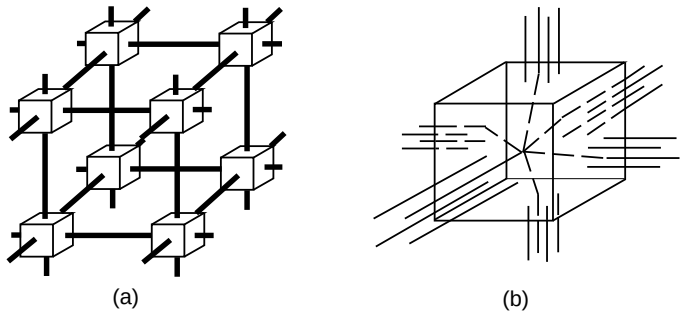

Figure 2: (a) 3D FPGA, (b) 3D switch block.

In this paper, we consider the switch-block design problem for three-dimensional FPGAs. A three-dimensional switch block M with W terminals on each *face* is said to be *universal* if every set of nets satisfying

the dimension constraint (i.e., the number of nets on each *face* of M is at most W) is simultaneously routable through M. In this paper, we present a class of universal switch blocks for three-dimensional FPGAs. Each of our switch blocks has $15W$ switches and *switch-block flexibility* 5 (i.e., $F_S = 5$). We prove that no switch block with less than $15W$ switches can be universal. We also compare our switch blocks with others of the topology associated with those used in the Xilinx XC4000 FPGAs. Experimental results demonstrate that our universal switch blocks improve routabilty at the chip level. The remainder of this article is organized as follows. Section 2 introduces the modeling for 3D switch blocks and their routing. Section 3 presents a class of 3D universal switch blocks and explore their properties. Section 4 considers clique-based switch blocks and compare them with universal switch blocks. Experimental results are reported in Section 5.

2 Switch-Block Modeling

In this section, we present the modeling for 3D switch blocks and their routing. We show that the 3D switch-block design problem can be transformed into the 6-sided one. A three-dimensional switch block is a cubic block with W terminals on each face of the block. We refer to the *size* of the 3D switch block as W. Some pairs of terminals, on different faces of the block, may have programmable switches and thus can be connected by programming the switches to be "ON." Moreover, these switches are electrically *non-interacting*, unless they share a terminal. We represent a 3D switch block by $M_{3d}(T, S)$, where T is the set of terminals, and S the set of switches. Let the faces F_1, F_2, F_3, F_4, F_5, and F_6 represent the front, hind, left, right, top, and bottom faces, respectively (see Figure 3). Label the terminals $t_{1,1}, t_{1,2}, \ldots, t_{1,W}, t_{2,1}, t_{2,2}, \ldots, t_{2,W}, \ldots, t_{6,1}, t_{6,2}, \ldots, t_{6,W}$ starting from the terminals on F_1 to those on F_6. Let $T(F) = \{t_{1,1}, \ldots, t_{1,W}\}$ (front terminals), $T(H) = \{t_{2,1}, \ldots, t_{2,W}\}$ (hind terminals), $T(L) = \{t_{3,1}, \ldots, t_{3,W}\}$ (left terminals), $T(r) = \{t_{4,1}, \ldots, t_{4,W}\}$ (right terminals), $T(T) = \{t_{5,1}, \ldots, t_{5,W}\}$ (*top terminals*), and $T(B) = \{t_{6,1}, \ldots, t_{6,W}\}$ (bottom terminals). Figure 3(b) shows the labeling of the terminals on F_i. Therefore, $S = \{(t_{i,j}, t_{p,q})|$ there exists a programmable switch between $t_{i,j}$ and $t_{p,q}\}$, and $T = \bigcup_{i \in \{F,H,L,R,T,B\}} T(i)$. For convenience, we often refer to a switch block $M_{3d}(T, S)$ simply as M_{3d}, omitting T and S, if there is no ambiguity about T and S, or T and S are not of concern in the context.

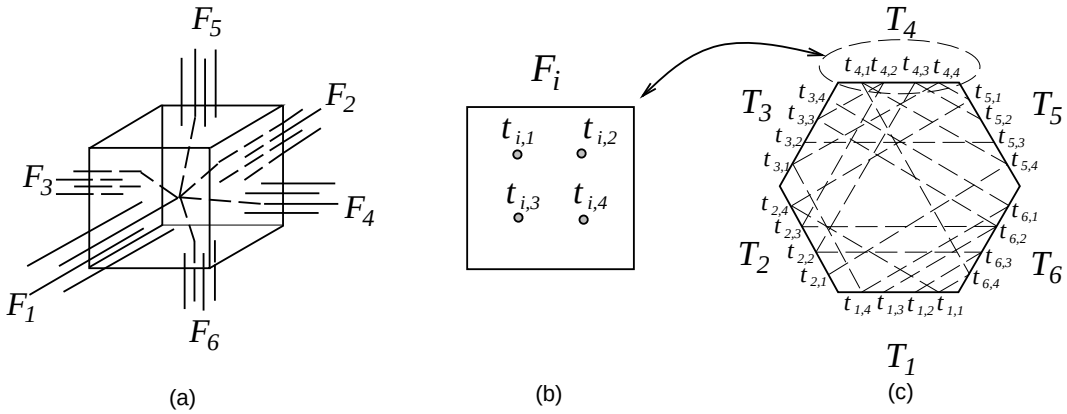

Figure 3: (a) A model of a 3D switch block. (b) One face on the 3D switch block and its terminals. (c) The corresponding 6-sided switch block.

A *hexagonal switch block* (*HSB*) is a 6-sided switch block with V terminals on each side of the block. We say that the HSB is of *size* V. We represent an HSB by $M_h(T_h, S_h)$, where T_h is the set of terminals, and S_h the set of programming switches. Label the terminals $t_{1,1}, t_{1,2}, \ldots, t_{1,V}$, $t_{2,1}, t_{2,2}, \ldots, t_{2,V}$, $\ldots$, $t_{6,1}, t_{6,2}, \ldots, t_{6,V}$ starting from the rightmost terminal on the bottom side and proceeding clockwise. (See Figure 3(c).) Let $T_h(i) = \{t_{i,1}, \ldots, t_{i,V}\}$, where $i = 1, 2, 3, 4, 5$, or 6. Therefore, $S_h = \{(t_{m,n}, t_{u,v}) |$ there exists a programmable switch between terminal $t_{m,n}$ and terminal $t_{u,v}\}$, where $m \neq u$, $m, u = 1, 2, \ldots, 6$, $n, v = 1, 2, \ldots, V$, and $T_h = \cup T_h(i)$, where $i = 1, 2, \ldots, 6$. For convenience, we often refer to $M_h(T_h, S_h)$ simply as M_h, omitting T_h and S_h, if there is no ambiguity about T_h and S_h, or T_h and S_h are not of concern in the context.

In the following, we transform the design problem for the 3D switch blocks into that for the HSBs. For convenience, we modify the terminology *isomorphism* used in [3] as follows. Let $M(T, S)$ ($M'(T', S')$) be a 3D or a hexagonal switch block. We have the following definition.

Definition 1 *Two switch blocks $M(T, S)$ and $M'(T', S')$ are isomorphic if there exists a bijection f: $T \rightarrow T'$ such that $(t_{m,n}, t_{u,v}) \in S$ if and only if $(f(t_{m,n}), f(t_{u,v})) \in S'$ and, for any two terminals $t_{m,n}$, and $t_{u,v}$, $t_{m,n}, t_{u,v} \in T$ if and only if $f(t_{m,n}), f(t_{u,v}) \in T'$.*

In other words, $M(T, S)$ and $M'(T', S')$ are isomorphic if we can relabel the terminals of M to be the terminals of M', maintaining the corresponding switches in M and M'; and for terminals on the same side (face) of M, their corresponding terminals are also on the same side (face) of M'. For any two isomorphic switch blocks, we have the following theorems.

Theorem 1 *[3] Any two isomorphic switch blocks have the same routing capacity.*

Theorem 2 *For any M_{3d} of size W, there exists an M_h of the same size such that M_{3d} and M_h are isomorphic, and vice versa.*

Proof: For an $M_{3d}(S, T)$ of size W, we can construct an $M_h(S_h, T_h)$ of the same size such that $(t_{m,n}, t_{u,v}) \in S_h$ if $(t_{m,n}, t_{u,v}) \in S$, where $m \neq u, m, u = 1, 2, \ldots, 6$ and $n, v = 1, 2, \ldots, W$. Let the mapping function f: $T \rightarrow T_h$ be $f(t_{m,n}) = t_{m,n}$. Obviously, $(t_{m,n}, t_{u,v}) \in S$ if and only if $(f(t_{m,n}), f(t_{u,v})) = (t_{m,n}, t_{u,v}) \in S_h$. Therefore, by Definition 1, M_{3d} and M_h are isomorphic. For an $M_h(S_h, T_h)$ of size V, we can construct an $M_{3d}(S, T)$ of the same size such that $(t_{m,n}, t_{u,v}) \in S$ if $(t_{m,n}, t_{u,v}) \in S_h$, where $m \neq u, m, u = 1, 2, \ldots, 6$ and $n, v = 1, 2, \ldots, V$. Similarly, there exists the bijection f': $T_h \rightarrow T$ such that $f(t_{m,n}) = t_{m,n}$ and $(t_{m,n}, t_{u,v}) \in S_h$ if and only if $(f(t_{m,n}), f(t_{u,v})) = (t_{m,n}, t_{u,v}) \in S$. Therefore, M_{3d} and M_h are isomorphic □ By Theorems 1 and 2, the design problem for the 3D switch block is equivalent to that for the 6-sided switch block. Therefore, we shall focus on the 6-sided switch block in the rest of the paper. In an HSB, the switches are electrically *non-interacting* unless they share a terminal. A *connection* is an electrical path between two terminals (say $t_{m,n}$ and $t_{u,v}$) on different sides of a switch block. If the switch ($t_{m,n}$, $t_{u,v}$) is programmed to be "ON," then a connection between these two terminals is established. Because each connection is characterized by two sides of a block, we can classify all connections passing through a switch block into a number of categories. For an HSB, connections can be of 15 types. See Figure 4 for the type definition.

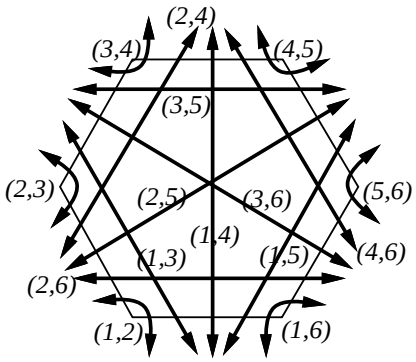

Figure 4: Fifteen types of connections in an HSB.

A *routing requirement vector* (*RRV*) $\vec{n}$ for an HSB is a 15-tuple ($n_{1,2}$,. . .,$n_{1,6}$,$n_{2,3}$,. . .,$n_{2,6}$, $n_{3,4}$,. . .,$n_{3,6}$,$n_{4,5}$,$n_{4,6}$,$n_{5,6}$), where $n_{i,j}$ is the number of type-(i,j) connections required to be routed through an HSB, $0 \leq n_{i,j} \leq V$, $i,j = 1,2,\ldots,6, i \neq j$. An RRV $\vec{n}$ is said to be *routable* on an HSB M_h if there exists a routing for $\vec{n}$ on M_h. For example, Figure 5(a) shows a routing instance with three nets and the RRV $\vec{n} = (0,0,0,0,0,1,1,0,0,1,0,0,0,0,0)$, and Figures 5(b) and (c) show two HSBs with the same flexibility ($F_S = 5$). The RRV $\vec{n}$ is routable on the HSB shown in Figure 5(b), and a routing solution is illustrated by the thick lines. In Figure 5(c), however, there is always one net that cannot be routed into M_b. Thus the RRV $\vec{n}$ is not routable on the HSB shown in Figure 5(c).

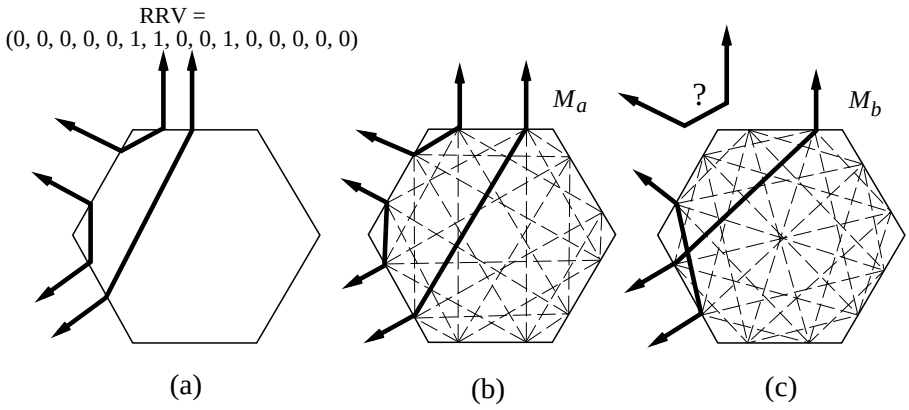

Figure 5: An example of routing on two HSBs of the same size and same flexibility. (a) A routing instance $\vec{n} = (0,0,0,0,0,1,1,0,0,1,0,0,0,0,0)$. (b) $\vec{n}$ is routable on M_a. (c) $\vec{n}$ is not routable on M_b.

The *routing capacity* of a switch block M is referred to as the number of distinct routable vectors on M; that is, the routing capacity of M is the cardinality $|\{\vec{n}|\vec{n}$ is routable on $M\}|$. A switch block M with V terminals on each side is called *universal* if every set of nets satisfying the dimension constraint (i.e., the number of nets on each side of M is at most V) is simultaneously routable through M. We have the following definition.

Definition 2 *An HSB M_h of size V is called universal if the following set of inequalities is the necessary*

and sufficient conditions for an RRV $\vec{n} = (n_{1,2}, \ldots, n_{1,6}, n_{2,3}, \ldots, n_{2,6}, n_{3,4}, \ldots, n_{3,6}, n_{4,5}, n_{4,6}, n_{5,6})$ *to be routable on* M_h*:*

$$n_{1,2} + n_{1,3} + n_{1,4} + n_{1,5} + n_{1,6} \leq V \quad (1)$$

$$n_{1,2} + n_{2,3} + n_{2,4} + n_{2,5} + n_{2,6} \leq V \quad (2)$$

$$n_{1,3} + n_{2,3} + n_{3,4} + n_{3,5} + n_{3,6} \leq V \quad (3)$$

$$n_{1,4} + n_{2,4} + n_{3,4} + n_{4,5} + n_{4,6} \leq V \quad (4)$$

$$n_{1,5} + n_{2,5} + n_{3,5} + n_{4,5} + n_{5,6} \leq V \quad (5)$$

$$n_{1,6} + n_{2,6} + n_{3,6} + n_{4,6} + n_{5,6} \leq V \quad (6)$$

We refer to the *dimension constraint* as the set of inequalities which characterizes a 6-sided universal switch block of size V. Therefore, the dimension constraint for an HSB is the set of Inequalities (1)–(6) listed in Definition 2. Note that the number of nets routed through each side of a switch block can not exceed V; therefore, a universal switch block has the maximum routing capacity.

3 Universal Switch Blocks

In this section, we present an algorithm for constructing symmetric HSBs and prove that the symmetric HSBs are universal. The symmetric HSB of size V has only $15V$ switches. We prove that no HSB with less than $15V$ switches can be universal. Based on isomorphism operations (Theorem 1), we can identify a whole class of universal switch blocks.

3.1 Symmetric Switch Blocks

Algorithm Symmetric_Switch_Block shown in Figure 6 constructs a 6-sided switch block M_h of size V. We refer to the topology of the switch block constructed by the algorithm as the *symmetric topology* and the switch block as the *symmetric switch block*. Figure 7 shows two examples of symmetric switch blocks. For a symmetric switch block, it has the flexibility (F_S) of 5; thus, the total number of switches in the symmetric switch block of size V is equal to $\frac{6 \times V \times F_s}{2} = 3 \times V \times F_s = 15V$.

For a symmetric switch block with an even V terminals on each side, it can be partitioned into $V/2$ sub-blocks of size two; and for an odd V, it can be partitioned into $\lfloor V/2 \rfloor$ sub-blocks of size two and one sub-block of size one. Thus, we have the following property.

Lemma 1 *(Switch-Block Decomposition Property) A symmetric switch block of size* V *can be partitioned into* $\lfloor V/2 \rfloor$ *symmetric sub-blocks of size two and* (V mod 2) *symmetric sub-block of size one.*

Proof: Consider Algorithm Symmetric_Switch_Block. For each k in line 3, we construct a symmetric sub-block of size two in lines 4–6. Therefore, we will have $\lfloor V/2 \rfloor$ sub-blocks of size two after $\lfloor V/2 \rfloor$ iterations (see line 3). Further, all these symmetric switch blocks of size two constructed in lines 4–6 have the same topology. Lines 7–10, just for an odd V, construct a clique of six nodes (i.e., a sub-block of size one) from the middle terminal of each side of the switch block. Thus we will have (V mod 2) such sub-block of size one (see lines 7–10). See Figure 8 for illustrations. □

Algorithm: Symmetric_Switch_Block(V)
Input: V—size of the hexagonal switch block.
Output: $M_h(T_h, S_h)$—the hexagonal switch block of size V;
T_h: set of terminals; S_h: set of switches.
/* See Figure 3(c) for the terminal labeling. */

1 $T_h \leftarrow t_{i,j}, \quad \forall i = 1, 2, \ldots, 6, \quad \forall j = 1, 2, \ldots, V;$
2 $S_h \leftarrow \emptyset;$
3 **for** $k = 1$ **to** $\lfloor \frac{V}{2} \rfloor$ **do**
4 **for** $i = 1$ **to** 6 **do**
5 **for** $j = 1$ **to** 6 **do**
6 $S_h \leftarrow S_h \cup \{(t_{i,k}, t_{j,V-k+1})\}, \ i \neq j;$
7 **if** V is odd
8 **for** $i = 1$ **to** 6 **do**
9 **for** $j = 1$ **to** 6 **do**
10 $S_h \leftarrow S_h \cup \{(t_{i,\lceil \frac{V}{2} \rceil}, t_{j,\lceil \frac{V}{2} \rceil})\}, \ i \neq j;$
11 **Output** $M_h(T_h, S_h)$.

Figure 6: Algorithm for constructing a 6-sided symmetric switch block of size V.

Note that these sub-blocks are non-interacting to each other; thus, each sub-block can be considered independently. Lemma 1 is not only an important property in the proof of the universality of symmetric HSBs, but is also the key to the layout implementation of an HSB with a smaller silicon area—the symmetric sub-block of size two is a building block for a larger symmetric switch block (see Figure 8), which can make the layout of an HSB very regular and compact [11].

3.2 Proof of Universality

In this subsection, we prove that the symmetric switch blocks constructed by Algorithm Symmetric_Switch_Block are universal. To show that the symmetric switch blocks are universal, we first prove that the symmetric

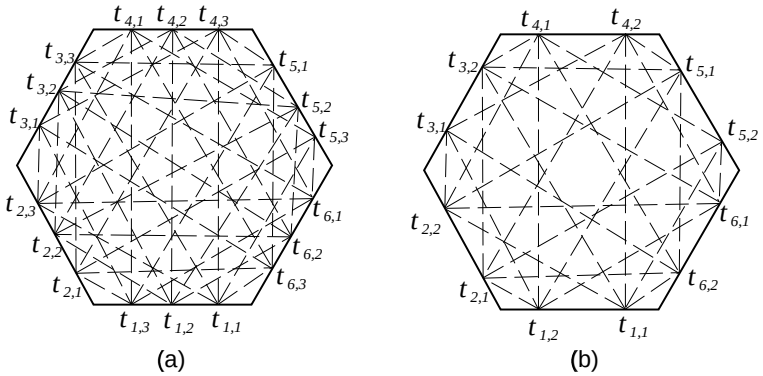

Figure 7: Two symmetric hexagonal switch blocks. (a) A symmetric HSB of $V = 3$. (b) A symmetric HSB of $V = 2$.

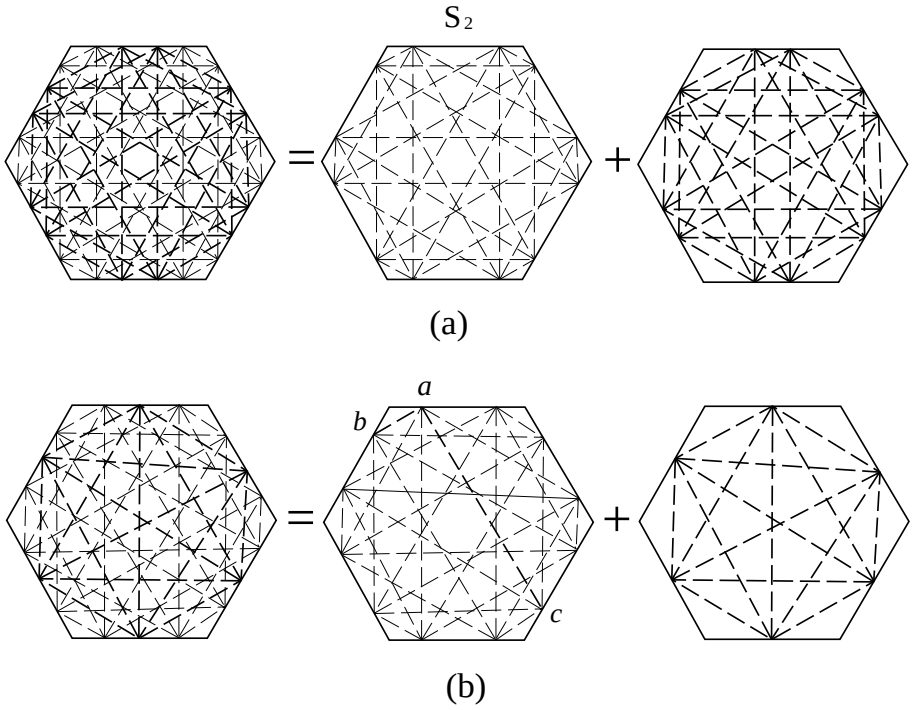

Figure 8: Two symmetric HSBs and their sub-blocks. (a) Decomposition of the symmetric HSB of $V = 4$. (b) Decomposition of the symmetric HSB of $V = 3$.

HSBs of size two are universal.

Lemma 2 *The HSB M_h of size two constructed by Algorithm Symmetric_Switch_Block is universal.*

Proof: By Definition 2, we must prove that $\vec{n}$ is routable on M_h if and only if the following inequalities are simultaneously satisfied:

$$n_{1,2} + n_{1,3} + n_{1,4} + n_{1,5} + n_{1,6} \leq 2 \quad (7)$$

$$n_{1,2} + n_{2,3} + n_{2,4} + n_{2,5} + n_{2,6} \leq 2 \quad (8)$$

$$n_{1,3} + n_{2,3} + n_{3,4} + n_{3,5} + n_{3,6} \leq 2 \quad (9)$$

$$n_{1,4} + n_{2,4} + n_{3,4} + n_{4,5} + n_{4,6} \leq 2 \quad (10)$$

$$n_{1,5} + n_{2,5} + n_{3,5} + n_{4,5} + n_{5,6} \leq 2 \quad (11)$$

$$n_{1,6} + n_{2,6} + n_{3,6} + n_{4,6} + n_{5,6} \leq 2. \quad (12)$$

(If) It is not difficult to identify all of the RRVs satisfying Inequalities (7)–(12). (In fact, there are 2578 such RRVs.) We verify the RRVs and conclude that they can all successfully be routed on the HSB of size two constructed by Algorithm Symmetric_Switch_Block [1]. The key insight is that the two terminals, say terminals b and c, which connect to a terminal, say a, do not share any switch (see Figure 8(b)); thus the connections associated with them are non-interacting, except those associated with a.

[1] In fact, based on the work in [10], we need to check only the RRVs in the corresponding *dominating set* (see [10] for the definition of dominating sets).

(Only If) For an HSB M_h of size two, the total number of connections routed through each side of M_h cannot exceed two. Hence, if $\vec{n}$ is routable on M_h, the six inequalities must be satisfied. □

Let U_V denote the set of RRVs which satisfies the dimension constraint for an HSB of size V. An RRV $\vec{\gamma} \in U_V$ is called a *maximal RRV* (*MRRV*) if there exists no other RRV in U_V that dominates $\vec{\gamma}$. In the following, we show that all RRVs in U_V can be decomposed into U_{V-2} and U_2. Similarly, we need to check only the RRVs in the corresponding dominating set (i.e., MRRVs). We have the following lemma.

Lemma 3 *When an MRRV $\vec{\gamma} \in U_V$ is routed on an HSB, all unused terminals, if any, must be on the same side and the number of unused terminals $\phi_{unused} = 2c$, $0 \leq c \leq \lfloor V/2 \rfloor$, $c \in Z$.*

Proof: If there are two unused terminals on different sides (say sides i and j, $i < j$), we can increase $\gamma_{i,j}$ by one without violating the dimension constraint, implying that $\vec{\gamma}$ is not maximal: a contradiction. Hence, all unused terminals, if any, must be on the same side. Note that the total number of terminals is $\phi_{total} = 6V$, an even number. Assume that there are ϕ_{used} used terminals. Obviously, ϕ_{used} is even since each switch is incident on two terminals. Also, $\phi_{unused} = \phi_{total} - \phi_{used} \leq V$ since all unused terminals, if any, must be on the same side. Since ϕ_{total} and ϕ_{used} are even numbers and $0 \leq \phi_{unsed} \leq V$, $\phi_{unused} = \phi_{total} - \phi_{used} = 2c$, $0 \leq c \leq \lfloor V/2 \rfloor$, $c \in Z$. □

Consider the MRRVs in U_V. By Lemma 3, we can classify the MRRVs into two types. One is that all terminals are used (i.e., $\phi_{unused} = 0$), and we call an MRRV of this type a *complete MRRV*. The other is that an even number of terminals on the same side are unused (i.e., $\phi_{unused} = 2c, c \in Z^+$), and we call an MRRV of this type a *degenerate complete MRRV*.

To show that an MRRV in U_V can be decomposed into U_{V-2} and U_2, we first construct a multiple graph and a weighted graph for the MRRV as follows: For any MRRV we construct a multiple graph $G_m(V_m, E_m)$, where $V_m = \{v_1, v_2, \ldots, v_6\}$. If $n_{i,j} = 1$, construct an edge between v_i and v_j with weight 1; if $n_{i,j} \geq 2$, construct two edges between v_i and v_j with total weights equal to $n_{i,j}$. (We call the two edges a *multi-edge*.) We induce a weighted graph $G_w(V_w, E_w)$ from $G_m(V_m, E_m)$ by substituting a *weighted edge* for a multi-edge. Figures 9(b) and 9(c) show a multiple graph G_{m_1} for $\vec{n} = (1,0,1,0,1,1,0,1,0,1,0,0,1,0,3)$ and its corresponding weighted graph G_{w_1}, respectively. In G_{m_1}, there are two edges between v_5 and v_6 because $n_{5,6} = 3$; thus, we construct the corresponding weighted edge (v_5, v_6) in G_{w_1}. In a weighted graph $G_w(V_w, E_w)$, a vertex $v \in V_w$ represents one side of an HSB, an edge $e \in E_h$ represents a type of connection between two sides of the HSB, and *weight(e)* denotes the number of connections of the type associated with e.

Let C_k denote a connected component of k vertices in G_w. We have the following lemma.

Lemma 4 *For a weighted graph G_w associated with a complete MRRV, there exists no isolated vertex in G_w and, for $k \geq 3$, C_k contains no degree-one vertex.*

Proof: There exists no isolated vertex in G_w, since the total connections associated with a complete MRRV for a side of HSB must be equal to V. Suppose there exists a $G_w(V_w, E_w)$ (associated with a complete MRRV) for an HSB of size V with a connected component C_k and, for $k \geq 3$, C_k contains a degree-one vertex v_i. Let v_i connect to a vertex v_j by an edge $e_{i,j} = (v_i, v_j)$. Since G_w is associated with a complete MRRV and v_i is a degree-one vertex. The total number of connections associated with v_i, weight$(e_{i,j})$, is equal to

the dimension constraint V. Further, the total number of connections associated with a vertex can be V at most; since weight$(e_{i,j}) = V$, v_j only connects to v_i. Hence, the degree of v_j must also equal one, implying that v_i and v_j form a C_2: a contradiction. Therefore, there exists no C_k ($k \geq 3$) with degree-one vertex in G_w. □

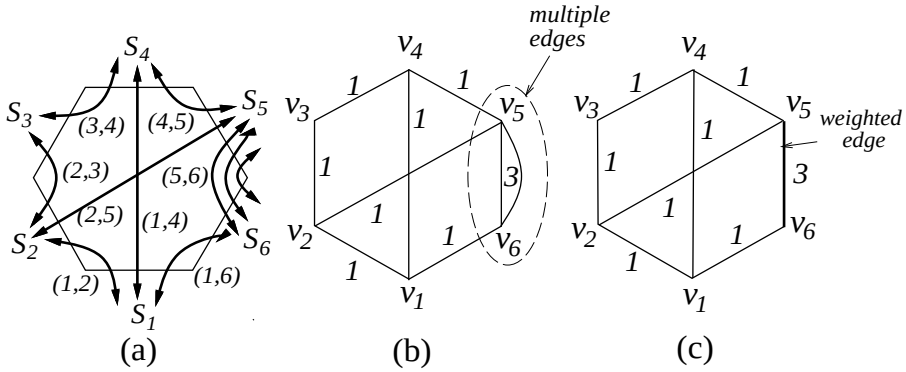

Figure 9: (a) A routing instance $\vec{n} = (1, 0, 1, 0, 1, 1, 0, 1, 0, 1, 0, 0, 1, 0, 3)$. (b) A multiple graph G_{m_1} associated with RRV $\vec{n}$. (c) A weighted graph G_{w_1} of (b).

A *hamiltonian subcycle* of a multiple graph $G_m(V_m, E_m)$ is a simple cycle that contains a subset of vertices in V_m. Two hamiltonian subcycles in a multiple graph are called *independent* if the two subcycles share no vertex. A multiple graph $G_m(V_m, E_m)$ is said to be *sub-hamiltonian* if it contains a set of independent hamiltonian subcycles and all vertices in V_m are on the subcycles; otherwise, it is *non-sub-hamiltonian*. Also, we call a weighted graph sub-hamiltonian if its associated multiple graph is sub-hamiltonian. For three RRVs $\vec{u}$, $\vec{v}$, and $\vec{x}$, we say $\vec{u}$ to be a *sub-RRV* of $\vec{v}$ if there exists an $\vec{x}$ such that $\vec{v} = \vec{u} + \vec{x}$. Let $\vec{n_i}$ be a sub-RRV of $\vec{n}$. We define Ω and Ω' as follows:

$$\begin{aligned} \Omega &= \{\vec{n} | \vec{n} \in U_V\}, \\ \Omega' &= \{\vec{n} | \vec{n} = \vec{n_1} + \vec{n_2}, \vec{n_1} \in U_{V-2} \text{ and } \vec{n_2} \in U_2\}, \text{ where } V \geq 2. \end{aligned}$$

We have the following Lemmas.

Lemma 5 *If the multiple graph of an MRRV $\vec{n}$ is sub-hamiltonian, $\vec{n}$ has a complete sub-RRV $\vec{n_2} \in U_2$.*

Proof: Let G_m be a sub-hamiltonian graph associated with an MRRV $\vec{n}$. G_m has a set of independent hamiltonian subcycles $I = \{c_1, c_2, \ldots, c_k\}$ that covers all vertices in G_m. We can choose a sub-RRV $\vec{n_2}$ of $\vec{n}$ as follows. For any cycle $c_i \in S$, $c_i =< v_{i_1}, v_{i_2}, \ldots, v_{i_k}, v_{i_1} >$. If $k = 2$, let $n_{2,(v_{i_1}, v_{i_2})} = 2$; otherwise, let $n_{2,(v_{i_1}, v_{i_2})} = n_{2,(v_{i_2}, v_{i_3})} = \ldots = n_{2,(v_{i_k}, v_{i_1})} = 1$. We traverse G_m based on I. I includes independent hamiltonian subcycles which contain all vertices in G_m. All vertices will be visited one time. A vertex in G_m corresponds to one side of an HSB associated with $\vec{n}$. Every vertex contributes two degrees in I. Thus, the number of connections with one side of the HSB is equal to 2. $\vec{n_2}$ satisfies the following inequalities:

$$\begin{aligned} n_{2,(1,2)} + n_{2,(1,3)} + n_{2,(1,4)} + n_{2,(1,5)} + n_{2,(1,6)} &= 2 \\ n_{2,(1,2)} + n_{2,(2,3)} + n_{2,(2,4)} + n_{2,(2,5)} + n_{2,(2,6)} &= 2 \end{aligned}$$

$$
\begin{aligned}
n_{2,(1,3)} + n_{2,(2,3)} + n_{2,(3,4)} + n_{2,(3,5)} + n_{2,(3,6)} &= 2 \\
n_{2,(1,4)} + n_{2,(2,4)} + n_{2,(3,4)} + n_{2,(4,5)} + n_{2,(4,6)} &= 2 \\
n_{2,(1,5)} + n_{2,(2,5)} + n_{2,(3,5)} + n_{2,(4,5)} + n_{2,(5,6)} &= 2 \\
n_{2,(1,6)} + n_{2,(2,6)} + n_{2,(3,6)} + n_{2,(4,6)} + n_{2,(5,6)} &= 2.
\end{aligned}
$$

Thus, $\vec{n_2} \in U_2$ and it is a complete MRRV. □

Lemma 6 *(RRV Decomposition Property)* $\Omega = \Omega'$.

Proof: First, we show that $\Omega' \subseteq \Omega$. By Definition 2, an RRV $\vec{n_1} \in U_{V-2}$ if and only if the following inequalities are simultaneously satisfied:

$$
\begin{aligned}
n_{1,(1,2)} + n_{1,(1,3)} + n_{1,(1,4)} + n_{1,(1,5)} + n_{1,(1,6)} &\leq V-2 && (13)\\
n_{1,(1,2)} + n_{1,(2,3)} + n_{1,(2,4)} + n_{1,(2,5)} + n_{1,(2,6)} &\leq V-2 && (14)\\
n_{1,(1,3)} + n_{1,(2,3)} + n_{1,(3,4)} + n_{1,(3,5)} + n_{1,(3,6)} &\leq V-2 && (15)\\
n_{1,(1,4)} + n_{1,(2,4)} + n_{1,(3,4)} + n_{1,(4,5)} + n_{1,(4,6)} &\leq V-2 && (16)\\
n_{1,(1,5)} + n_{1,(2,5)} + n_{1,(3,5)} + n_{1,(4,5)} + n_{1,(5,6)} &\leq V-2 && (17)\\
n_{1,(1,6)} + n_{1,(2,6)} + n_{1,(3,6)} + n_{1,(4,6)} + n_{1,(5,6)} &\leq V-2, && (18)
\end{aligned}
$$

and for an RRV $\vec{n_2} \in U_2$, the following inequalities are simultaneously satisfied:

$$
\begin{aligned}
n_{2,(1,2)} + n_{2,(1,3)} + n_{2,(1,4)} + n_{2,(1,5)} + n_{2,(1,6)} &\leq 2 && (19)\\
n_{2,(1,2)} + n_{2,(2,3)} + n_{2,(2,4)} + n_{2,(2,5)} + n_{2,(2,6)} &\leq 2 && (20)\\
n_{2,(1,3)} + n_{2,(2,3)} + n_{2,(3,4)} + n_{2,(3,5)} + n_{2,(3,6)} &\leq 2 && (21)\\
n_{2,(1,4)} + n_{2,(2,4)} + n_{2,(3,4)} + n_{2,(4,5)} + n_{2,(4,6)} &\leq 2 && (22)\\
n_{2,(1,5)} + n_{2,(2,5)} + n_{2,(3,5)} + n_{2,(4,5)} + n_{2,(5,6)} &\leq 2 && (23)\\
n_{2,(1,6)} + n_{2,(2,6)} + n_{2,(3,6)} + n_{2,(4,6)} + n_{2,(5,6)} &\leq 2. && (24)
\end{aligned}
$$

Let $\vec{n} = \vec{n_1} + \vec{n_2}$, $n_{1,2} = n_{1,(1,2)} + n_{2,(1,2)}$, $n_{1,3} = n_{1,(1,3)} + n_{2,(1,3)}$, $\ldots$, $n_{5,6} = n_{1,(5,6)} + n_{2,(5,6)}$. Combining Inequalities (13) and (19), (14) and (20), (15) and (21), (16) and (22), (17) and (23), and (18) and (24). We have Inequalities (25)–(30) as follows:

$$
\begin{aligned}
n_{1,2} + n_{1,3} + n_{1,4} + n_{1,5} + n_{1,6} &\leq V && (25)\\
n_{1,2} + n_{2,3} + n_{2,4} + n_{2,5} + n_{2,6} &\leq V && (26)\\
n_{1,3} + n_{2,3} + n_{3,4} + n_{3,5} + n_{3,6} &\leq V && (27)\\
n_{1,4} + n_{2,4} + n_{3,4} + n_{4,5} + n_{4,6} &\leq V && (28)\\
n_{1,5} + n_{2,5} + n_{3,5} + n_{4,5} + n_{5,6} &\leq V && (29)\\
n_{1,6} + n_{2,6} + n_{3,6} + n_{4,6} + n_{5,6} &\leq V. && (30)
\end{aligned}
$$

Thus, $\vec{n} \in U_V$, and we have $\Omega' \subseteq \Omega$.

Next, we show that $\Omega \subseteq \Omega'$. It suffices to show that each MRRV $\vec{n} \in \Omega$ is also in Ω'. By Lemma 3, all unused terminals for routing an MRRV on an HSB are on the same side, and the number of unused terminals is even. Without loss of generality, assume that all unused terminals, if any, are on side 1 and the number of unused terminals is equal to c_1, $0 \leq c_1 \leq \lfloor V/2 \rfloor$. By Definition 2, an MRRV $\vec{n} \in \Omega$ if and only if the following equalities are simultaneously satisfied:

$$n_{1,2} + n_{1,3} + n_{1,4} + n_{1,5} + n_{1,6} = V - 2c_1 \quad (31)$$

$$n_{1,2} + n_{2,3} + n_{2,4} + n_{2,5} + n_{2,6} = V \quad (32)$$

$$n_{1,3} + n_{2,3} + n_{3,4} + n_{3,5} + n_{3,6} = V \quad (33)$$

$$n_{1,4} + n_{2,4} + n_{3,4} + n_{4,5} + n_{4,6} = V \quad (34)$$

$$n_{1,5} + n_{2,5} + n_{3,5} + n_{4,5} + n_{5,6} = V \quad (35)$$

$$n_{1,6} + n_{2,6} + n_{3,6} + n_{4,6} + n_{5,6} = V. \quad (36)$$

Algorithm RRV-Decomposition listed in Figure 10 shows a method to decompose $\vec{n} \in U_V$ into $\vec{n_1}$ and $\vec{n_2}$, where $\vec{n_1} \in U_{V-2}$ and $\vec{n_2} \in U_2$. It derives $\vec{n}$ based on the two cases: (1) $\vec{n}$ is a complete MRRV, and (2) $\vec{n}$ is a degenerate complete MRRV.

We first consider the case where $\vec{n}$ is a complete MRRV. Let G_w be a weighted graph of $\vec{n}$ and C_i be a connected component of i vertices in G_w. By Lemma 4, there exists no isolated vertex or any C_k, $k \geq 3$, with a degree-one vertex in G_w. Thus, the number of vertices in C_k could only be 2, 3, 4, or 6.

We classify all weighted graphs for complete MRRVs into four categories α, β, γ, and δ, listed in Table 1. (Note that the weighted graphs, except C_2, contain no isolated vertex or degree-one vertex.) Categories α, β, γ, and δ represent the cases where G_w consists of three C_2's, one C_2 and one C_4, two C_3's, and one C_6, respectively. The total number of weighted graphs with complete MRRVs is 56, and twelve of them are illegal, which can be verified by checking if the total edge weights of the graphs equal $3V$. (Note that all $6V$ terminals are used for a complete MRRV, and a connection is incident on two terminals.) For example, Figure 11(a) shows an infeasible weighted graph G_w. Consider vertices v_1 and v_4. The total number of connections associated with v_1 must be equal to the dimension constraint V (i.e., all terminals on each side of the HSB are used); therefore, $|e_1| + |e_2| + |e_3| + |e_4| = V$. Similarly, there are V connections associated with v_4, and thus $|e_5| + |e_6| + |e_7| + |e_8| = V$. Therefore, the total number of connections associated with G_w is equal to $2V$. By Equalities (31)–(36), however, the total number of connections associated with a complete MRRV must be equal to $3V$. Therefore, G_w is illegal. We have the facts that the other 44 weighted graphs are sub-hamiltonian. (Table 1 summarizes the number of legal and illegal weighted graphs for complete MRRVs.) Figure 11(b) shows a sub-hamiltonian weighted graph associated with a complete MRRV. It has a hamiltonian subcycle $c_1 =< v_1, v_2, \ldots, v_6, v_1 >$ that contains all vertices. By Lemma 5, $\vec{n}$ has a complete sub-RRV $\vec{n_2} \in U_2$. In other words, $\vec{n_2}$ satisfies the following equalities:

$$n_{2,(1,2)} + n_{2,(1,3)} + n_{2,(1,4)} + n_{2,(1,5)} + n_{2,(1,6)} = 2 \quad (37)$$

$$n_{2,(1,2)} + n_{2,(2,3)} + n_{2,(2,4)} + n_{2,(2,5)} + n_{2,(2,6)} = 2 \quad (38)$$

$$n_{2,(1,3)} + n_{2,(2,3)} + n_{2,(3,4)} + n_{2,(3,5)} + n_{2,(3,6)} = 2 \quad (39)$$

$$n_{2,(1,4)} + n_{2,(2,4)} + n_{2,(3,4)} + n_{2,(4,5)} + n_{2,(4,6)} = 2 \quad (40)$$

$$n_{2,(1,5)} + n_{2,(2,5)} + n_{2,(3,5)} + n_{2,(4,5)} + n_{2,(5,6)} = 2 \quad (41)$$

$$n_{2,(1,6)} + n_{2,(2,6)} + n_{2,(3,6)} + n_{2,(4,6)} + n_{2,(5,6)} = 2. \quad (42)$$

Let $\vec{n_1} = \vec{n} - \vec{n_2}$. Since $\vec{n}$ is a complete MRRV, the constant c_1 in Equality (31) equals zero. By Equalities (31)–(36) and (13)–(18), we have the following equalities:

$$n_{2,(1,2)} + n_{2,(1,3)} + n_{2,(1,4)} + n_{2,(1,5)} + n_{2,(1,6)} = V - 2 \quad (43)$$

$$n_{2,(1,2)} + n_{2,(2,3)} + n_{2,(2,4)} + n_{2,(2,5)} + n_{2,(2,6)} = V - 2 \quad (44)$$

$$n_{2,(1,3)} + n_{2,(2,3)} + n_{2,(3,4)} + n_{2,(3,5)} + n_{2,(3,6)} = V - 2 \quad (45)$$

$$n_{2,(1,4)} + n_{2,(2,4)} + n_{2,(3,4)} + n_{2,(4,5)} + n_{2,(4,6)} = V - 2 \quad (46)$$

$$n_{2,(1,5)} + n_{2,(2,5)} + n_{2,(3,5)} + n_{2,(4,5)} + n_{2,(5,6)} = V - 2 \quad (47)$$

$$n_{2,(1,6)} + n_{2,(2,6)} + n_{2,(3,6)} + n_{2,(4,6)} + n_{2,(5,6)} = V - 2. \quad (48)$$

Obviously, $\vec{n_1} \in U_{V-2}$. Applying the similar techniques, we can show that all multiple graphs associated with degenerate complete MRRVs are sub-hamiltonian. Thus, $\Omega \subseteq \Omega'$. Based the above discussion, we have $\Omega' = \Omega$. □

Algorithm: RRV-Decomposition ($\vec{n}$)
Input: $\vec{n}$—An MRRV in U_V.
Output: $\vec{n_1}, \vec{n_2}$—MRRVs such that $\vec{n} = \vec{n_1} + \vec{n_2}$, $\vec{n_1} \in U_{V-2}$ and $\vec{n_2} \in U_2$.
/* Lines 1–7 construct a multiple graph $G_m(V_m, E_m)$. */
/* $\biguplus$ denotes the special "union" operation by keeping duplicate elements;
e.g., $\{a, b\} \biguplus \{a, c\} = \{a, a, b, c\}$. */
1 $V_m = \{v_1, v_2, \ldots, v_6\}$;
2 $C_1 = \left(V - \sum_{i=1}^{6} n_{1,i}\right)/2$;
3 **if** $c_1 \neq 0$ **then** /* degenerate complete MRRV */
4 let $n_{2,(1,2)} \leftarrow n_{2,(1,3)} \leftarrow \ldots \leftarrow n_{2,(1,6)} \leftarrow 0$;
5 $V_m \leftarrow V_m - \{v_1\}$;
6 $E_m = \{(v_i, v_j) | n_{i,j} \neq 0\}$;
7 $E_m = E_m \biguplus \{(v_i, v_j) | n_{i,j} \geq 2\}$;
8 $H \leftarrow$ all hamiltonian subcycles in $G_m(V_m, E_m)$;
9 $I \leftarrow$ set of independent hamiltonian subcycles which contain all vertices in V_m;
10 for each cycle $< v_{i_1}, v_{i_2}, \ldots, v_{i_k}, v_{i_1} > \in I$
11 **if** $k = 2$ **then**
12 $n_{2,(v_{i_1}, v_{i_2})} \leftarrow 2$;
13 **else**
14 $n_{2,(v_{i_1}, v_{i_2})} \leftarrow n_{2,(v_{i_2}, v_{i_3})} \leftarrow \ldots \leftarrow n_{2,(v_{i_k}, v_{i_1})} \leftarrow 1$;
15 $\vec{n_1} \leftarrow \vec{n} - \vec{n_2}$;
16 **Output** $\vec{n_1}$, $\vec{n_2}$.

Figure 10: Algorithm for RRV decomposition, assuming that all unused terminals, if any, are on side 1.

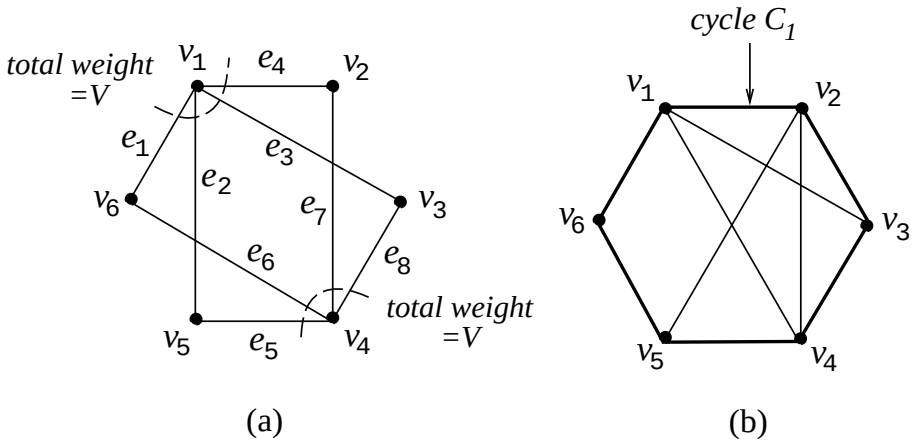

Figure 11: Weighted graphs for two complete MRRVs. (a) An illegal weighted graph—its total weights is equal to 2V. (b) A legal weighted graph with a hamiltonian subcycle $C_1 =< v_1, v_2, \ldots, v_6, v_1 >$.

Category	Number of weighted graphs	Number of illegal graphs	Number of legal graphs
α	1	0	1
β	3	0	3
γ	1	0	1
δ	52	12	40
Total	56	12	44

Table 1: Number of weighted graphs for complete $MRRVs$.

Two sub-blocks are said to be *independent* if they do not share any terminals. By Lemma 6, independent switch sub-blocks can be considered individually and merged to form a larger switch block, and the routable RRVs for the merged switch block are identical to those by applying vector addition operations on the routable RRVs for the independent switch sub-blocks. With the decomposition properties of symmetric switch blocks and RRVs, we can prove the following theorem by using mathematical induction.

Theorem 3 *The symmetric switch blocks are universal.*

Proof: By Definition 2, we shall show that, for an HSB M_h of size V constructed by Algorithm Symmetric_Switch_Block, $\vec{n}$ is routable on M_h if and only if the following inequalities are simultaneously satisfied:

$$\begin{aligned}
n_{1,2} + n_{1,3} + n_{1,4} + n_{1,5} + n_{1,6} &\leq V \\
n_{1,2} + n_{2,3} + n_{2,4} + n_{2,5} + n_{2,6} &\leq V \\
n_{1,3} + n_{2,3} + n_{3,4} + n_{3,5} + n_{3,6} &\leq V \\
n_{1,4} + n_{2,4} + n_{3,4} + n_{4,5} + n_{4,6} &\leq V \\
n_{1,5} + n_{2,5} + n_{3,5} + n_{4,5} + n_{5,6} &\leq V \\
n_{1,6} + n_{2,6} + n_{3,6} + n_{4,6} + n_{5,6} &\leq V.
\end{aligned}$$

For the HSBs constructed by the algorithm, we have the following key observations (see Figure 8). For an HSB of an even V, we can partition it into $V/2$ non-interacting sub-blocks (shown in Figure 8(a)); each sub-block has the same topology as that of S_2 shown in Figure 8(a). For an HSB of an odd V, we can partition it into $\lceil V/2 \rceil$ non-interacting sub-blocks, with each of the $\lfloor V/2 \rfloor$ sub-blocks identical to S_2 and one sub-block with a clique topology formed by the six terminals from the middle of each side (see Figure 8(b)). Because terminals in different sub-blocks are non-interacting, each sub-block can be considered independently (Lemma 6). Therefore, each symmetric HSB consists of $\lfloor V/2 \rfloor$ independent universal switch sub-blocks of size two, and additional one of size one if V is odd. Further, by Lemma 2, an HSB of size two constructed by Algorithm Symmetric_Switch_Block is universal.

(If) For an *even* V, by Lemma 6, we can decompose a vector $\vec{n} = (n_{1,2}, n_{1,3}, \ldots, n_{1,6}, n_{2,3}, \ldots, n_{2,6}, n_{3,4}, \ldots, n_{3,6}, n_{4,5}, n_{4,6}, n_{5,6})$ into $V/2$ sub-RRVs $\vec{n_i} = (n_{i,(1,2)}, n_{i,(1,3)}, \ldots, n_{i,(1,6)}, n_{i,(2,3)}, \ldots, n_{i,(2,6)}, n_{i,(3,4)}, \ldots, n_{i,(3,6)}, n_{i,(4,5)}, n_{i,(4,6)}, n_{i,(5,6)})$, where $i = 1, 2, \ldots, V/2$, such that each sub-RRV satisfies the following set of inequalities:

$$n_{i,(1,2)} + n_{i,(1,3)} + n_{i,(1,4)} + n_{i,(1,5)} + n_{i,(1,6)} \leq 2 \quad (49)$$

$$n_{i,(1,2)} + n_{i,(2,3)} + n_{i,(2,4)} + n_{i,(2,5)} + n_{i,(2,6)} \leq 2 \quad (50)$$

$$n_{i,(1,3)} + n_{i,(2,3)} + n_{i,(3,4)} + n_{i,(3,5)} + n_{i,(3,6)} \leq 2 \quad (51)$$

$$n_{i,(1,4)} + n_{i,(2,4)} + n_{i,(3,4)} + n_{i,(4,5)} + n_{i,(4,6)} \leq 2 \quad (52)$$

$$n_{i,(1,5)} + n_{i,(2,5)} + n_{i,(3,5)} + n_{i,(4,5)} + n_{i,(5,6)} \leq 2 \quad (53)$$

$$n_{i,(1,6)} + n_{i,(2,6)} + n_{i,(3,6)} + n_{i,(4,6)} + n_{i,(5,6)} \leq 2, \quad (54)$$

where $\vec{n} = \sum_{i=1}^{V/2} \vec{n_i}$. By Lemma 2, each RRV $\vec{n_i}$ satisfying Inequalities (49)–(54) must be routable on the HSB of size two, and by Lemma 6, $\vec{n}$ is also routable on the symmetric HSB of size V.

For an *odd* V, by Lemma 6, we can decompose a vector $\vec{n}$ into $\lceil V/2 \rceil$ sub-RRVs $\vec{n_i}$'s, where $i = 1, 2, \ldots, \lceil V/2 \rceil$, such that each of the sub-RRVs $\vec{n_i}, i = 1, 2, \ldots, \lfloor V/2 \rfloor$ satisfies the set of Inequalities (49)–(54), and the remaining one $\vec{n}_{\lceil V/2 \rceil}$ satisfies the following set of inequalities:

$$n_{\lceil V/2 \rceil,(1,2)} + n_{\lceil V/2 \rceil,(1,3)} + n_{\lceil V/2 \rceil,(1,4)} + n_{\lceil V/2 \rceil,(1,5)} + n_{\lceil V/2 \rceil,(1,6)} \leq 1 \quad (55)$$

$$n_{\lceil V/2 \rceil,(1,2)} + n_{\lceil V/2 \rceil,(2,3)} + n_{\lceil V/2 \rceil,(2,4)} + n_{\lceil V/2 \rceil,(2,5)} + n_{\lceil V/2 \rceil,(2,6)} \leq 1 \quad (56)$$

$$n_{\lceil V/2 \rceil,(1,3)} + n_{\lceil V/2 \rceil,(2,3)} + n_{\lceil V/2 \rceil,(3,4)} + n_{\lceil V/2 \rceil,(3,5)} + n_{\lceil V/2 \rceil,(3,6)} \leq 1 \quad (57)$$

$$n_{\lceil V/2 \rceil,(1,4)} + n_{\lceil V/2 \rceil,(2,4)} + n_{\lceil V/2 \rceil,(3,4)} + n_{\lceil V/2 \rceil,(4,5)} + n_{\lceil V/2 \rceil,(4,6)} \leq 1 \quad (58)$$

$$n_{\lceil V/2 \rceil,(1,5)} + n_{\lceil V/2 \rceil,(2,5)} + n_{\lceil V/2 \rceil,(3,5)} + n_{\lceil V/2 \rceil,(4,5)} + n_{\lceil V/2 \rceil,(5,6)} \leq 1 \quad (59)$$

$$n_{\lceil V/2 \rceil,(1,6)} + n_{\lceil V/2 \rceil,(2,6)} + n_{\lceil V/2 \rceil,(3,6)} + n_{\lceil V/2 \rceil,(4,6)} + n_{\lceil V/2 \rceil,(5,6)} \leq 1. \quad (60)$$

We have $\vec{n} = \sum_{i=1}^{\lceil V/2 \rceil} \vec{n_i}$. By Lemma 2, each RRV $\vec{n_i}$ satisfying the set of Inequalities (49)–(54) must be routable on the symmetric HSB of size two. Further, the last RRV is also routable on an HSB of size one (a clique of six terminals). Hence, by Lemma 6, $\vec{n}$ is also routable on the symmetric HSB of size V.

(Only If) For an HSB M_h of size V, the total number of connections routed through each side of M_h cannot exceed V. Hence, if $\vec{n}$ is routable on M_h, Inequalities (1)–(6) must be satisfied. □

Theorem 4 *No HSBs with less than* $15V$ *switches can be universal.*

Proof: By Definition 2, an RRV with only one non-zero component V such as $(V,0,0,0,0,0,0,0,0,0,0,0,0,0,0)$, $(0,V,0,0,0,0,0,0,0,0,0,0,0,0,0)$, ..., $(0,V,0,0,0,0,0,0,0,0,0,0,0,0,V)$ is routable on a universal HSB. Hence it needs at least V non-interacting switches for each type of connections to construct a universal HSB. Since there are 15 types of connections in an HSB, the smallest number of switches needed to construct a universal HSB is $15V$. □

As mentioned in Subsection 3.1, the total number of switches used in a 6-sided symmetric switch block is $15V$. Thus, the symmetric HSBs are the "cheapest" universal ones, i.e., it uses the minimum number of switches to construct a universal switch block. Note that the $15V$ switches requirement is quite small, compared to a fully connected HSB which has $15V^2$ switches. By Theorem 1, any two isomorphic switch blocks have the same routing capacity. Hence, we have following lemma.

Lemma 7 *For any two isomorphic switch blocks $M_h(T,S)$ and $M'_h(T',S')$, $M_h(T,S)$ is universal if and only if $M'_h(T',S')$ is universal.*

By Lemma 7, we can obtain a whole class of universal switch blocks by performing isomorphism operations on a symmetric switch block.

4 Clique-Based Switch Blocks

In this section, we consider the clique-based HSBs associated with those used in the Xilinx XC4000-series FPGAs (see Figure 12(a)) and show that the clique-based HSBs are not universal. Figures 12(a) and (b) show two clique-based switch blocks of four and six sides, respectively (Note that the switch block shown in Figure 12(a) is used in Xilinx XC4000-series FPGAs.). Nevertheless, as shown in Figure 5(c), the clique-based HSB is not universal since the RRV $(0,0,0,0,0,1,1,0,0,1,0,0,0,0,0)$ which satisfies the dimension constraint is not routable on the 6-sided clique-based switch block of size two. For the feasibility condition of the 6-sided clique-based switch blocks, we have the following lemma.

Lemma 8 *For a clique-based HSB $M_h(S_h,T_h)$ of size V, $\vec{n}$ is routable on M_h only if the following set of inequalities are simultaneously satisfied:*

$$n_{1,2}+n_{1,3}+n_{1,4}+n_{1,5}+n_{1,6} \leq V \quad (61)$$

$$n_{1,2}+n_{2,3}+n_{2,4}+n_{2,5}+n_{2,6} \leq V \quad (62)$$

$$n_{1,3}+n_{2,3}+n_{3,4}+n_{3,5}+n_{3,6} \leq V \quad (63)$$

$$n_{1,4}+n_{2,4}+n_{3,4}+n_{4,5}+n_{4,6} \leq V \quad (64)$$

$$n_{1,5}+n_{2,5}+n_{3,5}+n_{4,5}+n_{5,6} \leq V \quad (65)$$

$$n_{1,6}+n_{2,6}+n_{3,6}+n_{4,6}+n_{5,6} \leq V \quad (66)$$

$$n_{p,q}+n_{q,r}+n_{r,p} \leq V,\ p,q,r=1,2,\ldots 6, p\neq q, q\neq r,\ \text{and } p\neq r. \quad (67)$$

Proof: It is obvious that if an RRV is routable (on the clique-based HSB M_h), it must satisfy the dimension constraint Inequalities (61)–(66). For a clique-based HSB M_h of size V, we have the following key observation. Consider three arbitrary sides p, q, and r of M_h. The switches incident on p, q, r form V triangles, and these triangles are non-interacting and thus can be considered independently. (See Figure 12(b).) Since a triangle

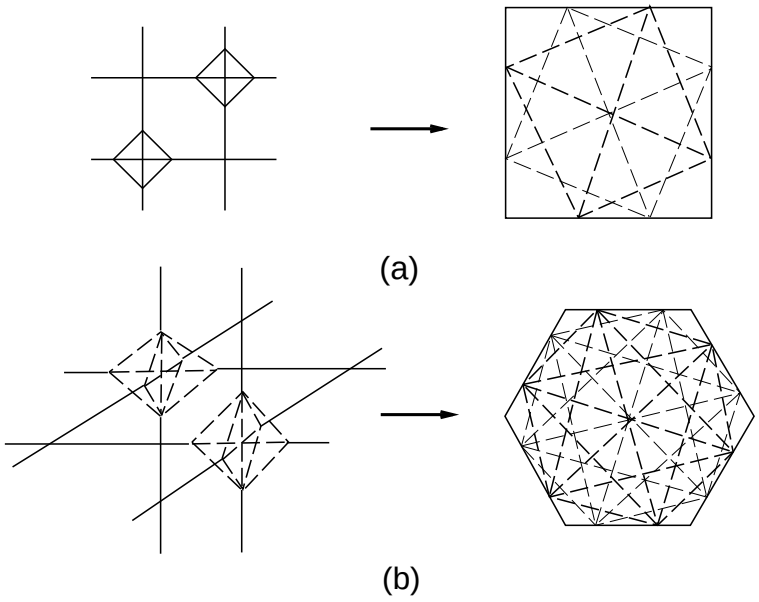

Figure 12: Clique-based switch blocks. (a) A 4-sided one. (b) A 6-sided one.

can be routed by at most one connection, the total number of connections that can route on p, q, r cannot exceed V. Thus the set of Inequalities (67) is also a necessary condition. □

Theorem 5 *The clique-based HSBs are not universal.*

Let $U_h(V)$ ($C_h(V)$) be the set of RRVs which satisfies the dimension constraint for the universal (clique-based) HSBs of size V. Let $|U_h(V)|$ ($|C_h(V)|$) be the cardinality of $U_h(V)$ ($C_h(V)$). We have the following corollary.

Corollary 5.1 *(1)* $C_h(V) \subseteq U_h(V)$*; (2)* $|C_h(V)| \leq |U_h(V)|$.

5 Experimental Results

To explore the effects of switch-block architectures on routing on a 3D FPGA, we implemented a maze router in the C language and ran on a SUN Ultra workstation. We tested the area performance of the router based on the CGE [8] and the SEGA [7] benchmark circuits. A logic-block pin was connected to any of the W tracks in the adjacent routing channel. We routed these circuits on a two-layer 3D FPGA and randomly assigned the layer for each terminal of a net. The switch-block architectures used were the symmetric switch blocks and clique-based (Xilinx XC4000-like) switch blocks. The quality of a switch block was evaluated by the area performance of the detailed router. Table 2 shows the results. For the results listed in this table, we determined the minimum number of tracks W required for 100% routing completion for each circuit, using the two kinds of switch blocks. Because net ordering often affects the performance of a maze router, we routed the benchmark circuits by using the following three net-ordering schemes to avoid possible biases: (1) net order as given in the original benchmark circuits, (2) shortest net first (non-decreasing order of net lengths), and (3) longest net first (non-increasing order of net lengths). Our results show that, between the

Circuit	#Logic blocks	#Con.	Number of tracks needed for detailed-routing completion					
			Original Order		Shortest net first		Longest net first	
			Symmetric	Clique	Sym.	Cliq.	Sym.	Cliq.
BUSC	$13 \times 12 \times 2$	392	7	9	7	7	8	8
DMA	$18 \times 16 \times 2$	771	9	9	8	8	10	10
BNRE	$22 \times 21 \times 2$	1257	9	9	8	9	10	10
DFSM	$23 \times 22 \times 2$	1422	9	9	8	8	9	9
Z03	$27 \times 26 \times 2$	2135	9	10	8	9	10	10
9symml	$11 \times 10 \times 2$	259	6	6	6	7	7	8
alu2	$15 \times 13 \times 2$	511	7	7	7	8	8	9
alu4	$19 \times 17 \times 2$	851	8	9	9	9	10	11
apex7	$12 \times 10 \times 2$	300	6	7	6	7	8	8
example2	$14 \times 12 \times 2$	444	8	8	8	8	9	10
k2	$22 \times 20 \times 2$	1256	11	11	10	11	12	12
term1	$10 \times 9 \times 2$	202	7	8	6	6	7	8
too_large	$15 \times 14 \times 2$	519	7	9	8	8	9	9
vda	$17 \times 16 \times 2$	722	7	9	8	9	9	10
Total	-	-	109	118	106	112	125	131
Comparison	-	-	1.00	1.08	1.00	1.06	1.00	1.05

Table 2: Minimum numbers of tracks needed for detailed-routing completion.

two kinds of switch blocks, the symmetric switch blocks usually needed the minimum W's for 100% routing completion, no matter what net order was used. The results show that our symmetric switch blocks improve the routability at the chip level. (An average of 6% improvement in the area performance was achieved.) We also performed experiments to explore the effects of net density on the area performance of switch blocks. We randomly generated connections on a $15 \times 15 \times 3$ (number of logic blocks in the three layers) 3D FPGA. For this purpose, we assume that the number of pins on each logic blocks is unlimited (so that we could test denser circuits). As shown in Figure 13, no matter how dense the circuit is (numbers of connections ranging from 400 to 1600), the symmetric switch blocks consistently outperform the clique-based switch blocks. (An average of 10% improvement in the area performance was achieved.)

6 Conclusion

We have presented a class of universal switch blocks for the three-dimensional FPGAs and shown that they have better routability than others of the topology associated with those used in the Xilinx XC4000 FPGAs. Further, the decomposition property of the universal switch block provides a key insight into its layout implementation with a smaller silicon area.

References

[1] M. J. Alexander, J. P. Cohoon, J. L. Ganley, and G. Robins, "Three-Dimensional Field-Programmable Gate Arrays," in *Proc. IEEE Intl. ASIC Conf.*, Austin, TX, September 1995, pp. 253–256.

[2] S. D. Brown, R. J. Francis, J. Rose, and Z. G. Vranesic, *Field-Programmable Gate Arrays*, Kluwer Academic Publishers, Boston, MA, 1992.

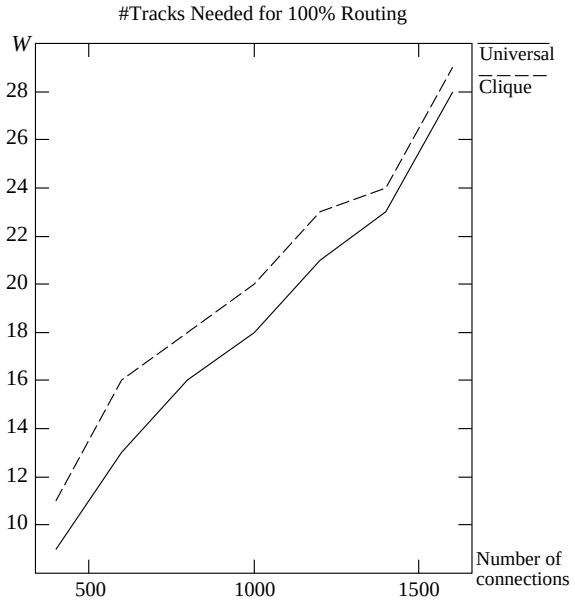

Figure 13: Comparison of the area performance by using the symmetric switch blocks and clique-based switch blocks for different numbers of connections on a $15 \times 15 \times 3$ 3D-FPGA.

[3] Y.-W. Chang, D. F. Wong, and C. K. Wong, "Universal switch blocks for FPGA design," *ACM Trans. Design Automation of Electronic Systems*, vol. 1, no. 1, pp. 80–101, Jan. 1996.

[4] Y.-W. Chang, D. F. Wong, and C. K. Wong, "Design and analysis of FPGA/FPIC switch modules," in *Proc. IEEE Int. Conf. Computer Design*, pp. 394–401, Austin, TX, Oct. 1995.

[5] J. Depreitere, H. Neefs, H. V. Marck, J. V. Campenhout, B. D. R. Baets, H. Thienpont, and I. Veretennicoff, "An optoelectronic 3-D field programmable gate array," in *Proc. 4th Intl. Workshop on Programmable Logic Applications*, Prague, September 1994.

[6] I. Dobbelaere, A. E. Gamal, D. How, and B. Kleveland, "Field programmable MCM Systems—Design of an Interconnection Frame," in *Custom Integrated Circuits Conf.*, Boston, MA, 1992, pp. 4.6.1-4.6.4.

[7] G. G. Lemienx and S. D. Brown, "A detailed routing algorithm for allocating wire segments in field-programmable gate arrays," in *Proc. ACM/SIGDA Physical Design Workshop*, pp. 215–216, Lake Arrowhead, CA, 1993.

[8] J. Rose and S. Brown, "Flexibility of interconnection structures for field-programmable gate arrays," *IEEE J. Solid State Circuits*, vol. 26, no.3, pp. 277–282, 1991.

[9] Y. Sun, T. -C, Wang, C. K. Wong, and C. L. Liu, "Routing for symmetric FPGAs and FPICs," in *Proc. IEEE/ACM Int. Conf. Computer-Aided Design*, pp. 486–490, Santa Clara, Nov. 1993.

[10] S. Thakur, Y. -W, Chang, D. F. Wong, and S. Muthukrishnan, "Algorithms for an FPGA switch module routing problem with application to global routing," *IEEE Trans. on Computer-Aided Design*, Jan. 1997.

[11] W. Tsu, "A comparison of universal and Xilinx switches," CS294-7 Project Report, University of California at Berkeley, Spring 1997.

[12] G.-M. Wu and Y.-W. Chang, "Switch matrix architecture and routing for FPDs," in *Proc. ACM Int. Symp. Physical Design*, pp. 481–486, Monterey, CA, April, 1998.

[13] K. Zhu, D. F. Wong, and Y.-W. Chang, "Switch module design with application to two-dimensional segmentation design," in *Proc. IEEE/ACM Int. Conf. Computer-Aided Design*, pp. 481–486, Santa Clara, Nov. 1993.

For reviewer's reference, the preliminary version of this work was cited in the following article by EE Times: "FPGA'99: Advanced processes unleash architectural ideas," in *EE Times*, Feb. 23, 1999

MONTEREY, Calif. - It may not be obvious that the FPGA industry is in upheaval. But attendees at the FPGA'99 conference here had a front-row seat to watch architectural change, driven on the tide of process advances, begin a sweep through the industry. The key underpinnings of this generation's FPGA architectures have already been undermined, and new structures are already beginning to appear in their place. But indications from conference papers are that the change has only just begun.

The driving force behind all this activity is, not surprisingly, process improvement. Where a generation ago FPGA designers were delighted to get a fast CMOS process with three usable metal layers, they are now being offered vastly superior speeds, up to six layers of high-conductivity metal and the ability to route signals over delicate logic structures. These advances have negated - or at least brought up for reexamination - many of the assumed truths of FPGA architecture.

The most prominent truth to be questioned is the supremacy of the four-input lookup table (LUT) as the basic element of combinatorial logic. Research by Jonathan Rose and associates at the University of Toronto years ago established that the ideal combination of utilization and performance could be achieved by an FPGA built out of a uniform array of four-input LUTs.

But, as presenters from Actel Corp. pointed out in their opening paper, Rose's research assumed an interconnect architecture without hierarchy, and also assumed that it was impossible to route over logic. With current processes, these assumptions are no longer necessary.

Technically, assaults on the doctrine of homogeneous architecture began some time ago, with the inclusion of SRAM blocks into FPGAs. But the dominance of the four-input LUT has just in this generation been seriously challenged.

The first attack came from Altera Corp., with the incorporation of even more flexible memory blocks into its Apex architecture. In a presentation Monday (Feb.22), Altera pointed out that the Embedded System Blocks (ESBs) in the new architecture served logic as well as memory functions. In common with the Embedded Array Blocks in the Flex architecture, the ESBs can be configured as ROM and used as wide-input LUTs. But in addition, the ESBs can be configured as AND arrays, very similar to the AND arrays that form the basis of Altera's Max CPLD family. While the wide LUT configuration permits single-level implementation of an arbitrary 1-bit function of up to 11 inputs, the AND array configuration can implement up to 16 bits of output functions from 32 inputs. Of course, as in any product-term structure, not all possible combinations of functions can be implemented. Thus the ESBs give Altera a way to accommodate either very dense clusters of combinatorial logic or very wide fan-in functions much more efficiently than they could be handled with four-input LUTs.

An entirely different approach to the same end was described by Vantis Corp. In that vendor's latest FPGA family, very fast local interconnect is used to, in effect, cascade three-input LUTs to form four-, five- and six-input LUTs within a local island of logic. This permit's Vantis' design tools to work with, in effect, an heterogeneous array of LUT of varying widths, while the underlying silicon retains the simplicity of an array of homogeneous three-input LUT islands.

Actel has carried this idea in a slightly different direction in its new reprogrammable FPGA architecture, which is now sampling. Repeating Rose's original research after removing the assumptions about non-hierarchical routing and no over-the-top routing, the Actel developers concluded that in the latest processes, a basic logic element that included both three-input and two-input LUTs would be more efficiently used, particularly by data path compilation tools. Hence their new architecture, based on islands of logic suspended in a three-layered routing hierarchy, employs basic blocks of one flip-flop, two three-input LUTs and one two-input LUT, sewn together and linked to nearest neighbors by very fast (0.25-ns) local interconnect.

These papers have shown that fast local interconnect has changed the ground rules for logic topology. But global interconnect topologies came under as much examination as logic in this year's presentations. As the amount of metal available to designers grows, the question becomes not how to get a minimum of links between logic elements, but how to use additional links.

The answer, it appears, will be borrowed from the world of supercomputing. In a poster session, several papers considered the possibility of three-dimensional and even four-dimensional topologies for linking the growing islands of logic in an FPGA.

Herman Schmit of Carnegie Mellon University demonstrated that a partially populated four-dimensional interconnect scheme - essentially, a hypercube - behaved much better under intensive routing demands than existing two-dimensional arrays. And a team from the National Chiao Tung University of Taiwan explored the micro-architecture of three-dimensional switching blocks - the

all-important connection points between routing elements.

Meanwhile, Rose and his associates at Toronto have not been sleeping. In another poster paper, Rose and Vaughn Betz demonstrated that a mixture of pass-transistor-controlled segments and buffered interconnect lines could outperform an interconnect scheme composed exclusively of either pass transistors or buffers. Hence heterogeneity may be coming not only to logic elements, but to interconnect programming elements as well.

The bottom line for the architectural papers at this year's conference appears to be simple: everything is up for reconsideration. Heterogeneous architectures are in. Enabled by the relative unimportance of logic real estate on the modern die, logic islands of growing sophistication are in. And complex, hierarchical interconnect schemes are on the way.

The next question, mostly skirted by the architecture papers, is the one that stopped heterogeneous architectures in their tracks several years ago. Can tools be developed that can exploit the new heterogeneous structures? Or will the increasingly clear advantages to be gained by more complex FPGA hardware be lost on tool suites still struggling to exploit a field of sparsely-connected four-input LUTs. That question remains on the table.