LINEAR AMPLIFIER DESIGN

**IMPEDANCE MATCHING**

\[ G_1 = \text{Transducer power gain} \]

(most commonly used gain definition)

S parameter description of 2 port chosen for best measurement accuracy

\[ G_1 = F(S_{11}, S_{21}, S_{12}, S_{22}, I_{G}, I_L) \]

(12 numbers)

\(|S_{21}|\) and \(|S_{42}|\) may be expressed as either dB or ratio

\[ |S_{21}| \text{ dB} = 20 \log |S_{21}| \]

Notes:

**STABILITY AND GAIN**

Rollett's Stability Factor:

\[ k = \frac{1 + IS_{12} \cdot S_{21} \cdot S_{11} \cdot S_{22}}{2 IS_{12} I S_{22}} \]

k > 1 guarantees stability

Design Goal for Gain:

\[ G_f = G_m = \frac{IS_{12}}{IS_{22}} \]

If \( k < 1 \) then:

\[ G_f \geq G_m = \frac{IS_{12}}{IS_{22}} \]

k > 1 allows simultaneous conjugate match with positive resistance terminations

If k < 1 there is no maximum gain

At least 9 other definitions of power gain exist, from \(|S_{21}|\) (transducer gain) to \(U\) (unilateral gain), the largest possible power gain.

Common systems use HP 8510, HP 8409 or HP 8410.

Common 50Ω test fixtures are available from HP, Maury Microwave, and Inter-Continental Microwave.

Notes:

Accuracy depends on f and |Γ| (usually ±5% expected)

"Plumbing" is usually a cost-consistency tradeoff

Fixture must reflect actual part mounting, including bond wires, grounding techniques, etc.

Calibration of Network Analyzer ends at connector reference plane

Measurement of DUT includes test fixture and transitions, which must be de-embedded from the data

MEASURED S PARAMETERS (AT 41435)
Typical Scattering Parameters, Common Emitter

Both low noise and power (gain) bias points shown

With proper models, S parameters can be simulated as well as measured.
Note that bond wires are included as part of the package model.

Package model accurate to 8 GHz

Equivalent circuit topology follows from analysis of physical layout.

TOUCHSTONE™ File 41435.TCKT

Combines equivalent circuit for bipolar and package equivalent circuit.

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PACKAGE EQUIVALENT CIRCUIT

(414x or "3S" Package)

Notes:

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SIMULATION OF AT41435 S PARAMETERS

Circuit Description

Range of Analysis

Subject of Analysis

Notes:

A-23
The output file of the simulation can be saved (as AT4135.OUT) by pressing shift F4 while the output is displayed on the monitor screen.

With minor editing (placing an "!'" in the left margin before each line of the heading to make them comments) the file can be used directly as a device S parameter description in an S2PA statement.

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SIMULATED PARAMETERS OF AT4135
Data File Format

<table>
<thead>
<tr>
<th>Frequency</th>
<th>S11</th>
<th>S12</th>
<th>S21</th>
<th>S22</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.000000</td>
<td>0.045</td>
<td>0.039</td>
<td>0.039</td>
<td>0.039</td>
</tr>
<tr>
<td>2.000000</td>
<td>0.029</td>
<td>0.029</td>
<td>0.029</td>
<td>0.029</td>
</tr>
<tr>
<td>3.000000</td>
<td>0.029</td>
<td>0.029</td>
<td>0.029</td>
<td>0.029</td>
</tr>
<tr>
<td>4.000000</td>
<td>0.029</td>
<td>0.029</td>
<td>0.029</td>
<td>0.029</td>
</tr>
</tbody>
</table>

Notes:

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COMPARISON OF SIMULATED AND MEASURED S PARAMETERS AT4135 - S11, AND S22

<table>
<thead>
<tr>
<th>S11 DATA</th>
<th>S11</th>
<th>S21</th>
<th>S22</th>
</tr>
</thead>
<tbody>
<tr>
<td>AT4135</td>
<td>0.01</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>DATA</td>
<td>0.02</td>
<td>0.03</td>
<td>0.03</td>
</tr>
</tbody>
</table>

Notes:

AT4135 = Output of simulation
DATA = Catalog data (measured S parameters).
\( \text{AT41435} = \text{Output of simulation} \)

\( \text{DATA} = \text{Catalog data (measured S parameters)} \)

Notes:

\( \text{AT41435} = \text{Output of simulation} \)

\( \text{DATA} = \text{Catalog data (measured S parameters)} \)

Notes:
BEGIN EXAMPLE 1

TOUCHSTONE file
414AMP_1.CKT
Gain block design

DESIGN EXAMPLE 1
A Single Stage Small Signal Amplifier

System Use: Gain Block for 4 GHz TVRO
Desired Performance: Gain > 9 dB
Frequency = 3.7 - 4.2 GHz

Notes:

Major Design Concerns
Stability
Match

DESIGN STEPS
Single Stage Small Signal Amplifier

1 Select Transistor
2 Design DC Bias Network
3 Design RF Matching Network
   A Match S11 for Minimum Reflected Power
   B Match S21 for Maximum Gain
   C Combine Input and Output Matches
4 Integrate DC and RF Networks

Notes:

A-26
DEVICE SELECTION

Consider AT 4142S: Bias = V_{CC} = 8 V, I_{C} = 10 mA

S Parameters at GHz:

Then: D = S_{22}S_{11} - S_{21}S_{12} = .0482 \angle -17.4^\circ

\[ k = \frac{1 + (.0482)^2 - (.65)^2 - (.36)^2}{2 (1.96) (10)} = 1.15 \] Unconditionally

Stable at 4 GHz

G_{max} = \frac{(1.15 - \sqrt{(1.15^2 - 1))}}{1} = 11.6 or 10.6 dB Suitable

Gain at 4 GHz

Notes:

Graph confirms correct device selection

DEVICE SELECTION: GAIN AND STABILITY VS FREQUENCY

AT4142S AT V_{CC} = 8V, I_{C} = 10mA

Notes:
Step 2

DC BIAS DESIGN

Notes:

Step 3

Match S_{11} for minimum reflected power
Use minimum element topology

AT41435 INPUT MATCH

Match:
1. S_{11} to A (Z Plane)
2. A to B (Y Plane)
3. B to 50\(\Omega\) (Y Plane)

Notes:
**AT41435 INPUT MATCH STRUCTURE**

1. Series Transmission Line
   340\( \mu \)m Long (\sim 0\% Length)
2. Open Stub
   \( Z_0 = 50 \Omega \Rightarrow w = 0.080^\circ \)
   90.6\( \mu \)m Long \( \Rightarrow f = 329^\circ \)

1/32\" Teflon-Fiberglass Board
\( S_{11} \) Matched to 50\( \Omega \)
(Minimum Reflected Power)

\( \lambda_g = \frac{c}{f \sqrt{\varepsilon_r}} \)
where 
\( c = \) speed of light
\( = 3 \times 10^8 \) cm/sec

\( f = \) frequency

\( \varepsilon_r = \) effective dielectric constant

\[ \frac{3 \times 10^8 \text{ cm/sec}}{(4 \text{ GHz}) \left( \sqrt{2.2} \right) \left( 2.54 \text{ cm/in} \right)} = 1.991 \text{ inches} \]

\[ \frac{59.5}{360} \lambda_g = 0.329 \text{ inches} \]

**Notes:**

---

**AT41435 OUTPUT MATCH**

Match: 3 \( S_{21} \) to A (Z Plane)
A to B (Y Plane)
4 B to 50\( \Omega \) (Y Plane)

**Notes:**

---

Step 3 continued
Match \( S_{22} \) for maximum gain
\[ \lambda_g = 1.994 \text{ inches} \]

\[
\frac{52.5^\circ}{360^\circ} \times \lambda_g = 0.290 \text{ inches}
\]

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**AT41435 OUTPUT MATCH STRUCTURE**

3. Series Transmission Line
   \[ \varphi \rightarrow S \rightarrow 0 \]

4. Short Stub
   \[ Z_0 = 50 \Omega \Rightarrow \varphi = 0.080^\circ \]
   \[ 52.5^\circ \text{ Long} \Rightarrow S = 0.290^\circ \]

**Notes:**

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Step 3 concluded
Combine input and output matches

Nodal circuit description

TOUCHSTONE simulation
Circuit file 414AMP ula.CKT
Data file AT41435A.S2P
(Avanteck AT41435 at low noise bias)

Parasitics added to simplified design

**AVANTEK**

**SIMULATION OF INTEGRATED DESIGN**

Notes:
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OPTIMIZATION OF RF DESIGN

Before: 4 GHz

Opt

After: 3.7-4.2 GHz

Note proper initial design means computer optimization is a fine tune.

Notes:

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SCHEMATIC OF OPTIMIZED AMPLIFIER

Step 4

Notes: